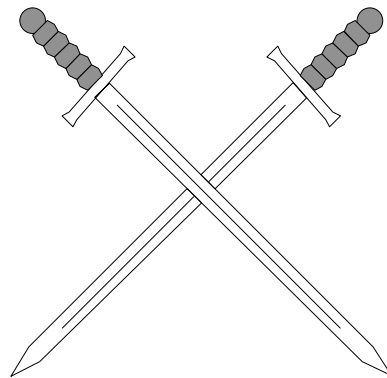


YELLOWKNIFE



4.2

FINAL

This schematic describes the Yellowknife X4 platform.
All information is subject to change. Contact PowerPC
Applications at <http://www.mot.com/SPS/PowerPC> to
obtain updated schematics and other information.



NOTES:


- 1) Unless otherwise specified:
All resistors are SMD0805, in ohms, 0.1W, +/-5%
All capacitors are SMD0805, in microfarads (uF), +/-20%.
All inductances are in microhenries (uH).
All ferrites are Z=50 ohms at 100 MHz.
All fuses are self-resetting polyswitch (PTC) devices.
- 2) Most IC devices shown have default connections to appropriate power and ground levels unless shown explicitly otherwise.
- 3) Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.
- 4) Motorola and the Motorola colophon are registered trademarks of Motorola. PowerPC is a trademark of IBM. MacOS, ADB and GeoPort are trademarks of Apple. Other trademarks are the respective property of their respective copyright holders. Moose trained to fill out complicated insurance forms by Sigi Churchill. All rights reserved. All this fine print can't be good for your eyes.
- 5) The sheet-to-sheet cross reference format is:
Sheet "-": VertZoneLetter HorizZoneNumber
- 6) Components surrounded by a dashed/crossed-out box are not to be installed by default; they are for test or manufacturing purposes only:

- 7) All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

TABLE OF CONTENTS

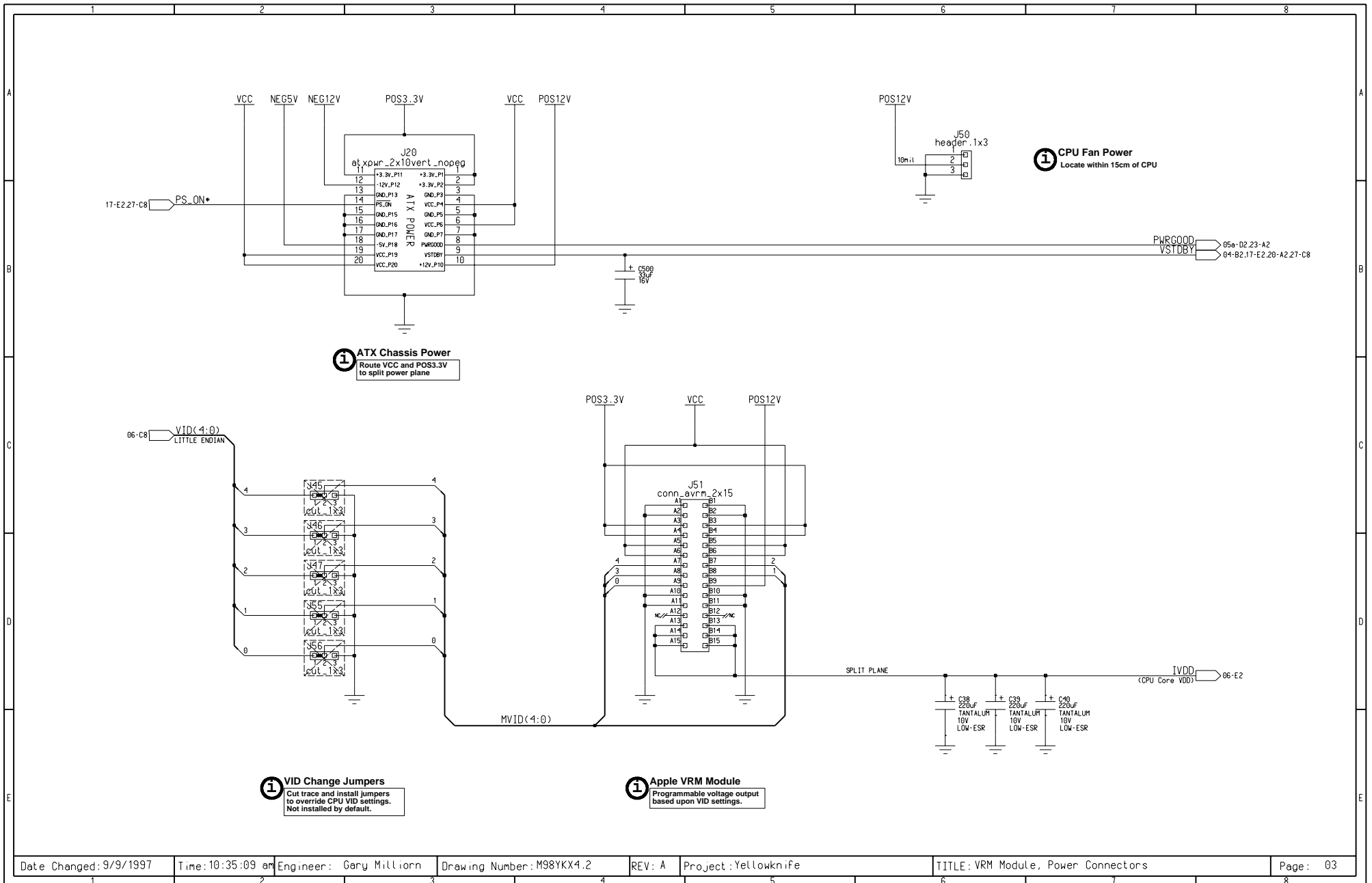
PG	Description
1	Information
2	Block Diagram
2a	System Configuration
3	Power Supply
4	System Power Control
5	Primary Clock Generation
5a	Skew-controller Clock Generation
6	PowerPC Interposer PGA Socket
7	MPC106 Memory/PCI Controller
8	Cache TagRAM/Comparator
9	Cache Memory
10	Memory Control Termination
11	Memory Data Bus Buffers
11a	Parity/ROM Address Bus Buffers
12	DIMM Memory #1 and #2
12a	DIMM Memory #3
13	MacOS Toolbox ROM; Boot ROM
14	Hydra: Apple I/O Controller
14a	Apple I/O: ADB and GeoPort Slot; SCSI
15	PCI/ISA Bridge
16	IDE Connectors
17	Super I/O Controller
18	Floppy Disk, PC I/O Slot
19	Serial Ports
20	NVRAM, Battery power supply
21	PCI Slots #1 and #2
21a	PCI Slot #3
22	ISA Slots
23	System reset
24	Spares, ESP Port
25	Bypass capacitors
26	Global pullups/pulldowns
27	Chassis Header
28	Routing Instructions

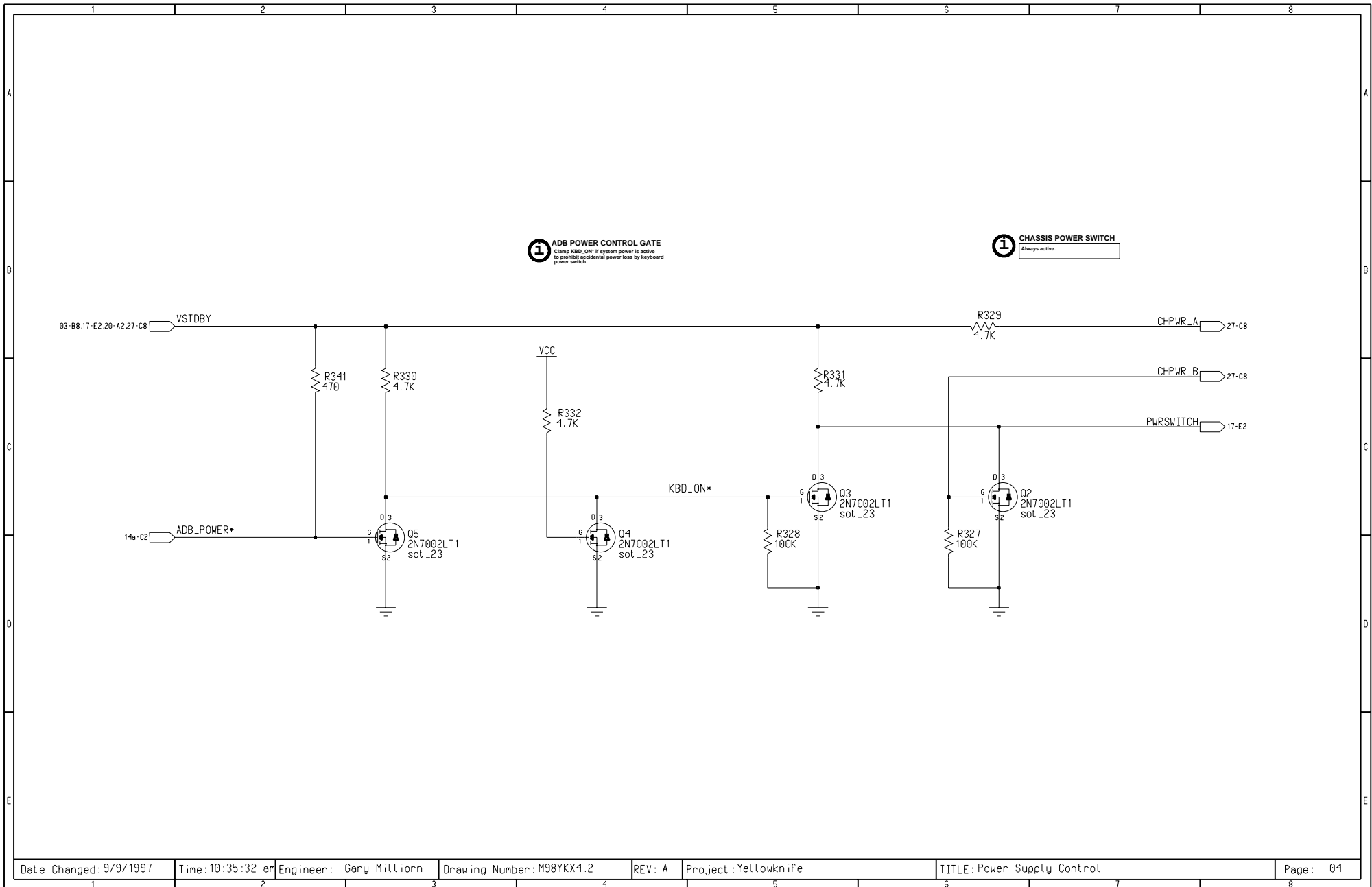
REV	DATE	CHANGES
X1	09SEP96	Original
X2	11OCT96	PWB fab error fixed
X3	23NOV96	Errata "I" included
X4	03APR97	Performance upgrade
X4.1	02JAN98	Updates
X4.2	01SEP98	Notes; Final Cleanup

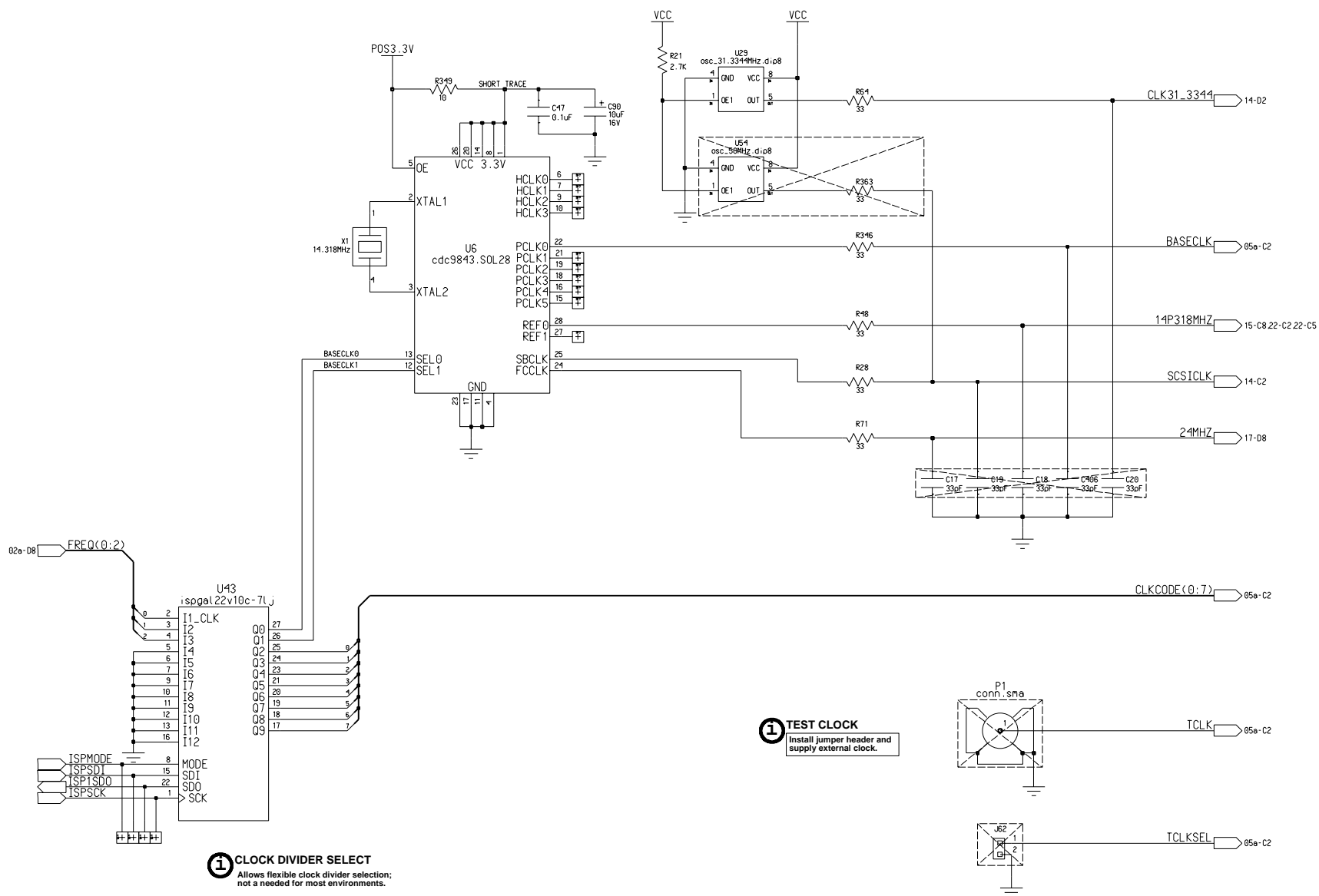
Yellowknife
PowerPC Multi-OS Platform
Version X4
Copyright 1998 by Motorola Inc.

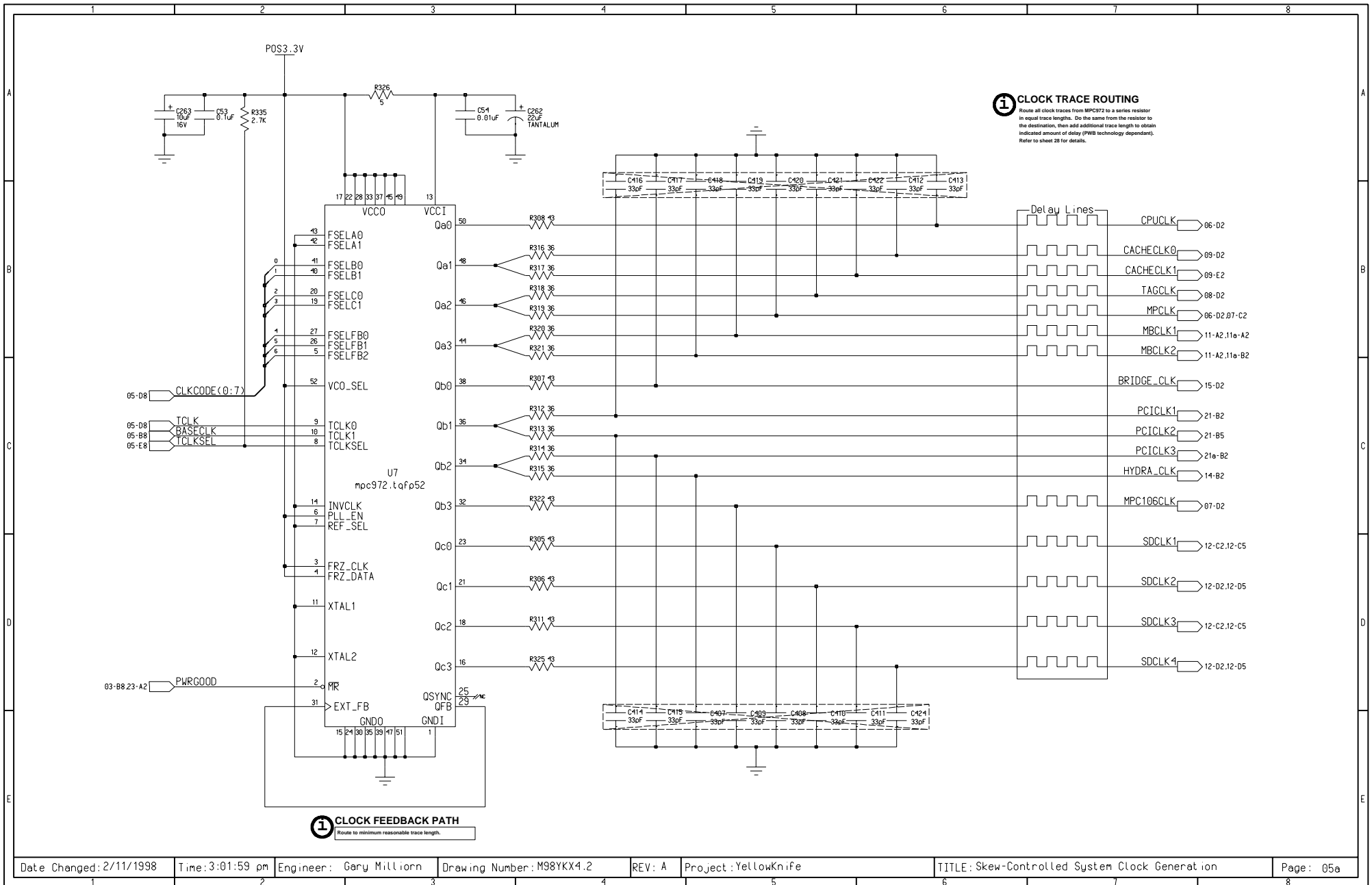
Team Yellowknife

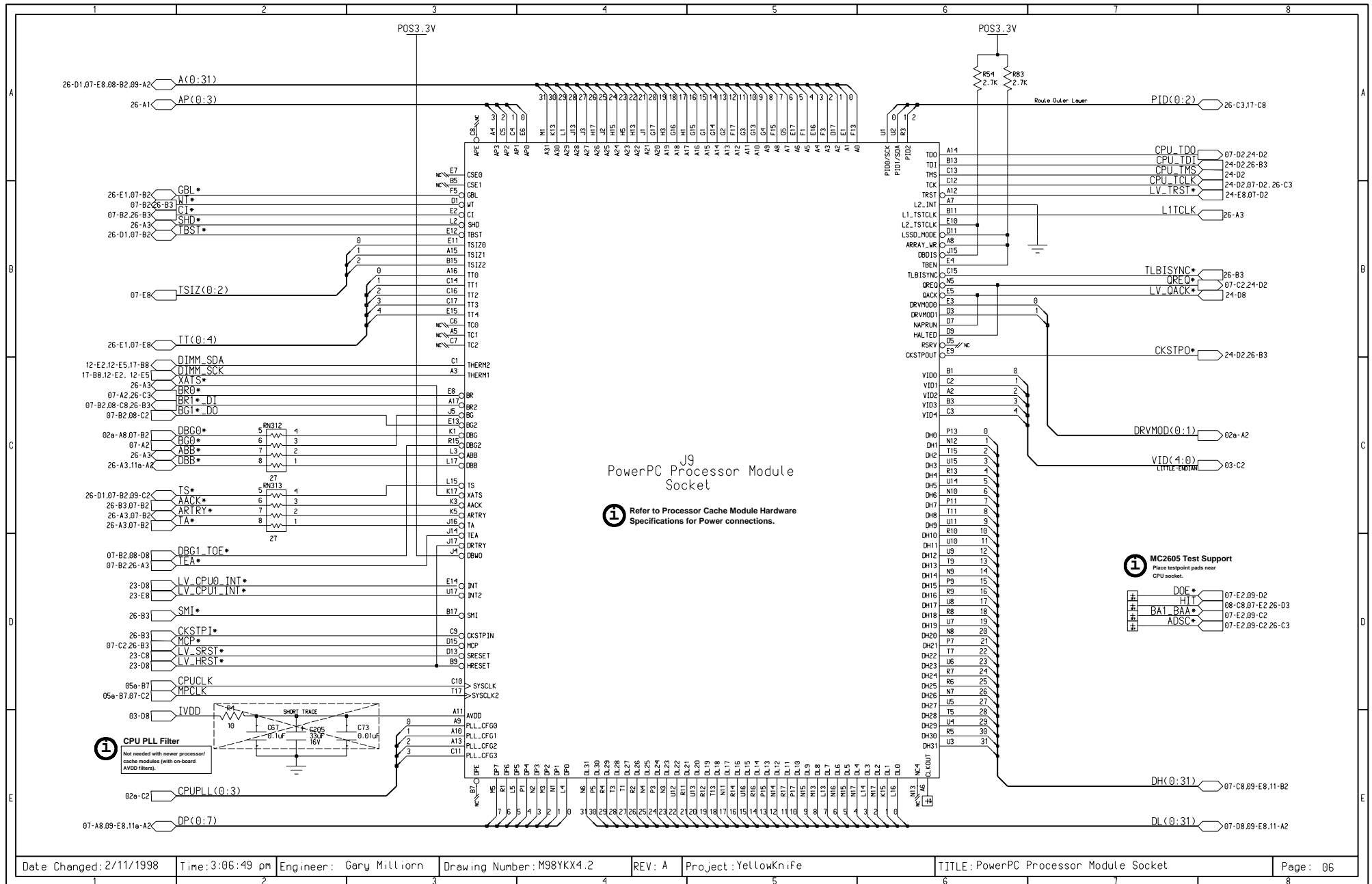
Gary Milliorn
Jeff Nutt
Margarito Trevino
Joey Tsai
Pat Darnell
Steve Foster
Gary Wojcik
Earl Lord
Wayne Long
Ivan Erickson
Gary Kromann
Dave Bernstein
Gregg Mack
and introducing...
Sparky the backwards tantalum

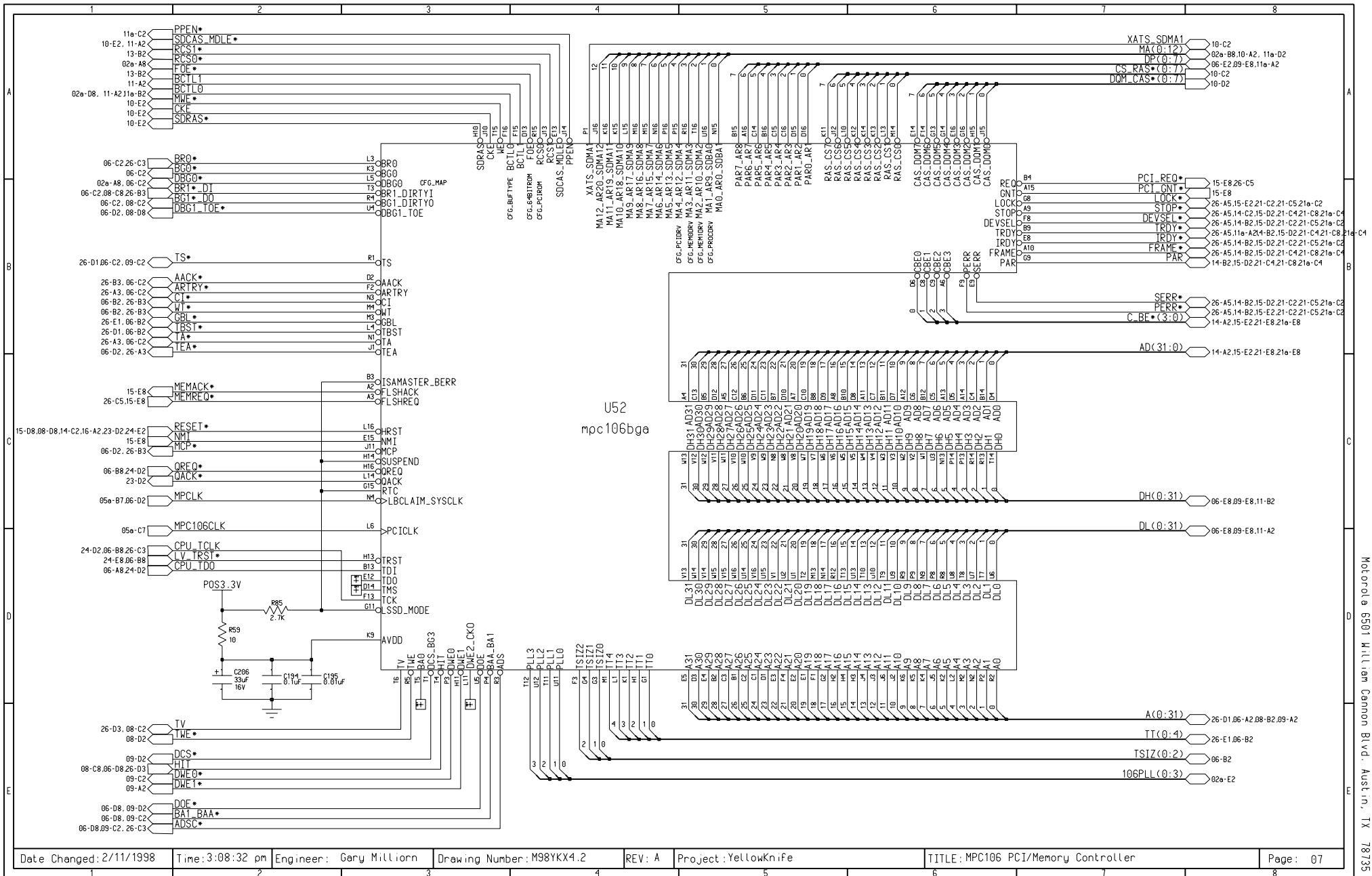


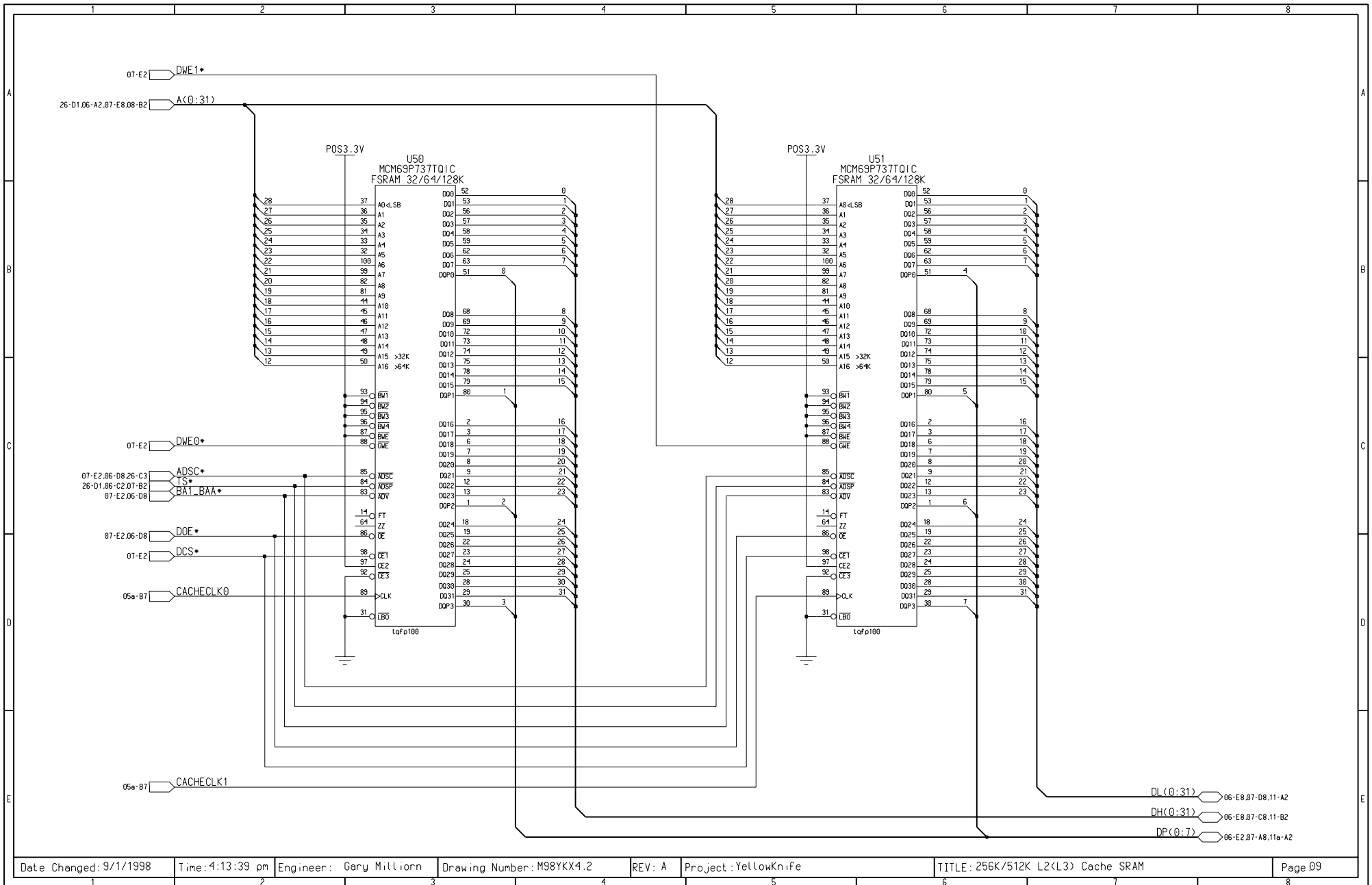


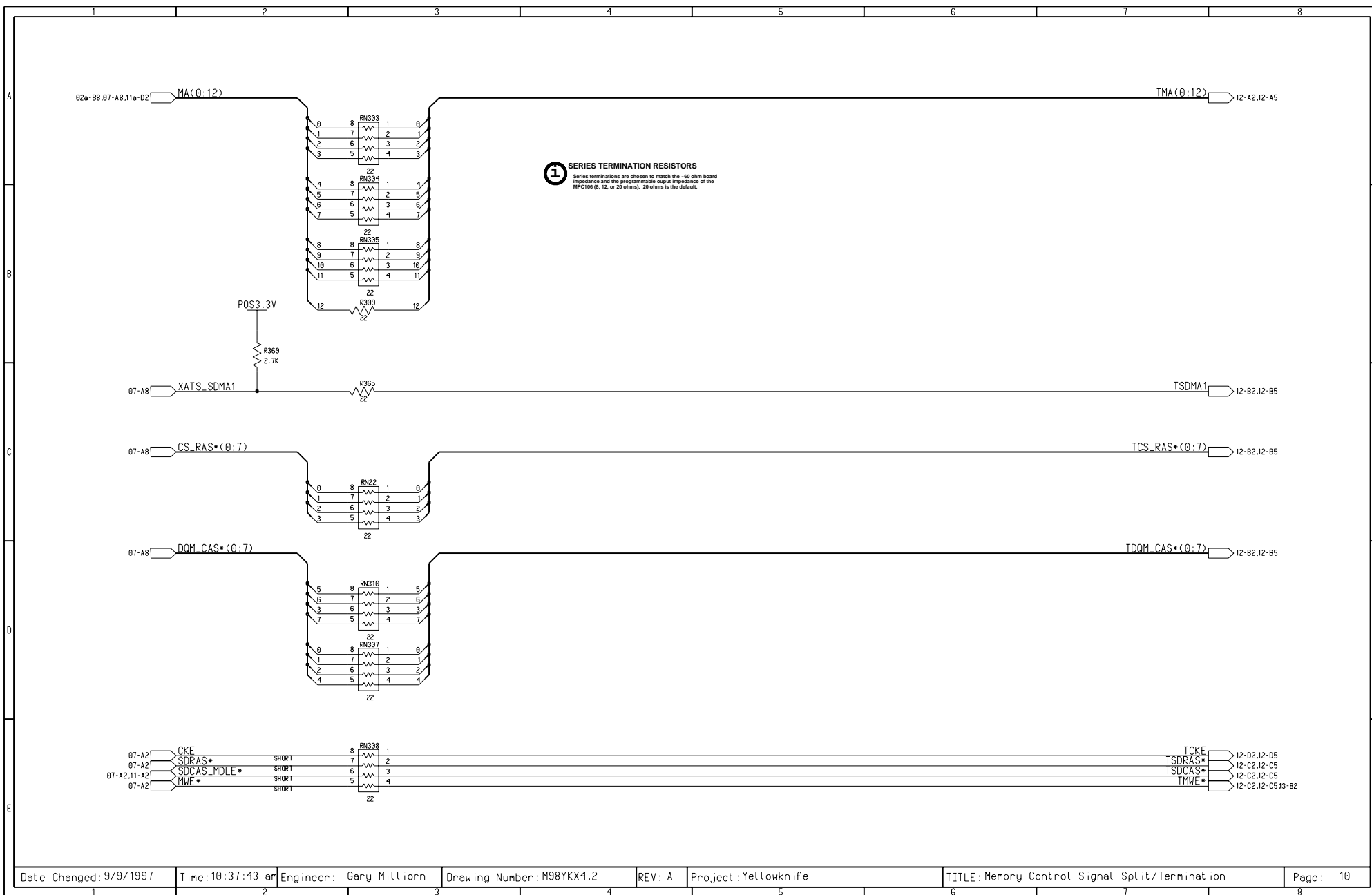


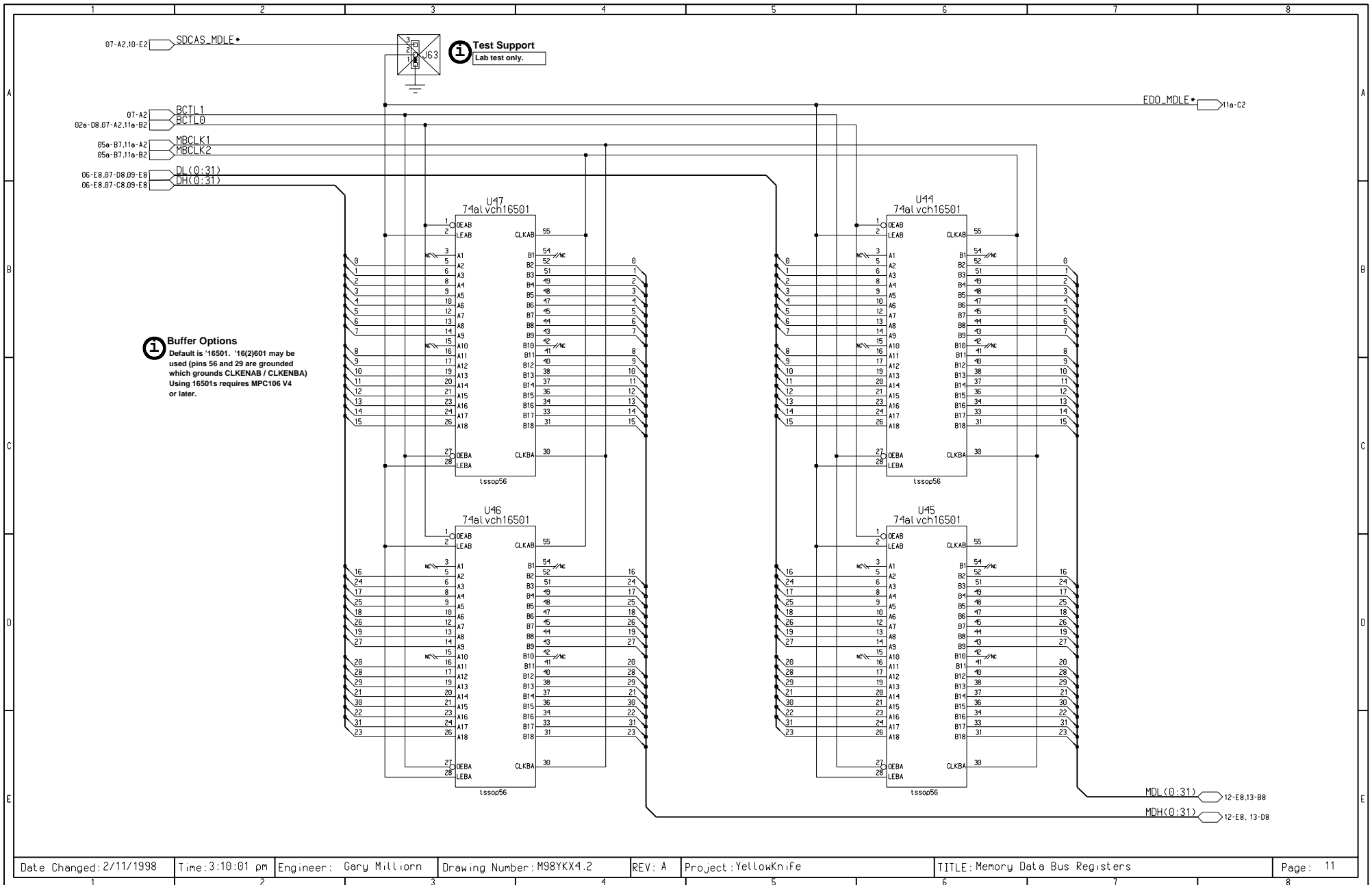


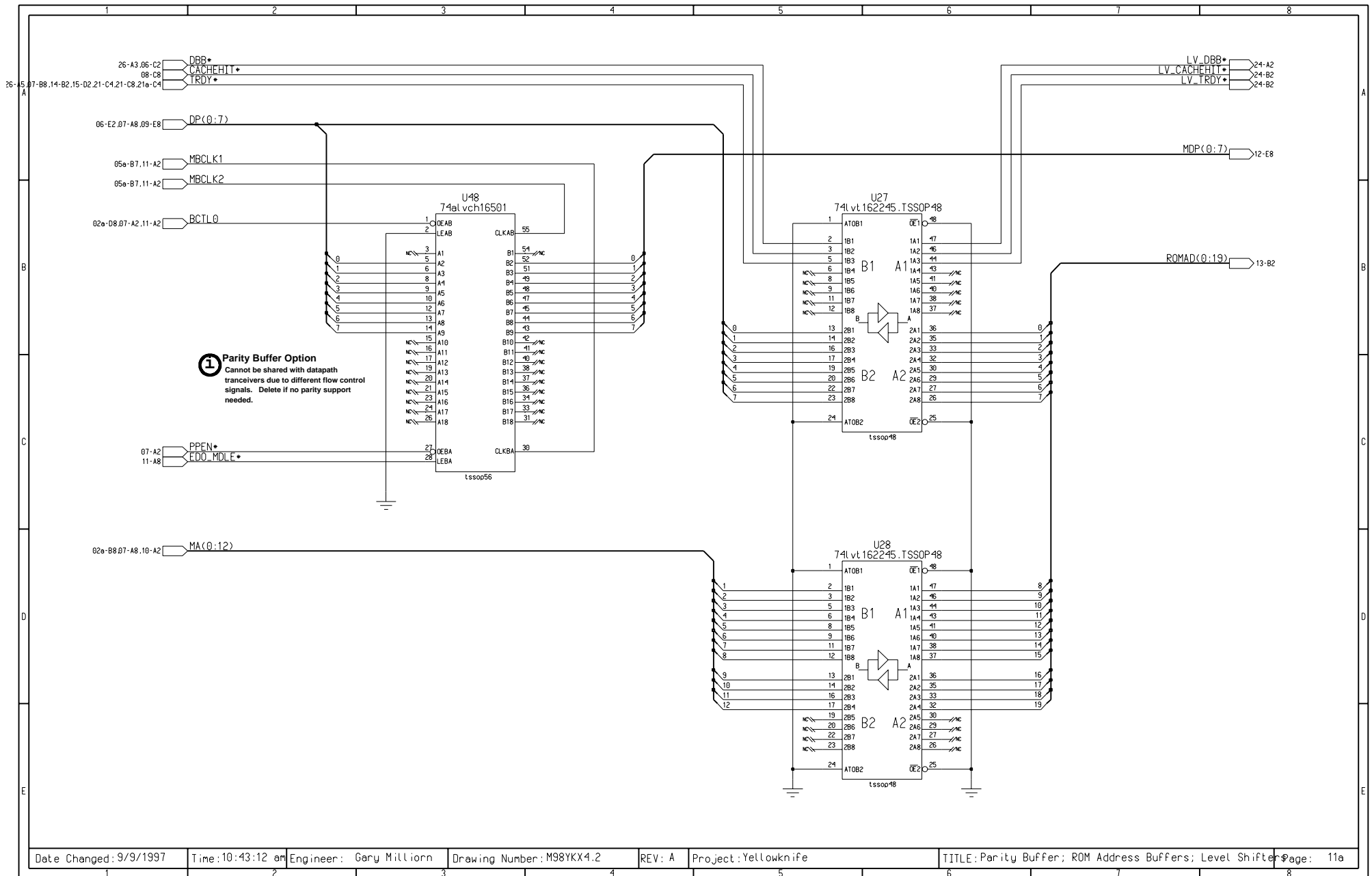


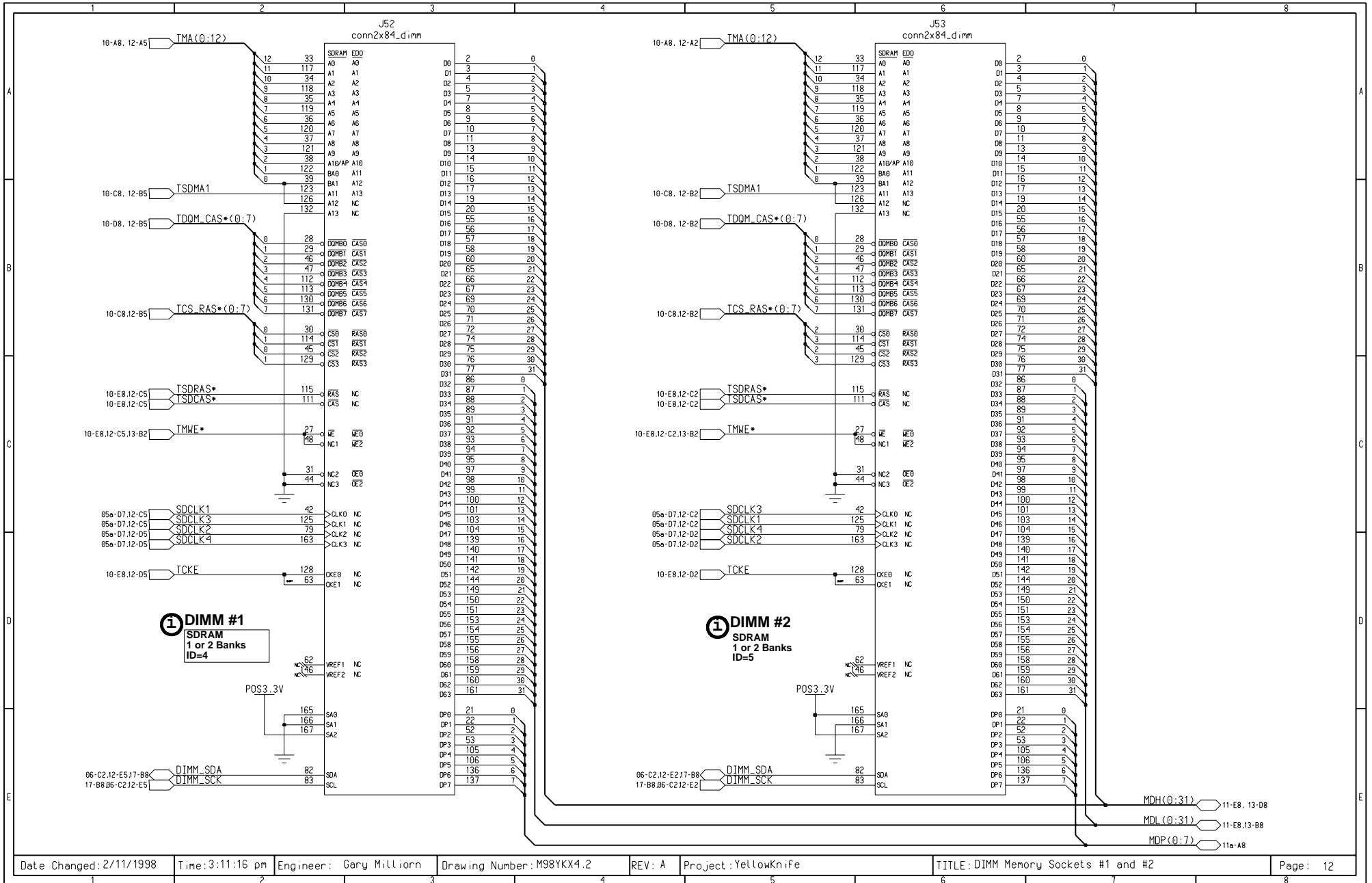


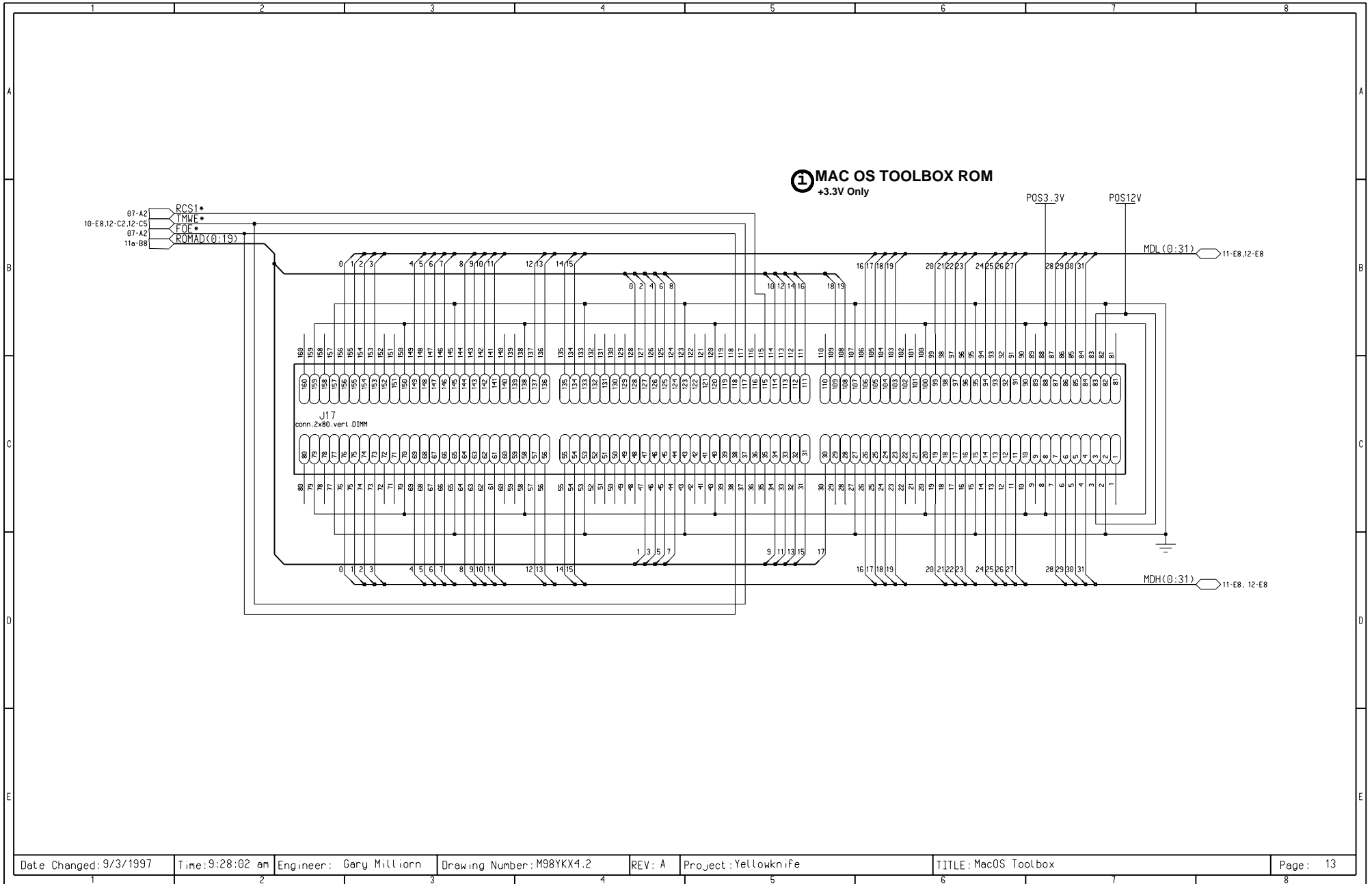


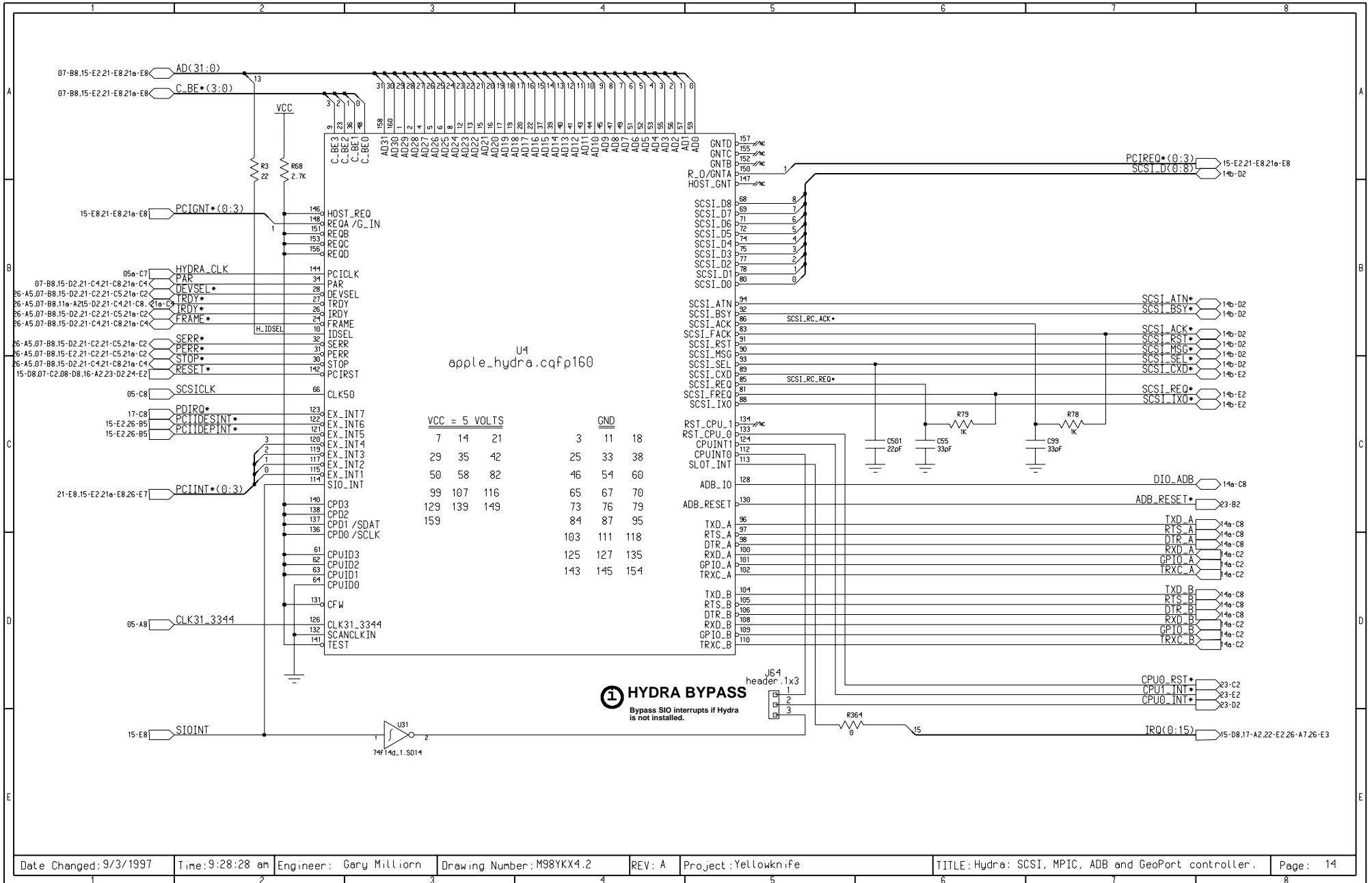


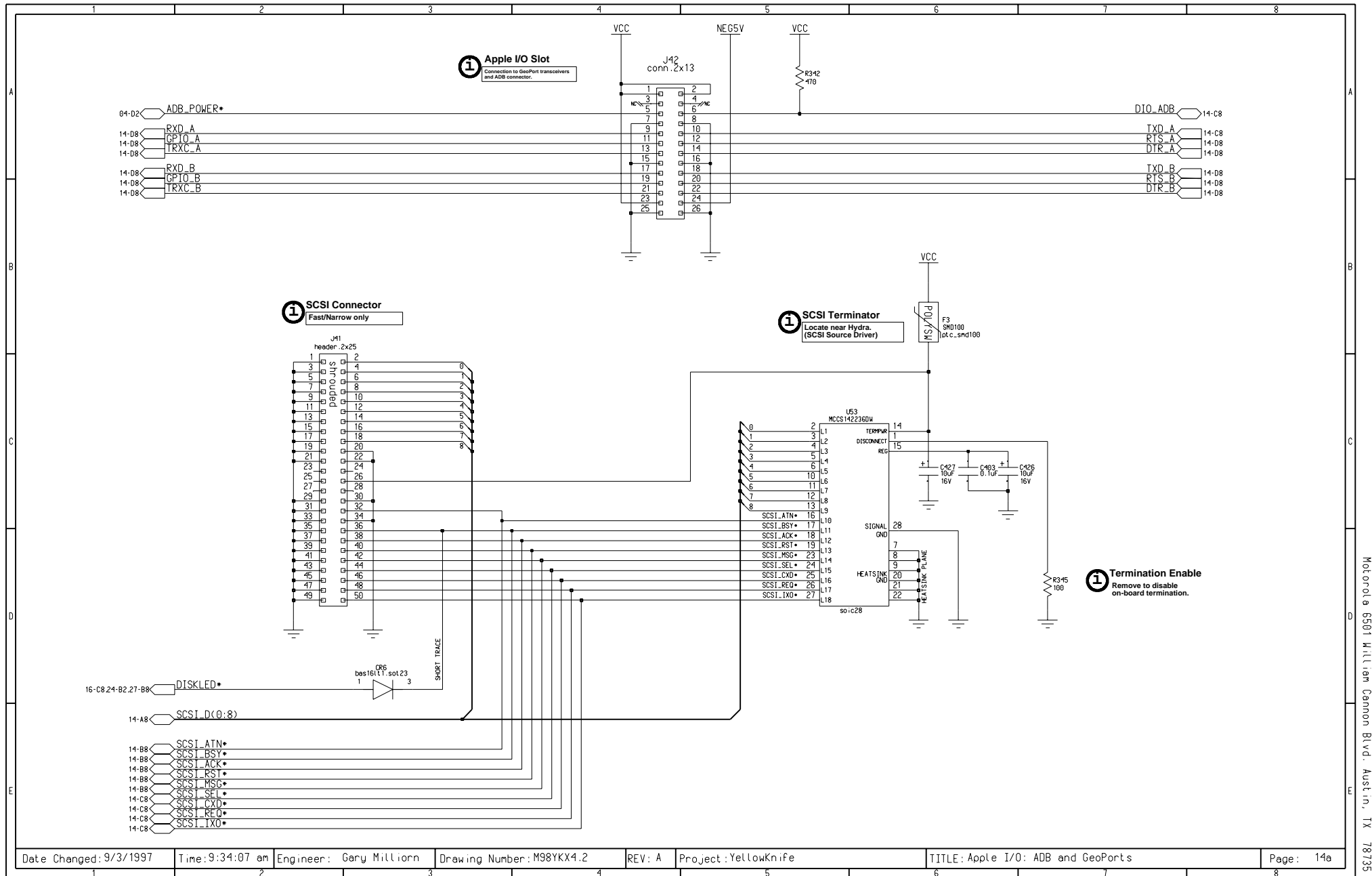


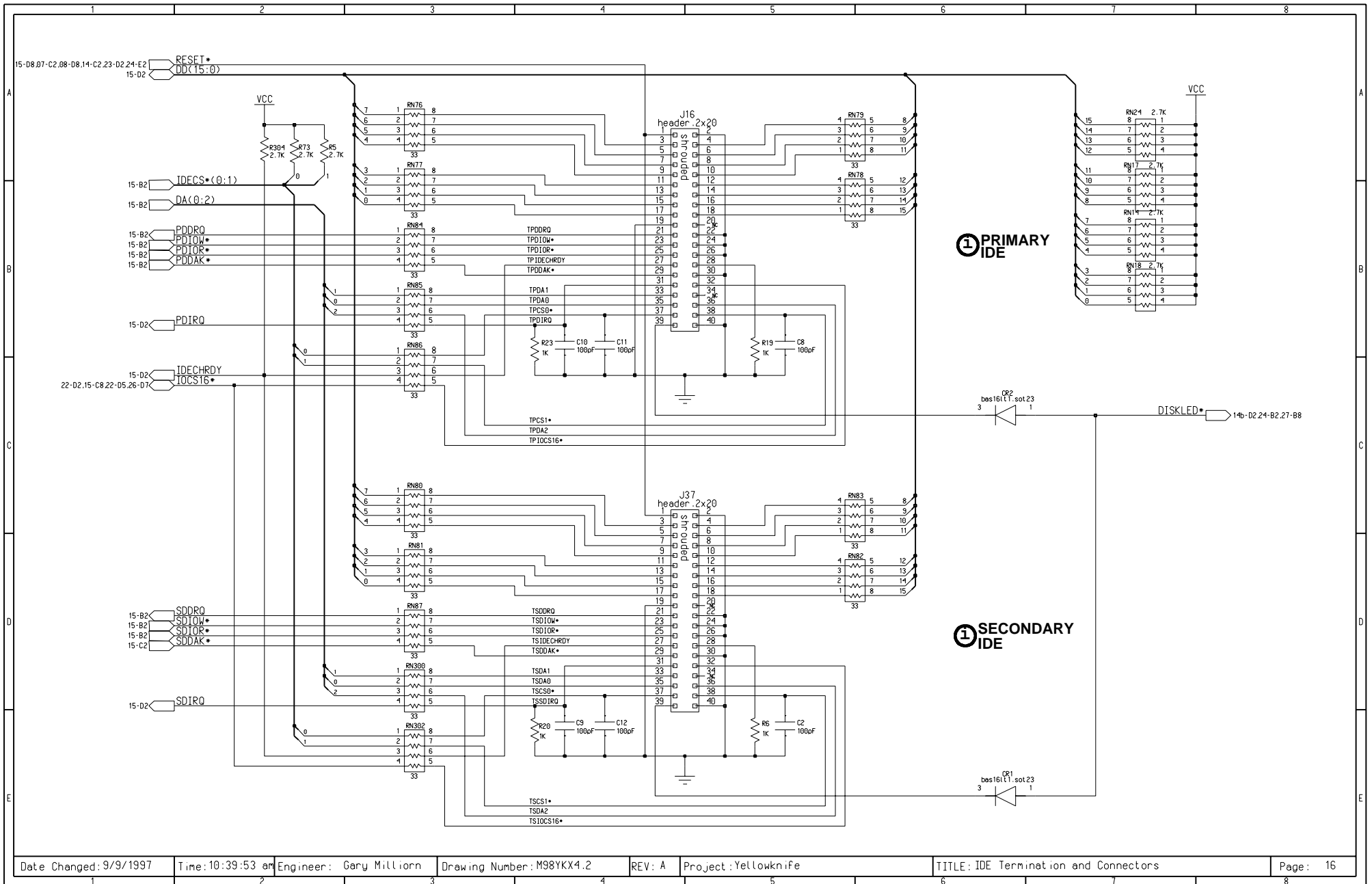


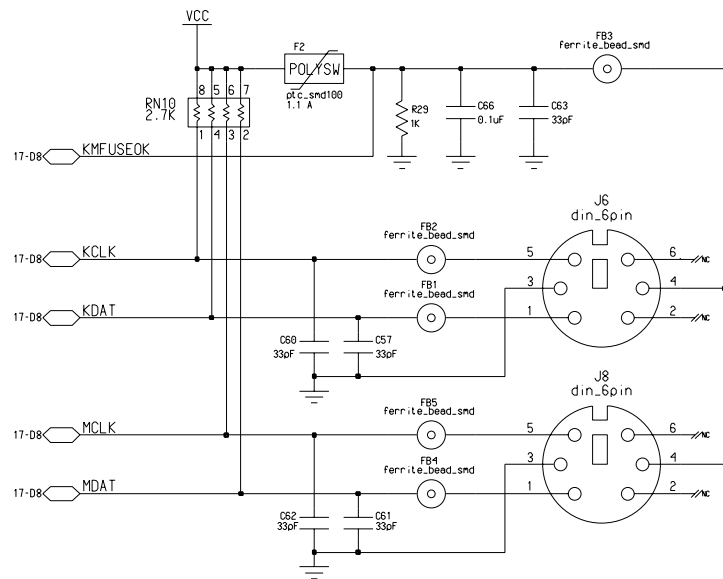






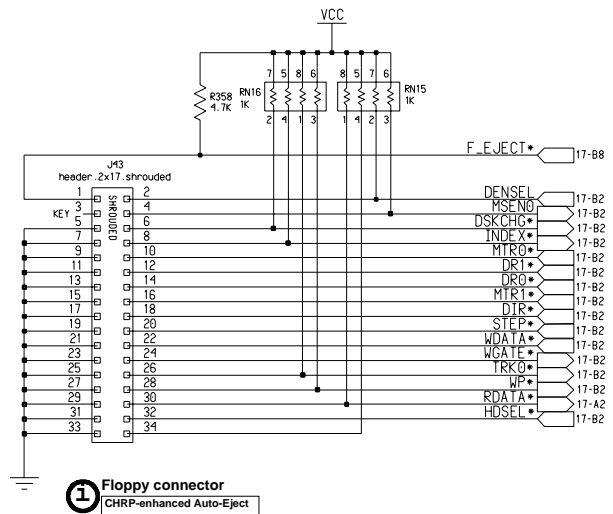






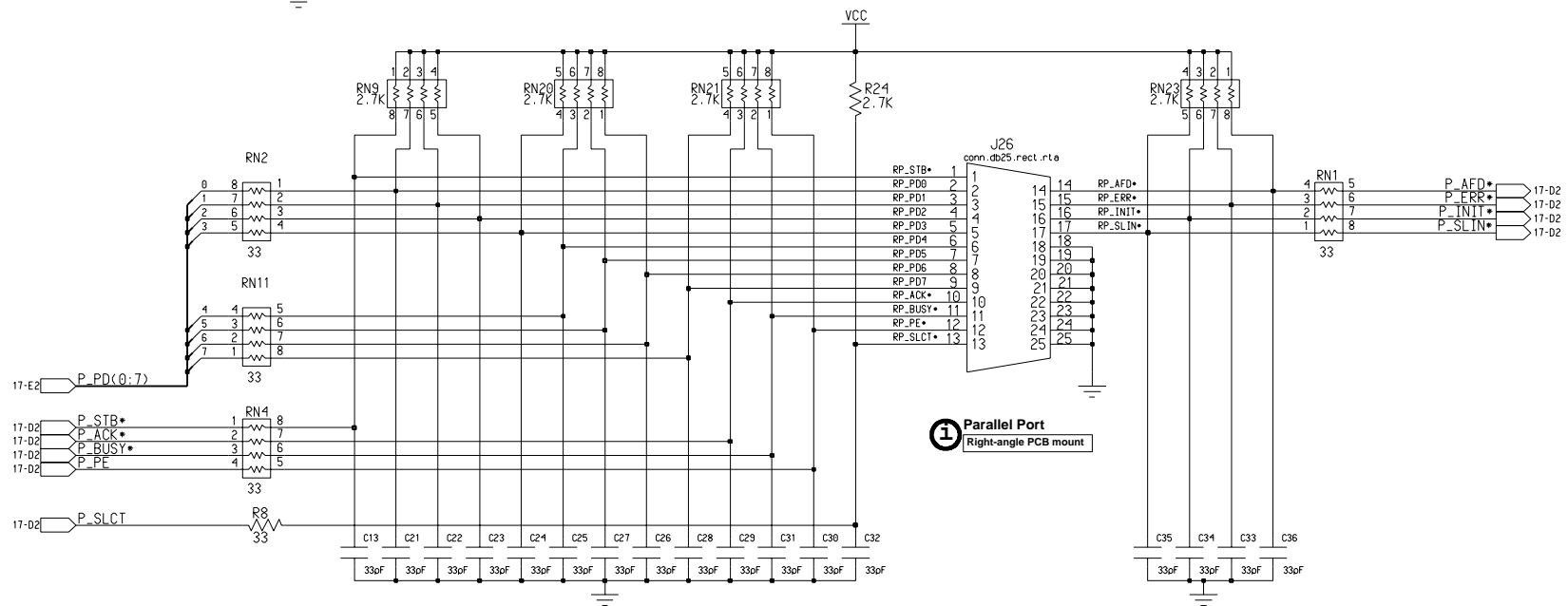
① PS/2 Keyboard

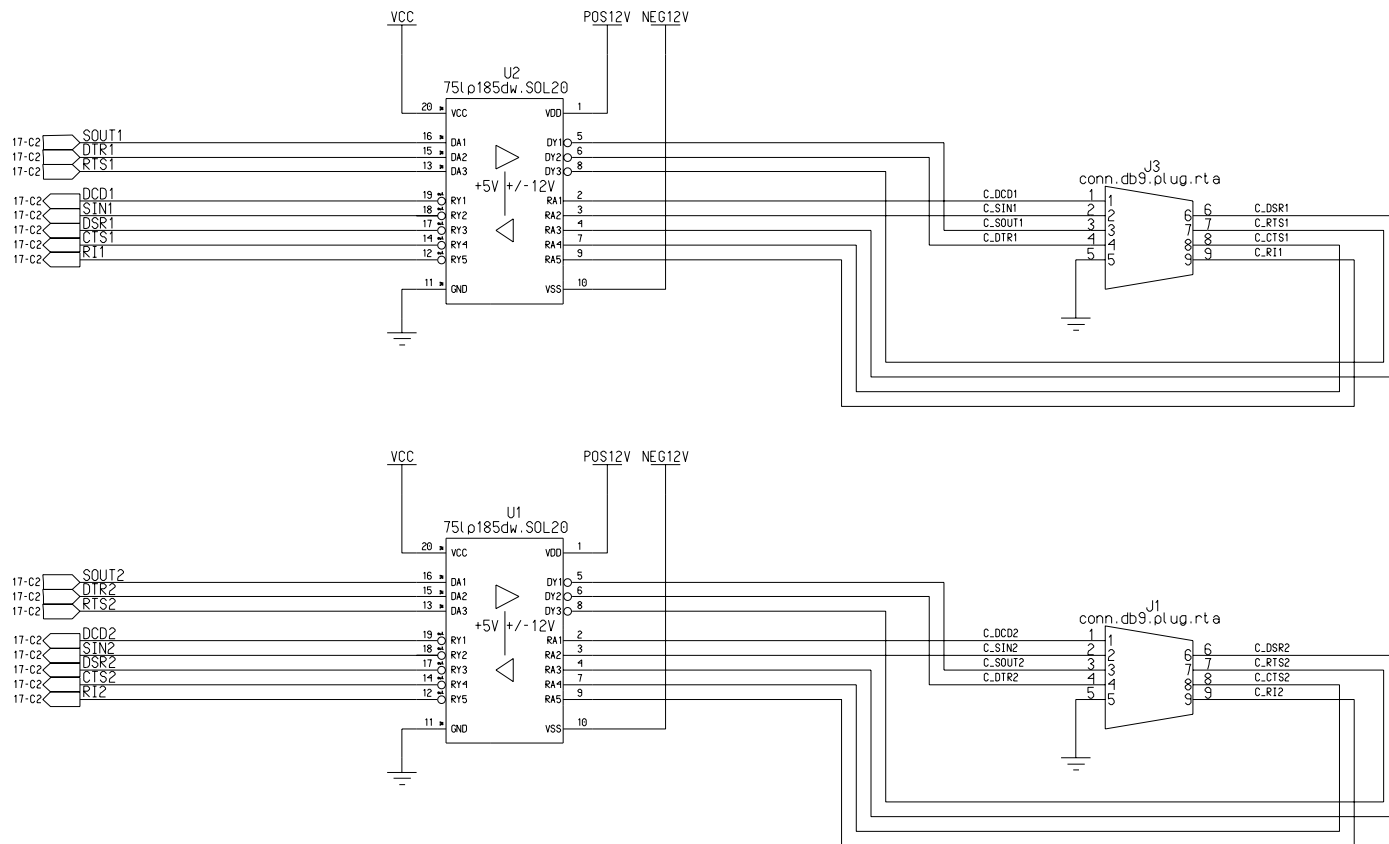
① PS/2 Mouse



① Floppy connector
CHRP-enhanced Auto-Eject

① Parallel Port
Right-angle PCB mount

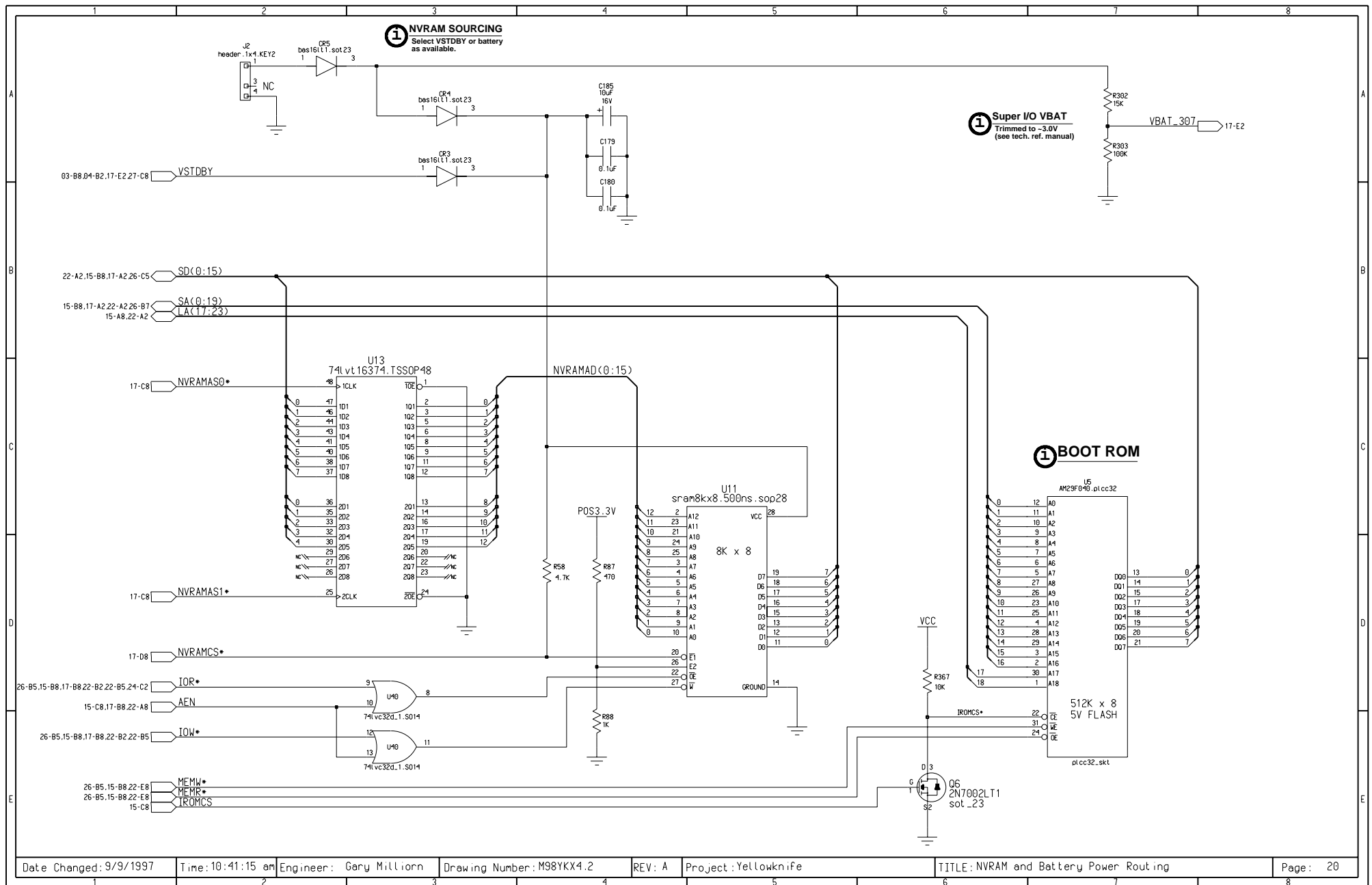


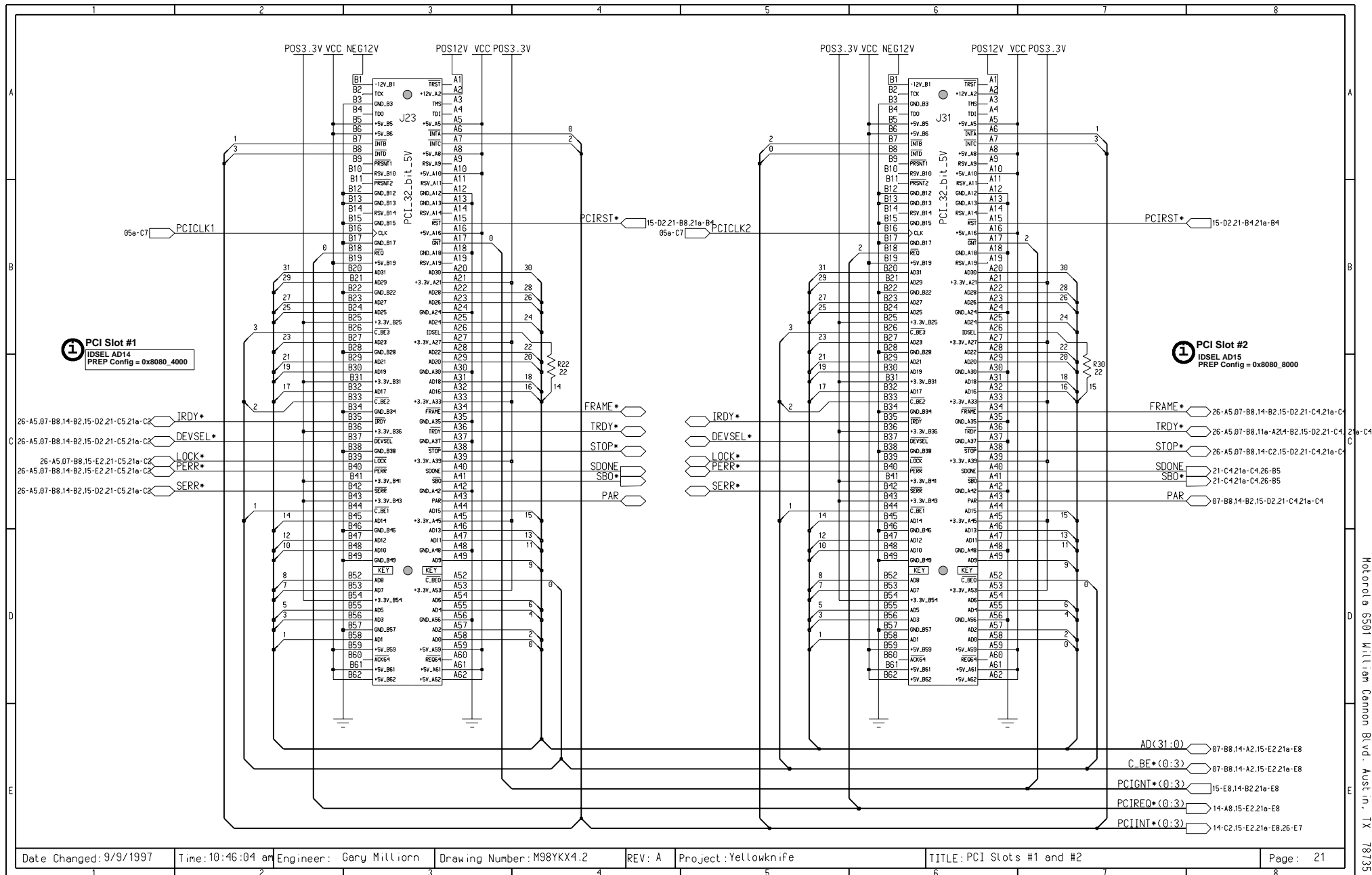


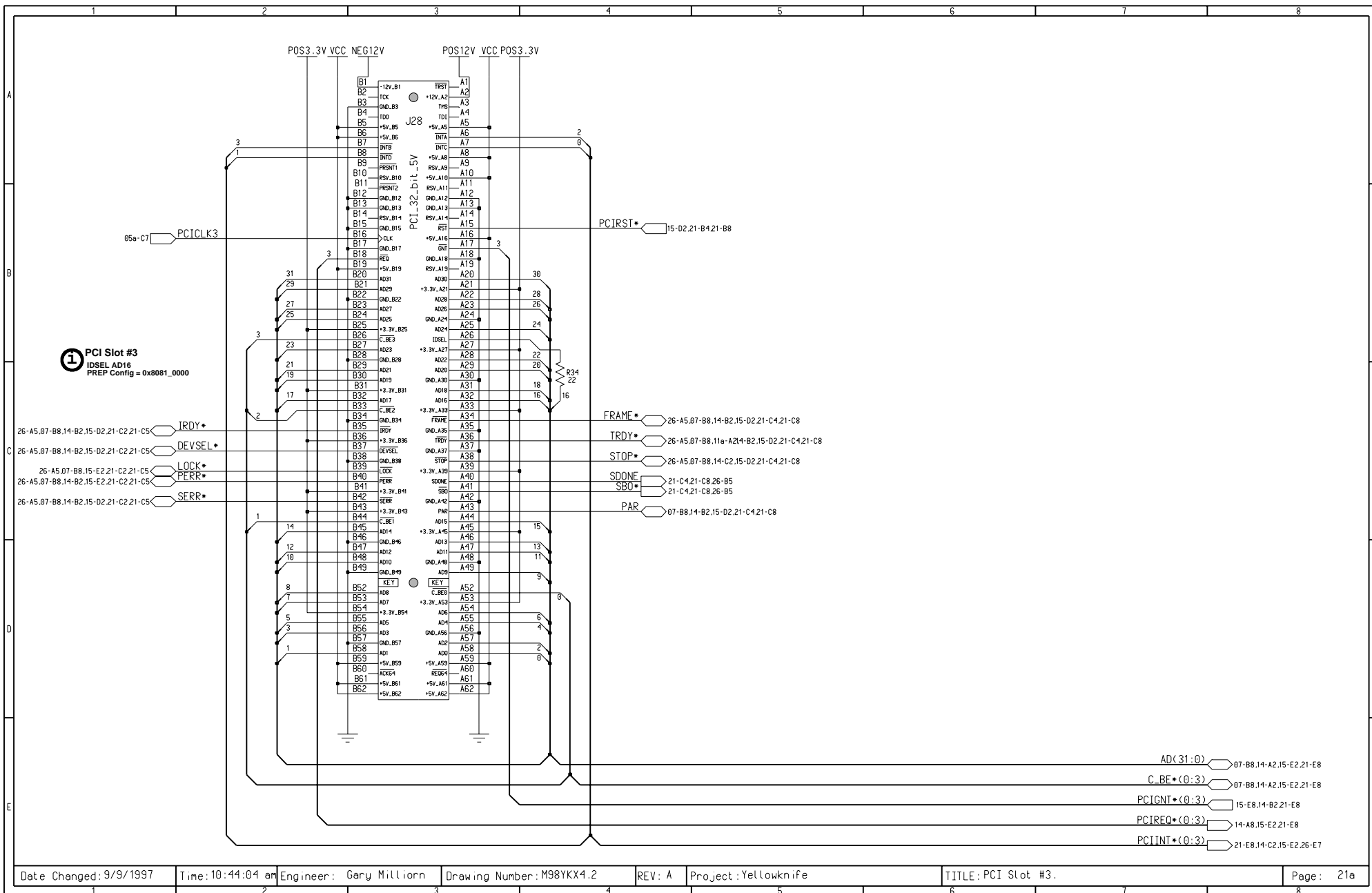
1 Serial Port #1

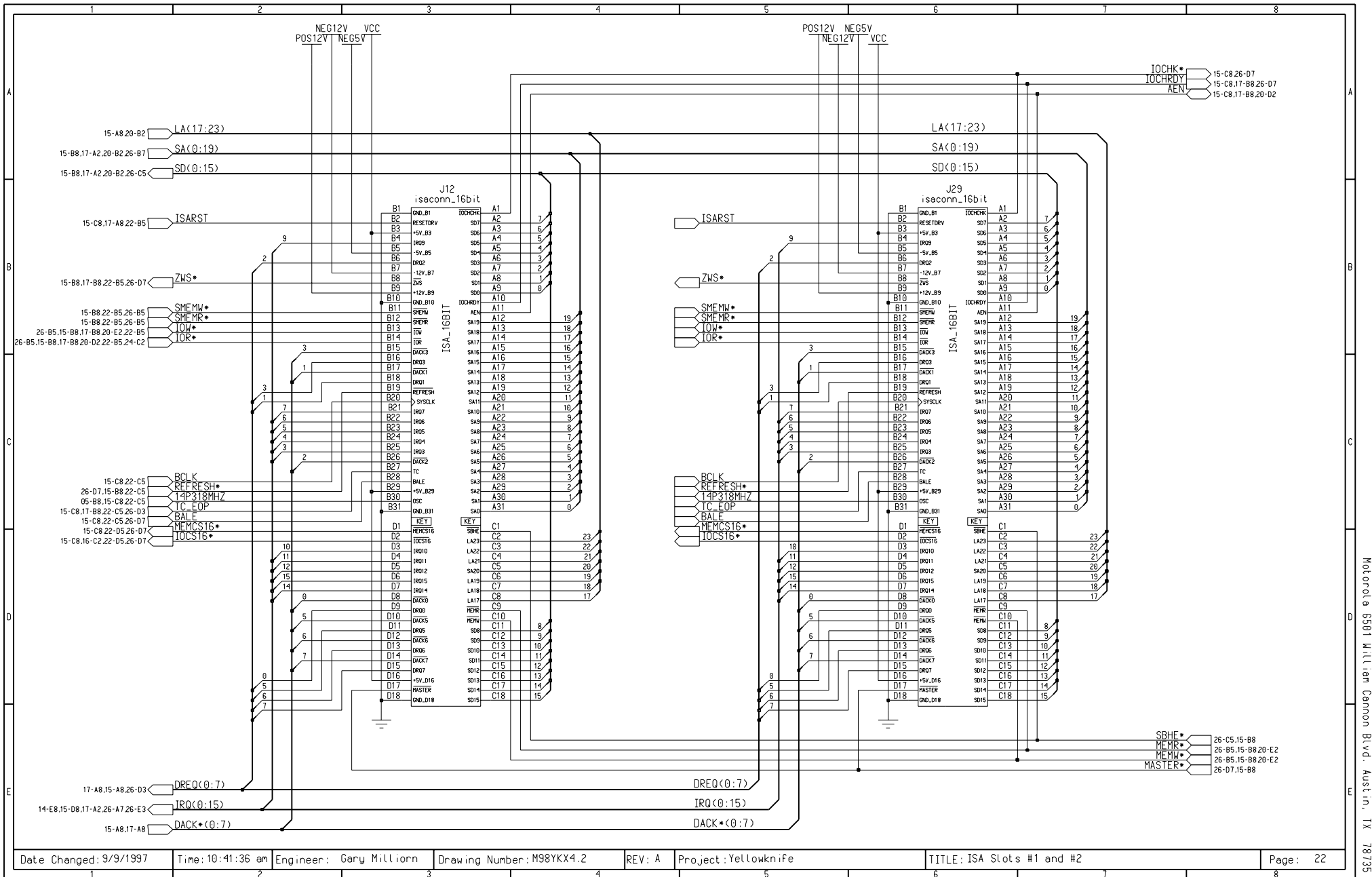
1 Serial Port #2

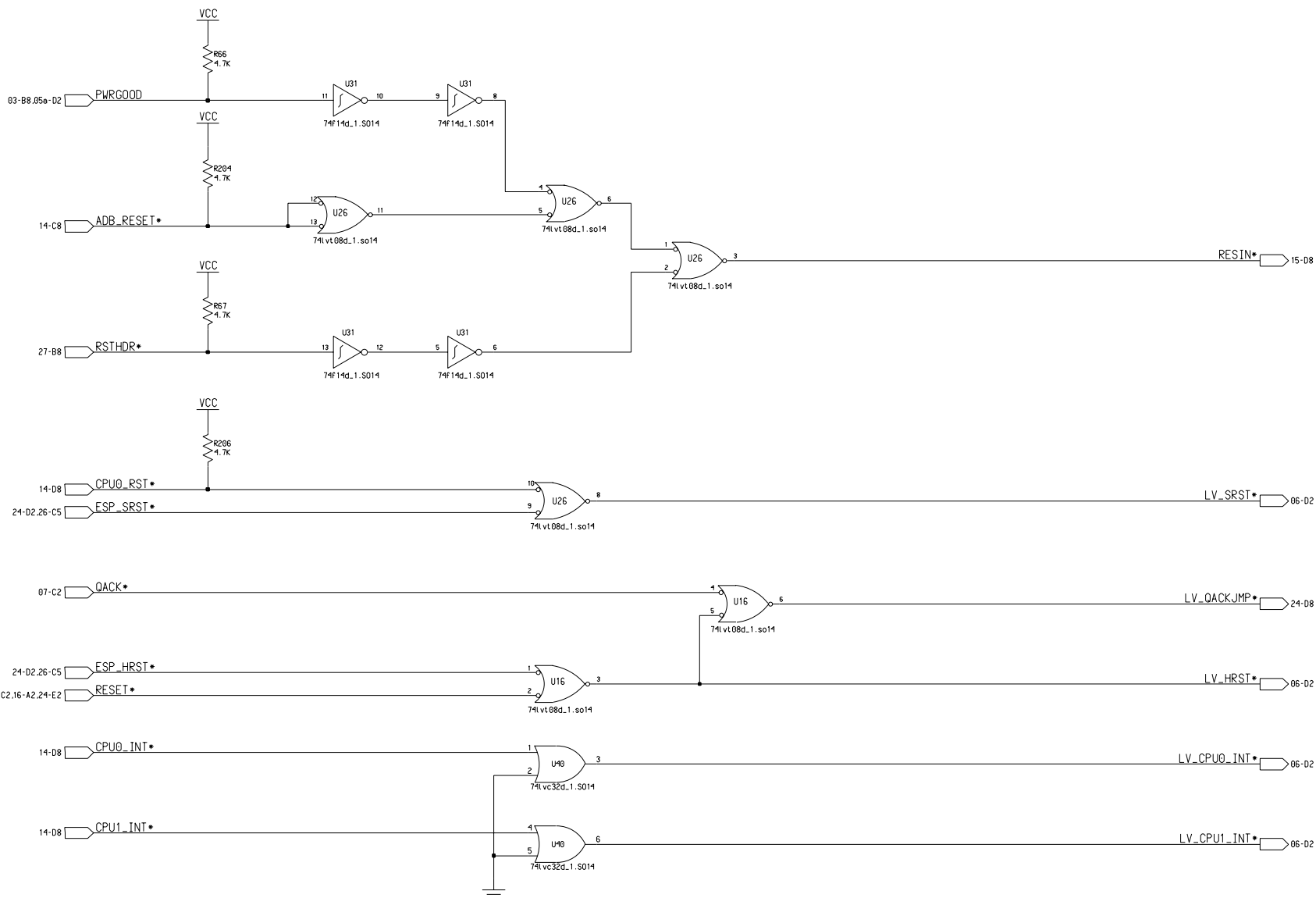
	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E

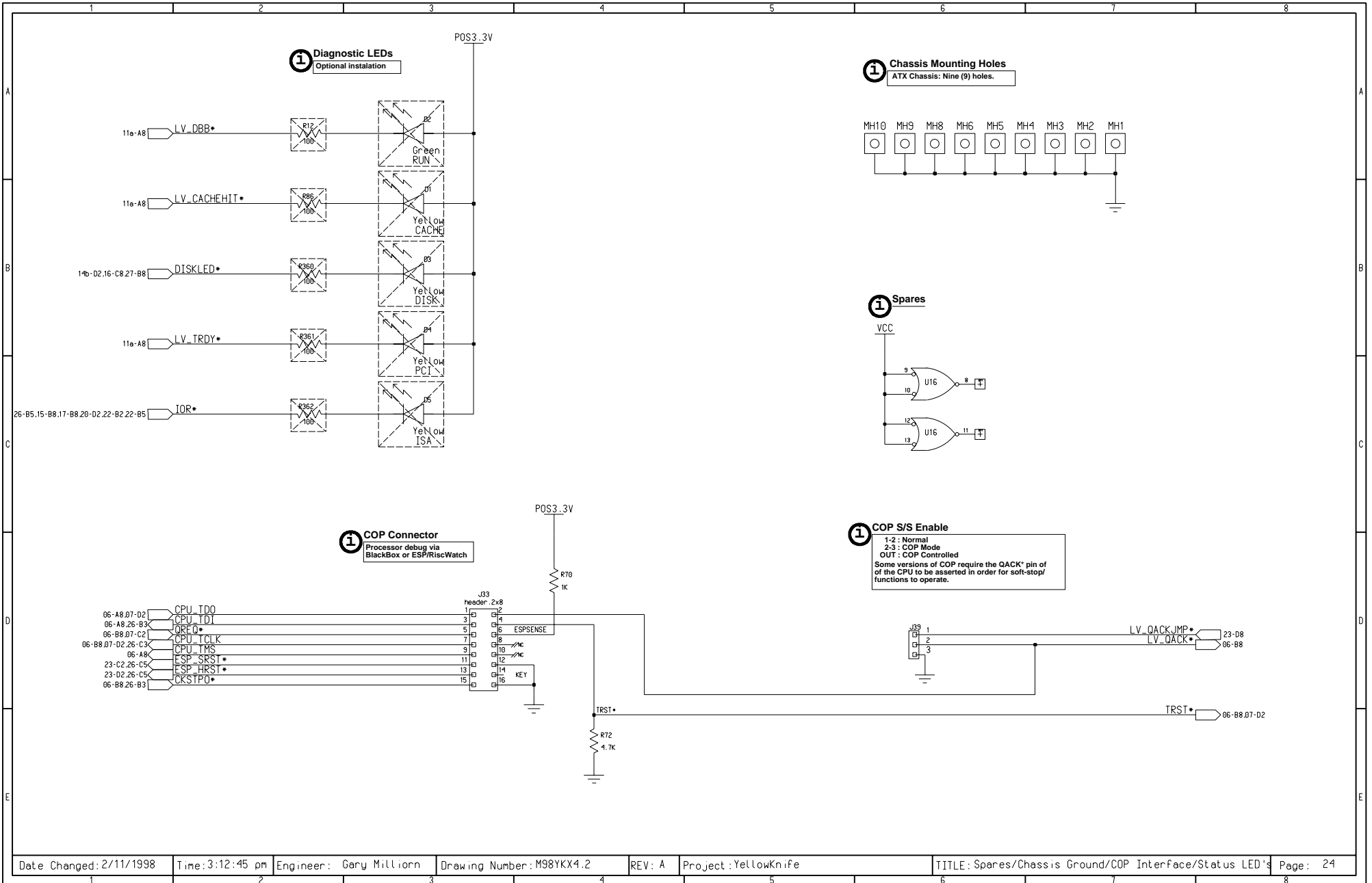


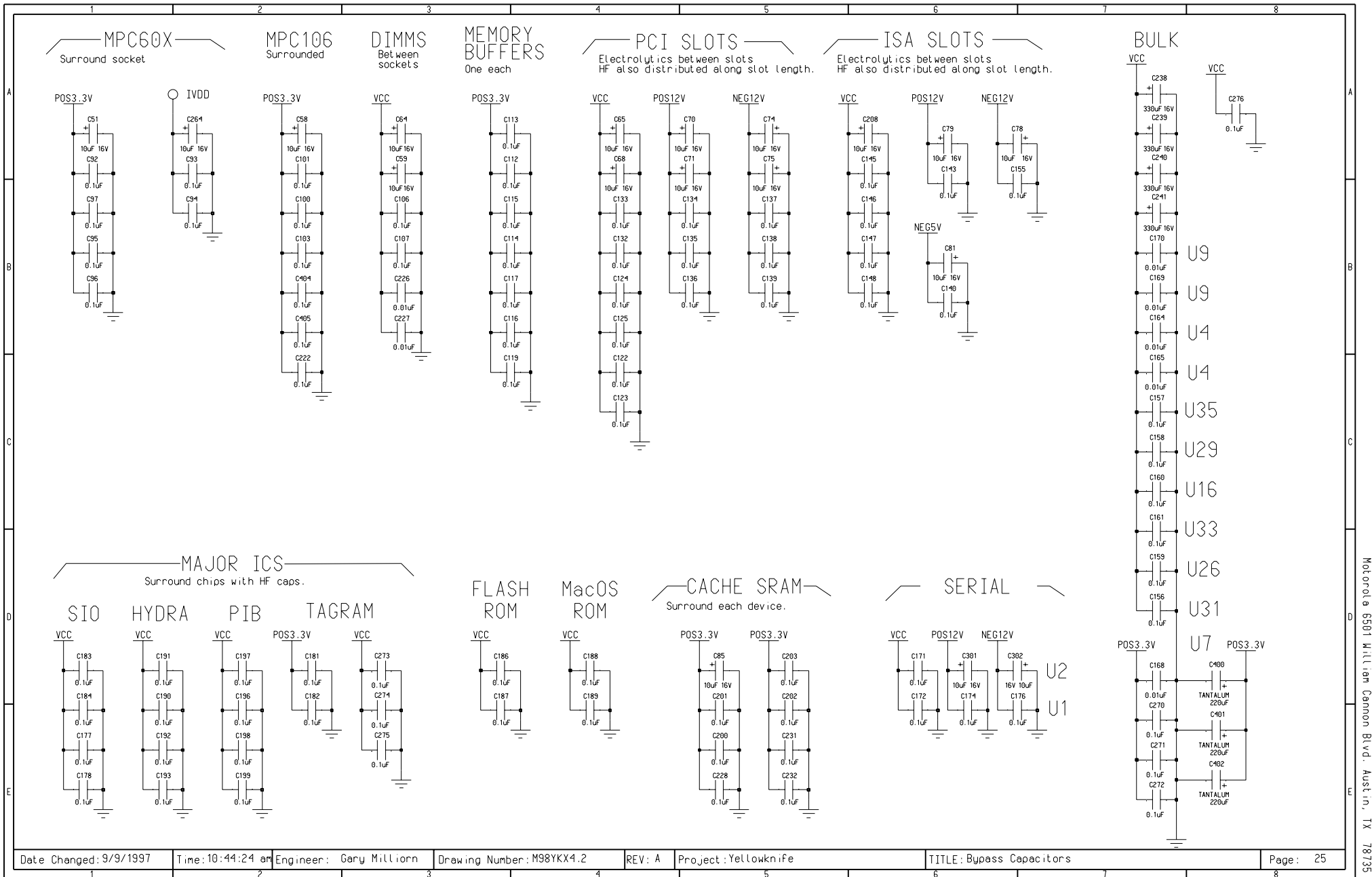


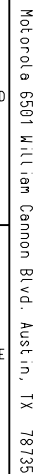


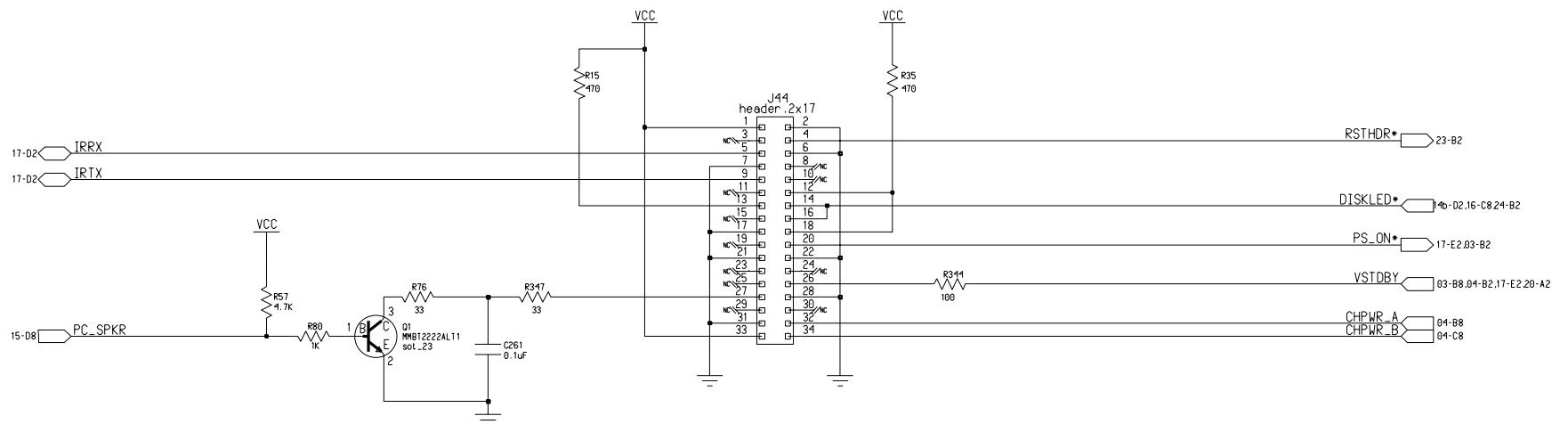






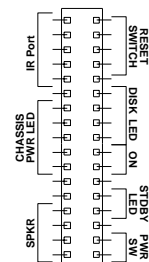






1 CHASSIS HEADER BLOCK

Label pin groups as shown.
Maintain clearance around connector
for silkscreen labels.



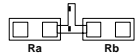
Sheet Routing Instructions

- 02a Avoid routing traces, especially noisy ones, across CPUPLL and 106PLL busses.
Keep CPUPLL, 106PLL and FREQ jumpers grouped in order shown. Leave area for silkscreen legends.
- 03 Use split power plane to connect IVDD from VRM module to CPU core.
Insert tantalum bypass capacitors between VRM and Socket7.
Keep optional VRM "cut-jumpers" grouped in order shown.
Keep fan power header within 6" of socket 7 lift-arm.
Use 30 mil trace for fan power.

04 No special restrictions.

05 Keep series termination resistors near the output pins.
EMI filtering caps may be placed anywhere along trace.

05a Keep series termination resistors near the output pins.
Connect dual (split) series termination using as shown, do not use a daisy-chain:



Route all clock traces from the MPC972 to equal trace lengths with the following allowances

Trace	PCI Slot Delta	Socket Delta	MPC106 PCI Hold Errata Delta	Time Of Flight Delta	Total Delta
PCICLK(1:3)	0"	0"	0"	0"	0"
HYDRACLK	2.5"	0"	0"	0"	2.5"
BRIDGE_CLK	2.5"	0"	0"	0"	2.5"
MPC106CLK	2.5"	0"	6"	0"	8.5"
MBCLK(1:2)	2.5"	0"	6"	0"	8.5"
SDCLK(1:4)	2.5"	-2.5"	6"	16"	22"
CPUCCLK	2.5"	-1.0"	6"	0"	7.5"
MPCLK	2.5"	-1.0"	6"	0"	7.5"
CACHECLK(0:1)	2.5"	-2.5"	6"	0"	6.0"
TAGCLK	2.5"	0"	6"	0"	8.5"

NOTE!

These trace lengths are optimized for a 100 MHz system bus. Refer to application note AN1722 for details and for different options for faster or slower buses.

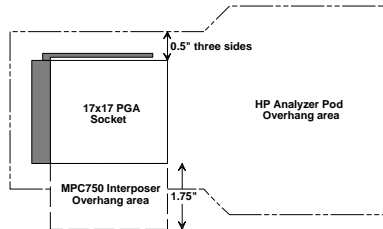
EMI filtering caps may be placed anywhere along trace.

Use heavy traces for power path through filter:

+3.3V => VCCO pins & Rxxx/Rxxx Combo => VCCI Pin.

Surround MPC972 with 4-6 0.1uF caps to provide good ground-return paths.

06 Keep series termination resistors near the output pins.
Keep AVDD filtering near AVDD pin. Use short traces and multiple vias to make good attachments to IVDD.
CPU+Cache Interposers (such as the MPC750) overhang the socket outline. Avoid high-profile component placement in the following area:



Route PID(0:2) traces on outer layers for Doubletake support.

Surround socket with 6 (six) 0.1uF caps to provide additional ground-return paths. Use two ground-attach vias.
Place bulk capacitance near socket for IVDD and +3.3V ground planes.

07 Keep AVDD filtering near AVDD pin. Use short traces and multiple vias to make good attachments to +3.3V.
Surround MPC106 with 6 (six) 0.1uF caps to provide good ground-return paths. Use two ground-attach vias.
Place bulk capacitance near socket for +3.3V ground plane.

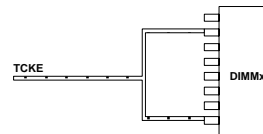
08 Place TAGRAM so that HIT, TV and DI/DO are minimized.

Sheet Routing Instructions

- 09 Route databus to cache SRAM using split-Y traces of equal length.
- 10 Place series termination resistors very near source (MPC106), < 1".
Route terminated traces using equal trace lengths towards SDRAM array.

11/11a Place 0.1uF cap near each buffer adjacent to a ground pin. Use two ground-attach vias.

12/12a Use split-Y connections between MPC106 (or series termination resistors) and the following signals:
TMA(0:12) TSDCAS*
TSDMA1 TMWE
TDQM_CAS(0:7) SDCLK(1:4) (all pins separately)
TCS_RAS(0:7) TCKE*
TSDRAS*



Connect data bus and parity in daisy-chain manner.

13 Connect +12V using 30mil power trace.

14 Place SCSI filters (on nets SCSI_RC_ACK* etc.) near Hydra chip.
Place IDSEL resistor near IDSEL pin.

14a Placement may vary; restrictions apply if using the Motorola Apple I/O card.
Place AIO between ISA and PCI slots.
Keep SCSI termination (MCCS142236) near Hydra.
Use short trace from SCSI_BSY* pin on connector to diode tap (CR10).
Use multiple vias to attach power to polyswitch Fx.
Use 30 mil traces from polyswitch to SCSI connector and to TERMPWR pin and capacitor.

15 Use equal-length traces on nets DAK(2:0) from WinBond to 'F138.

16 Place series termination resistors near socket.

17 Use very short traces from 32kHz crystal to SuperI/O and to connected components.
Allow no other traces to enter or cross the crystal oscillator area.
Use 12 mil traces for VBAT and VSTDBY.

18 Place EMI filtering caps and ferrite beads very close to DIN6 and DB25 connectors.
Place series resistors for parallel port near DB25 connector.

19 Keep traces very short between RS232 drivers (U1, U2) and DB9 connectors.
Use 12 mil traces for +12V and -12V.

19a Consult hardware specification for details on this complicated routing procedure.

20 Use 12 mil traces between battery connector and diodes (before and after).

21,21a Place IDSEL resistor near IDSEL pin.

22 No special restrictions.

23 No special restrictions.

24 Recommended placement for status LEDs is under the disk tray area.
Follow ATX chassis specifications for ATX mounting hole sizes and plated area allowance.
The COP connector may be placed wherever is convenient.

25 Distribute capacitors as shown, unless otherwise specified.

26 Keep traces as short as possible. Pin swapping within and without of a package is encouraged in order to minimize trace length.

27 Place header in lower-left hand corner of the board (I/O connectors would be in the upper right).
Allow clearance around header to allow for silkscreen legends.