
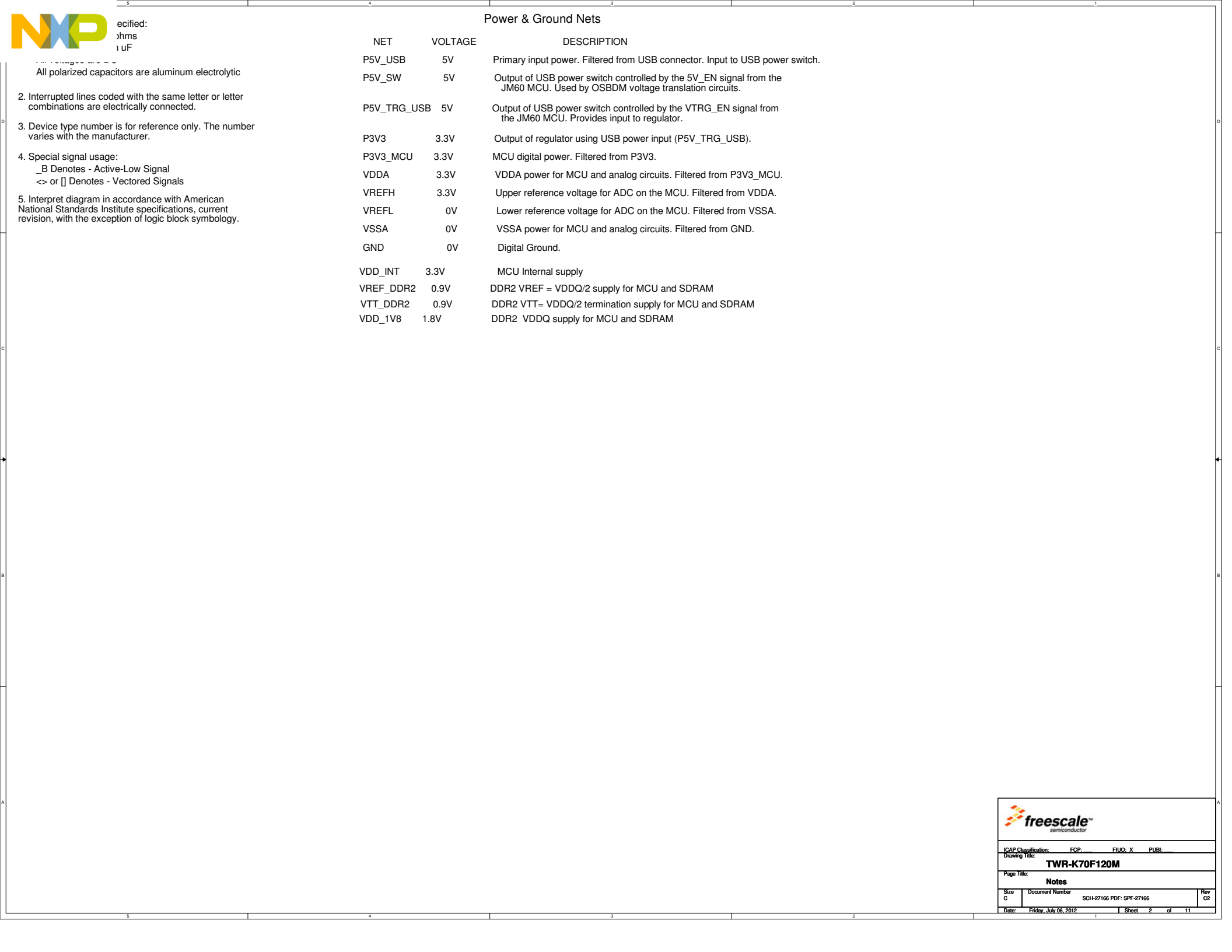


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5	K70N1M MCU-2
6	USB/OSBDM/VTRAN/PWR
7	PERIPHERALS
8	ELEVATOR CONNECTORS
9	SENSORS
10	DDR2 SDRAM, NAND FLASH
11	DDR POWER & TERMINATIONS

Revisions			
Rev	Description	Date	Approved
A	Prototype release	22 Jul 11	TTC
B	A085 Release	27 Oct 11	Peter
B1	A085 Release - MCU Marketing part number updated as per MCO30515	3 Nov 11	Peter
C	A085 Release	8 Feb 12	Peter, Kevin
C1	- Replaced obsolete resistor 470-80310 with 470-75416 - Changed R326 to DNP	2 Jul 12	Peter, Kevin
C2	- Changed R31, R32, R35, and R71 to DNP	6 Jul 12	Peter, Kevin

		Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78752-8689	
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Designer: ionDSN		ICAP Classification: FOP: FUC: X PUB:	
Drawing Title: TWR-K70F120M			
Drawn by: ionDSN		Page Title: Table of Contents/Revisions	
Approved: Peter/Kevin		Size C	Document Number SCH-27166 PDF: SPF-27166
Date: Friday, July 06, 2012		Sheet 1 of 11	Rev C2



Power & Ground Nets

NET	VOLTAGE	DESCRIPTION
P5V_USB	5V	Primary input power. Filtered from USB connector. Input to USB power switch.
P5V_SW	5V	Output of USB power switch controlled by the 5V_EN signal from the JM60 MCU. Used by OSBDM voltage translation circuits.
P5V_TRG_USB	5V	Output of USB power switch controlled by the VTRG_EN signal from the JM60 MCU. Provides input to regulator.
P3V3	3.3V	Output of regulator using USB power input (P5V_TRG_USB).
P3V3_MCU	3.3V	MCU digital power. Filtered from P3V3.
VDDA	3.3V	VDDA power for MCU and analog circuits. Filtered from P3V3_MCU.
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital Ground.
VDD_INT	3.3V	MCU Internal supply
VREF_DDR2	0.9V	DDR2 VREF = VDDQ/2 supply for MCU and SDRAM
VTT_DDR2	0.9V	DDR2 VTT= VDDQ/2 termination supply for MCU and SDRAM
VDD_1V8	1.8V	DDR2 VDDQ supply for MCU and SDRAM

- Specified:
 100nms
 1 uF
- All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
 - Device type number is for reference only. The number varies with the manufacturer.
 - Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
 - Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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ICAP Classification: FCP: FIUC: X PUBI:

Drawing Title: **TWR-K70F120M**

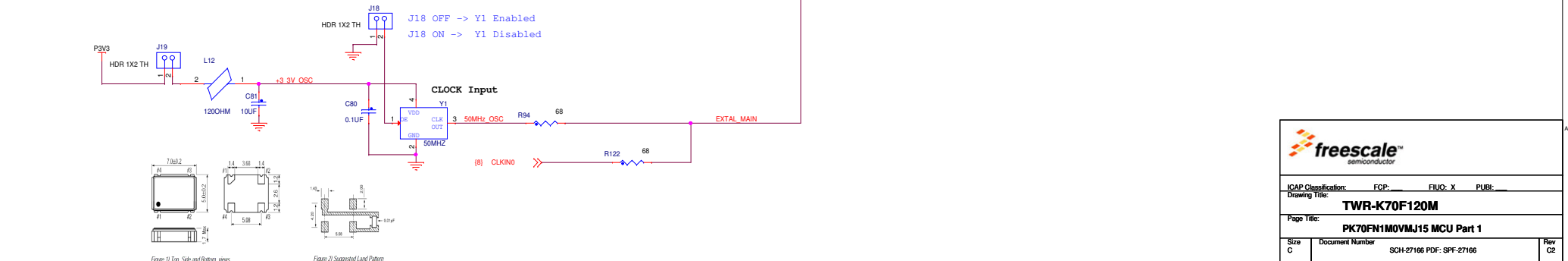
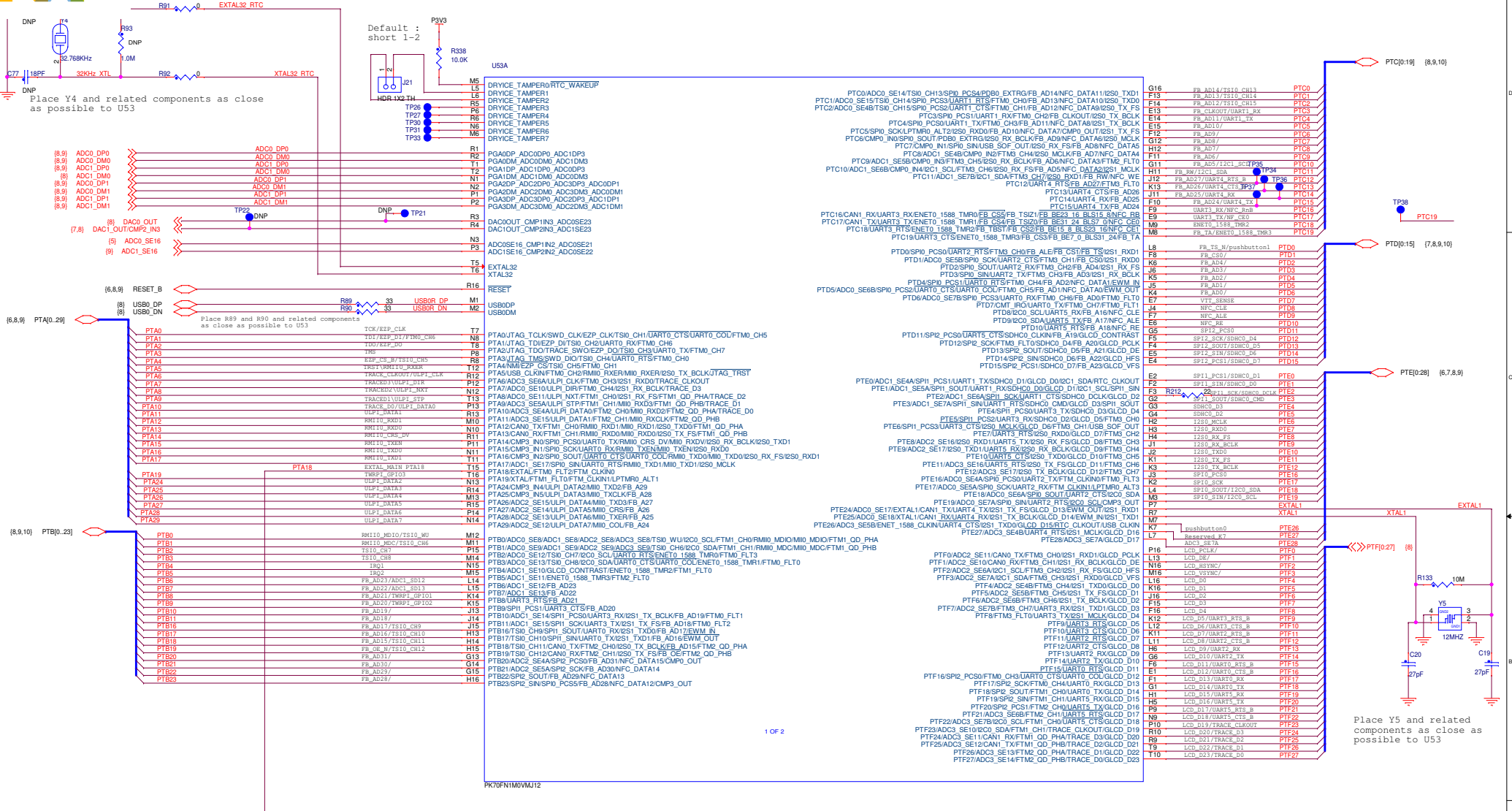
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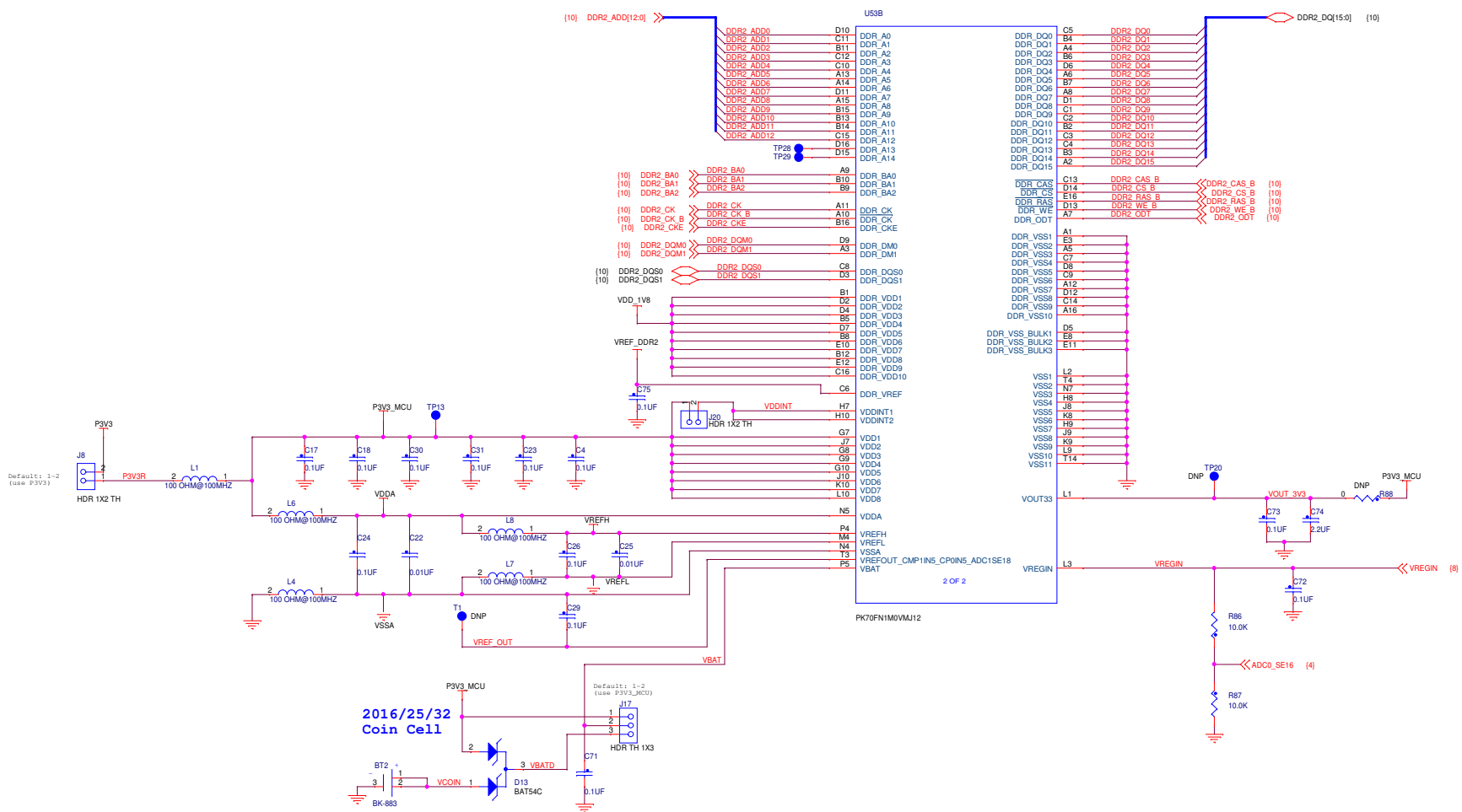
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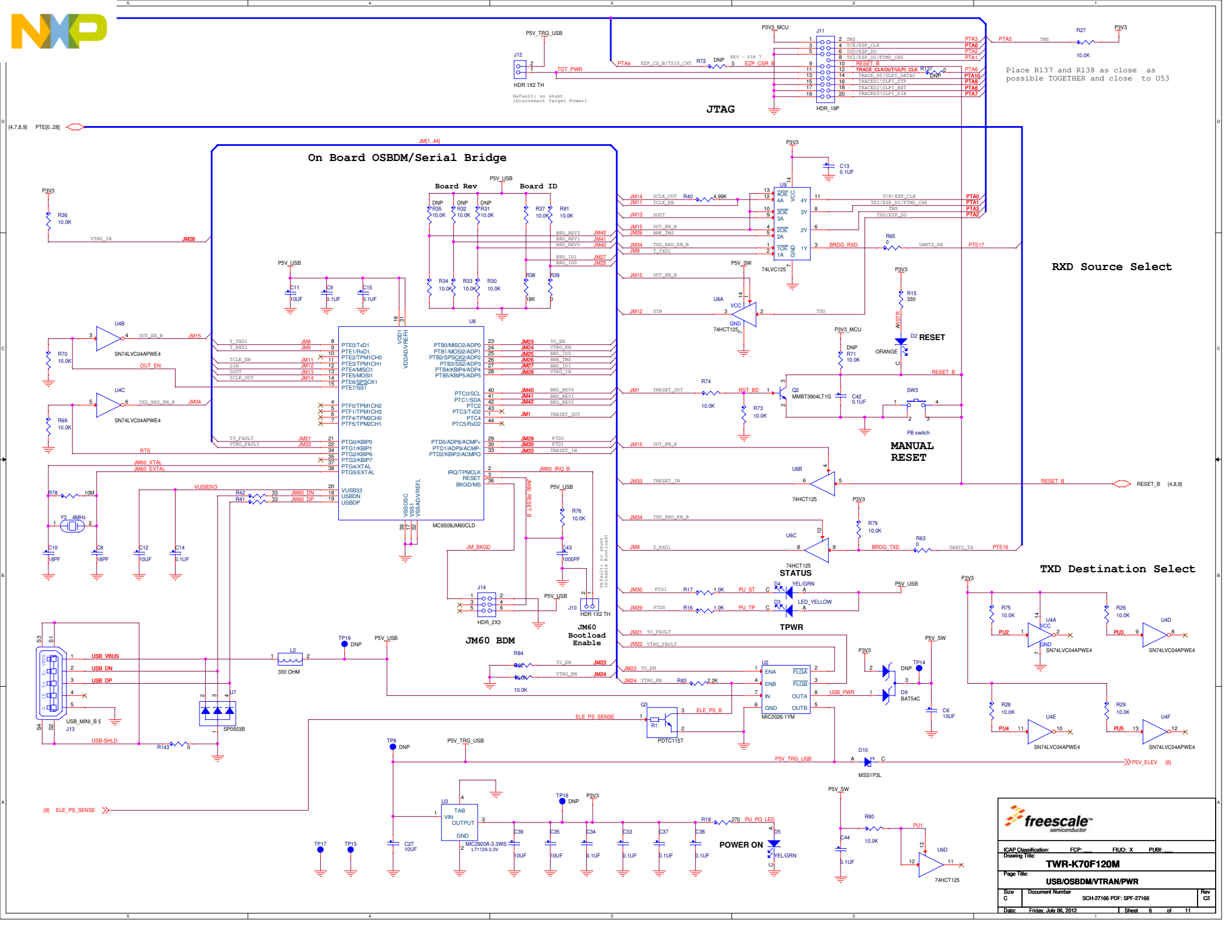
Date: Friday, July 06, 2012 Sheet 2 of 11



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Drawing Title: TWR-K70F120M		
Page Title: Reserved		
Size C	Document Number SCH-27166 PDF: SPF-27166	Rev C2
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Place R137 and R138 as close as possible TOGETHER and close to U53

RXD Source Select

TXD Destination Select

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ICAP Classification: FCP: FIUC: X PUBL:

Drawing Title: **TWR-K70F120M**

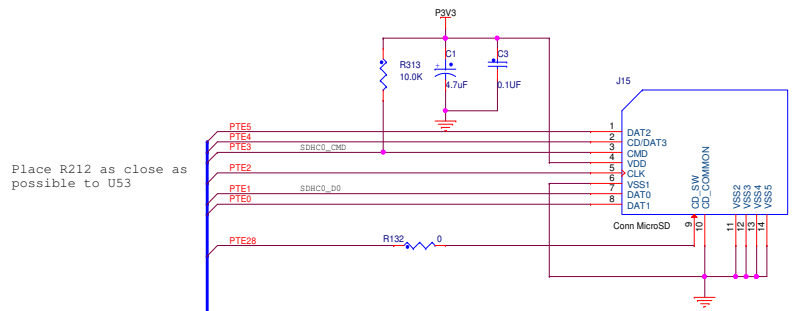
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Size C Document Number SCH-27166 PDF: SPF-27166 Rev C2

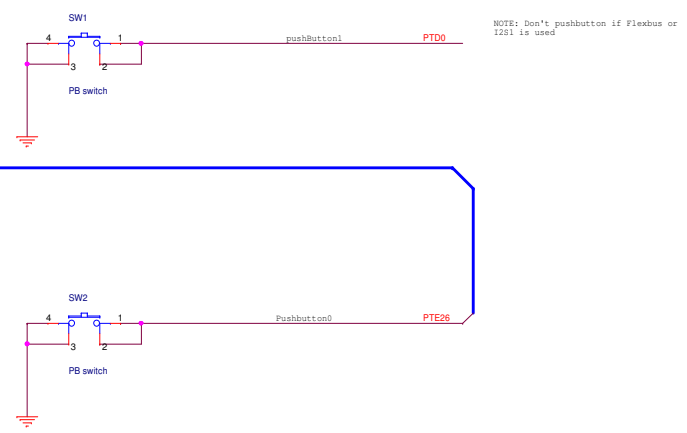
Date: Friday, July 06, 2012 Sheet 6 of 11



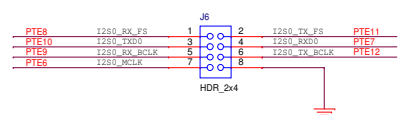
MICRO SD INTERFACE



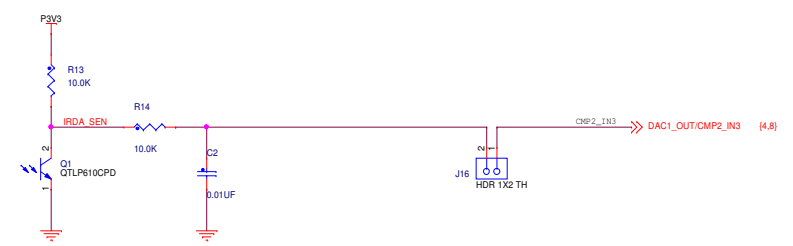
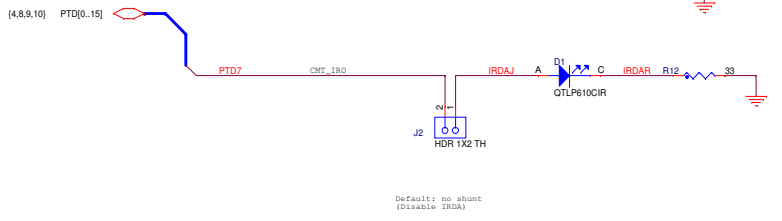
PUSH BUTTON



I2S SAI HEADER



IRDA

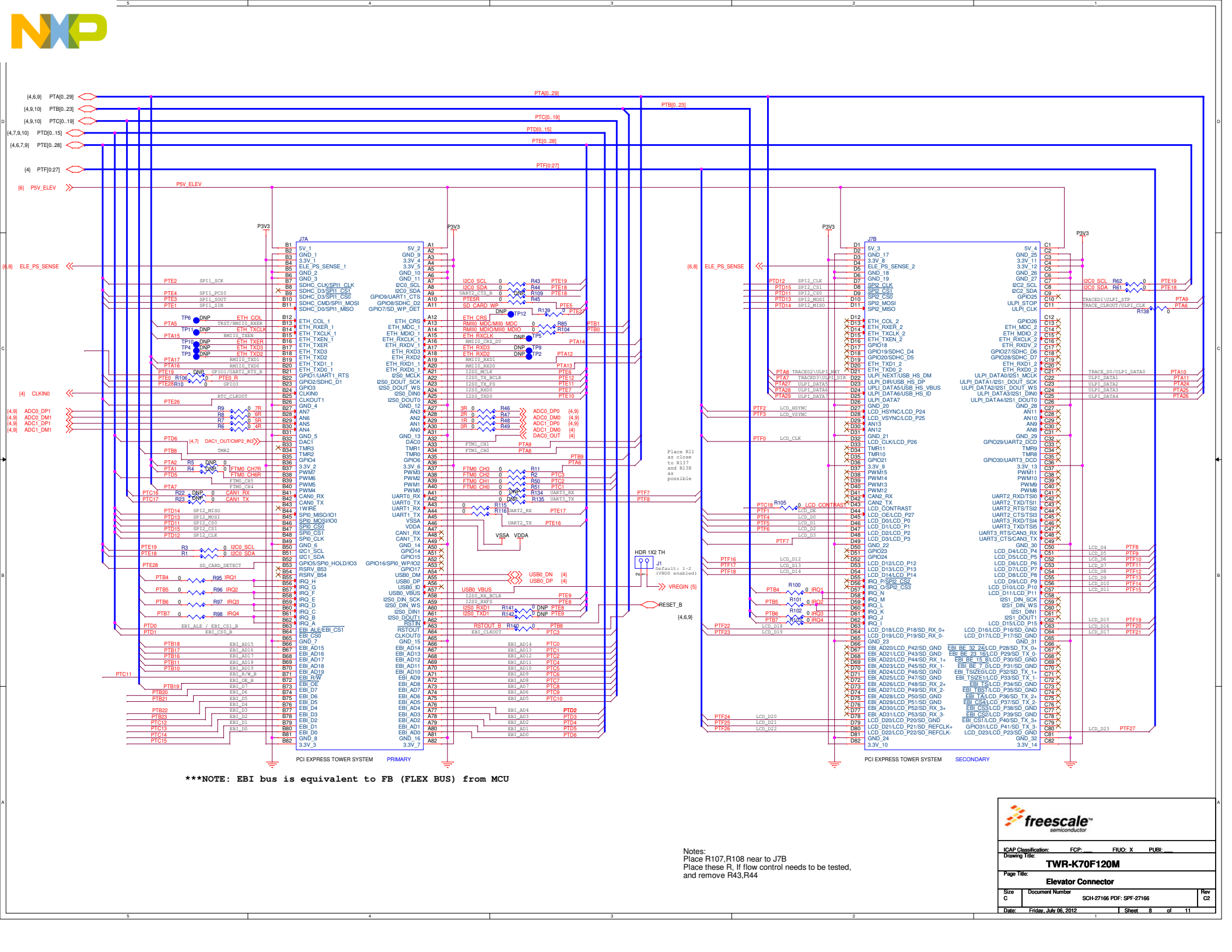


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ICAP Classification: FCP: FIUC: X PUBL: _____
Drawing Title: **TWR-K70F120M**

Page Title: **Peripherals**

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***NOTE: EB1 bus is equivalent to FB (FLEX BUS) from MCU

Notes:
Place R107,R108 near to J7B
Place these R. If flow control needs to be tested,
and remove R43,R44



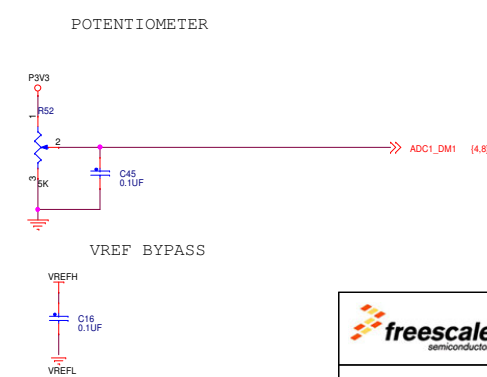
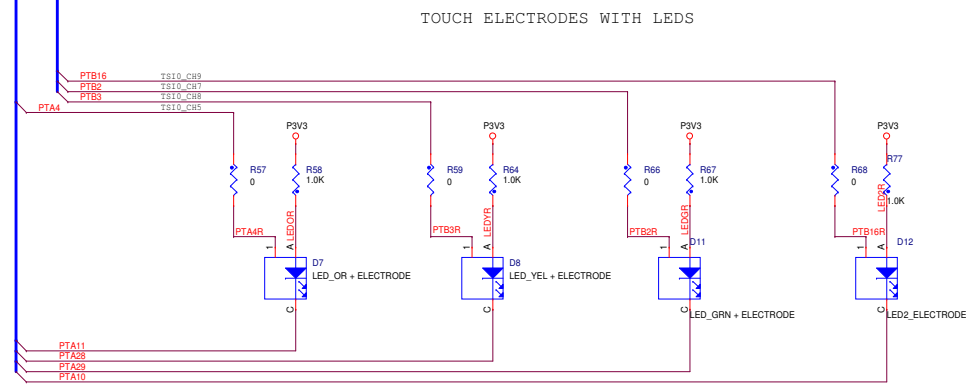
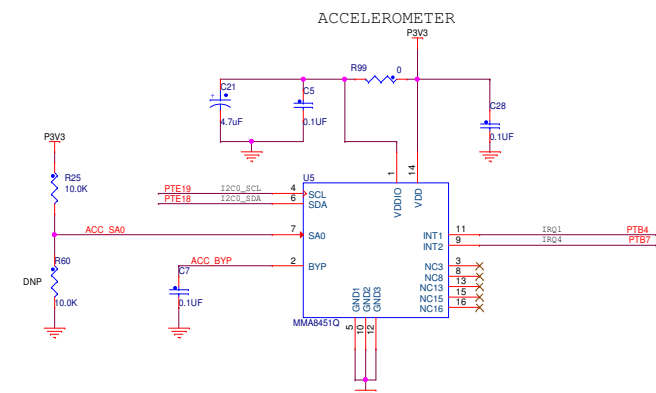
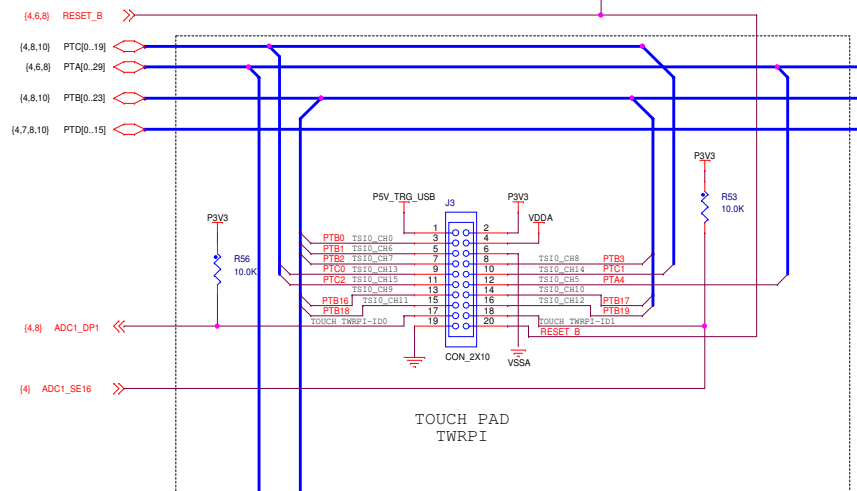
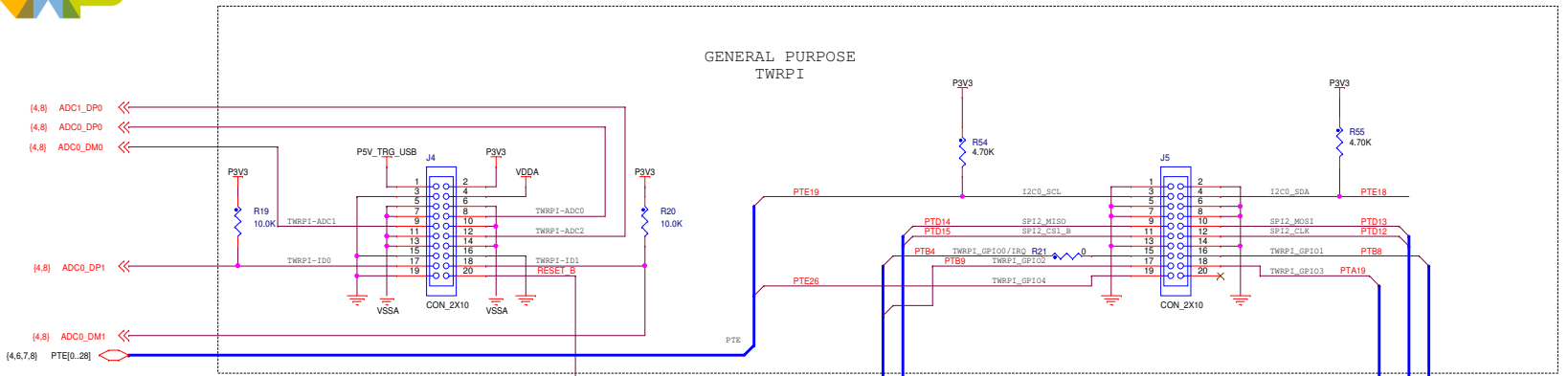
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Page Title: Elevator Connector

Size C Document Number SCH-27166 PDF: SPF-27166

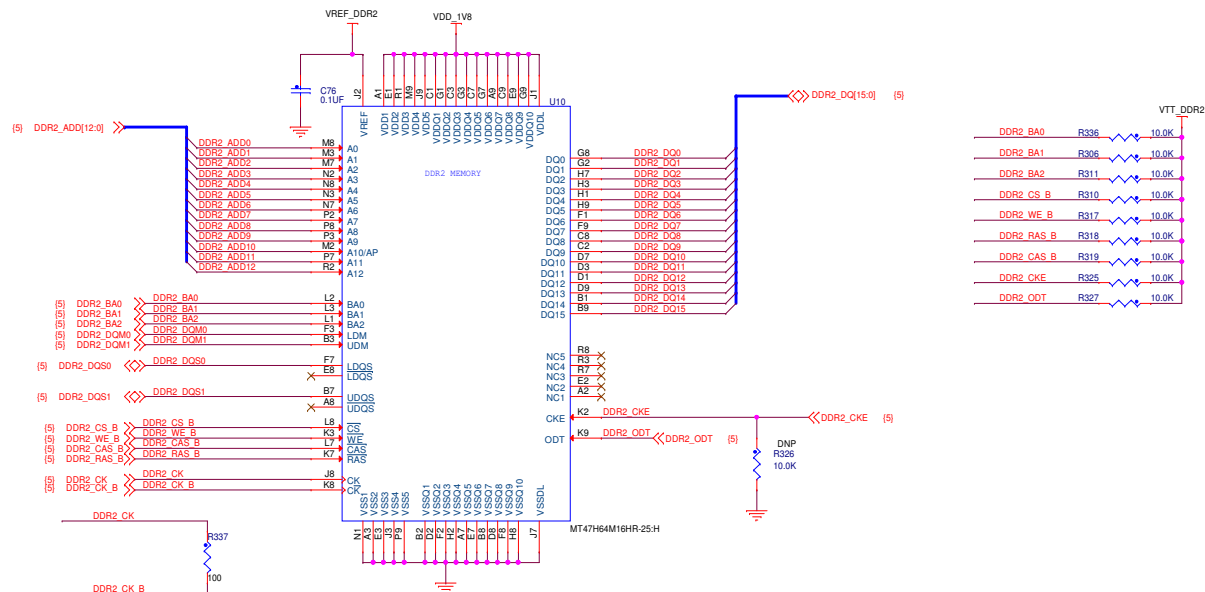
Date: Friday, July 06, 2012 Sheet 8 of 11



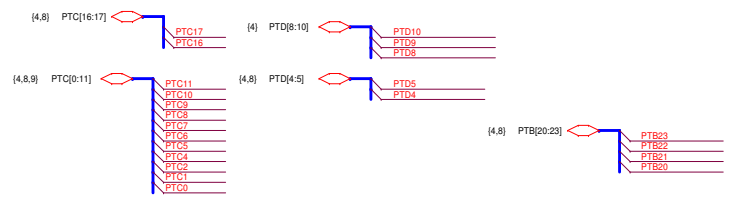
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 Page Title: **Sensors**
 Size C Document Number SCH-27166 PDF: SPF-27166 Rev C2
 Date: Friday, July 06, 2012 Sheet 9 of 11



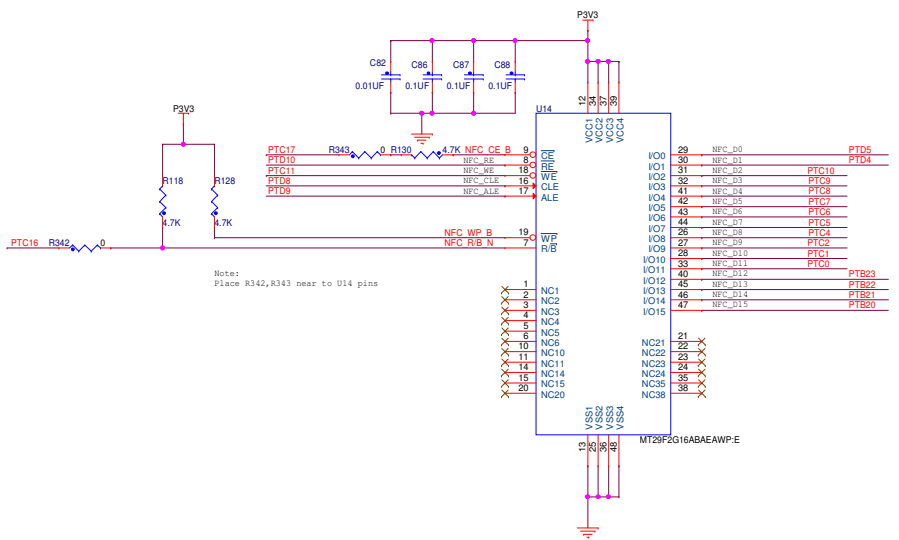
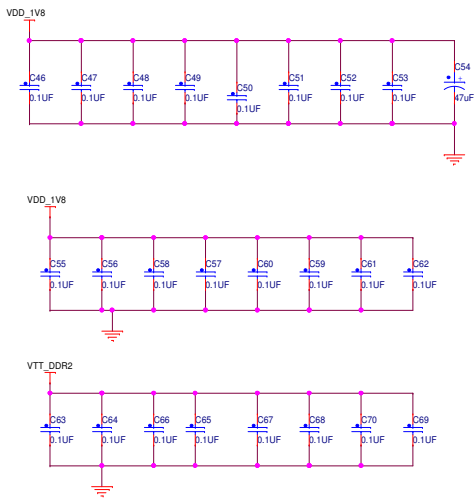
DDR-2 MEMORIES AND TERMINATIONS



Note:
Place the DDR2 CLK Termination resistor R337 close the Chips



NAND FLASH



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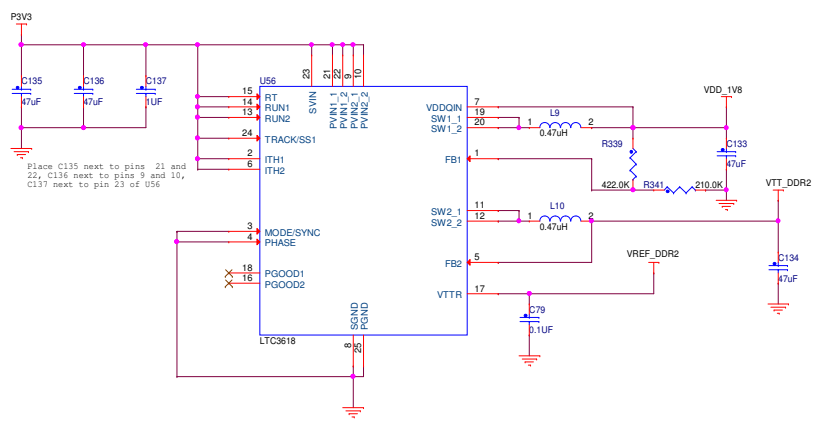
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Drawing Title: **TWR-K70F120M**

Page Title: **DDR2 SDRAM, NAND FLASH**

Size C	Document Number SCH-27166 PDF: SPF-27166	Rev C2
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Date: Friday, July 06, 2012 Sheet 10 of 11

DDR-2 TERMINATION REG (3A)





TWR-K70FN1M Tower Module

Schematic Executive Summary

Rev. 0.2



Revision History

Revision	Author	Date	Changes
0.1	MH	06/28/2013	Preliminary version
0.2	MH	07/19/2013	First release

1 Purpose

The purpose of this document is to provide a written overview of the TWR-K70F120M board. The schematic source, BOM, layout, and other design files are all available for download from the Freescale website (TWR-K70F120M-PWB). The schematics and board design package are useful for reference, but notes embedded in the schematic are not sufficient to document important items and explain design decisions.

This document will walk through the schematic for the TWR-K70F120M rev C2 board page by page providing explanation for connections on the board and pointing out design rules and tips.

1 Abbreviations

This summary will refer to components using the reference designators in the schematics. The beginning letters or letters identify the type of components as follows:

C = Capacitor	ex: C1
D = LED	ex: D1
J = Connector (male)	ex: J1
P = Plug (female)	ex: P1
R = Resistor	ex: R1
T = Transformer	ex: T1
U = Device	ex: U1
Y = Crystal	ex: Y1
RP = Resistor pack	ex: RP1
SW = Switch	ex: SW1
TP = Test point	ex: TP1

DNP = Do not populate. There is a footprint present on the board for the component, but it is not installed on the board.

2 Schematic Page 1 – Table of Contents and Revision History

3 Schematic Page 2 - Notes

In addition to some notes on units and signal nomenclature, this page provides a list of the power and ground nets used in the design. This includes the nominal voltage for each rail and a brief description of the usage.

4 Schematic Page 3 - Unused

5 Schematic Page 4 – K70 Processor (Non-DDR signals)

This page is the first part of the symbol for the K70 processor. In general most of the signals are routed to buses or other off page connectors so that the signal names can be references for making connections to circuitry on other pages of the schematic.

5.1 Clocks

There are three clock inputs available on the K70 processor, all of which have circuitry on this page of the schematic.



TIP:

All signals on your board should be properly coupled to a plane with enough distance between traces to make sure the traces couple to planes instead of each other. This is particularly important for clock signals, so pay special attention to the layout of all clock traces.

5.1.1 EXTALO/EXTAL_MAIN

The circuit in the lower, left hand side of this page provides the primary clock input to the processor on the EXTALO pin (EXTAL_MAIN net). This board is designed to support an RMII Ethernet connection. In order to support RMII, the 50MHz clock used for the Ethernet PHY must also be routed to the processor on EXTALO. For the tower system, a TWR-SER or TWR-SER2 card configured for RMII operation would drive the 50 MHz PHY clock on the CLKIN0 net shown here. Because the tower needs to run in stand-alone mode (no other tower cards present), there is also an option to use an on-board 50 Mhz oscillator to provide the main input clock. Jumpers (J18 and J19) and/or 0 ohm resistor population options (R94 and R122) can be used to select between the two clock sources.

In order to support the flexibility of the tower system, the circuit here is more complicated than what would be used in a typical end system where the input clock would usually come from a single, fixed source.



TIP:

Keep in mind that if RMII is being used the EXTALO input must be 50 MHz and the clock trace length should be setup so that the clock reaches the Ethernet PHY and processor at the same time. Skew between the two clocks could result in timing violations on the RMII signals.

5.1.2 EXTAL1/XTAL1

The K70 supports a secondary high frequency clock input on the EXTAL1/XTAL1 pins. The *Kinetis Peripheral Module Quick Reference* document (KQRUG) available from the Freescale website, contains useful information and board layout guidelines for crystal circuits. Please refer to “Section 2.1.3.3 Oscillators” in the KQRUG for more information.



TIP:

OSC1 can be used as the reference clock source for one or both of the PLLs, but there are some restrictions on its use. The following items should be taken into account if you are considering using OSC1 as the main clock input on your board:

- Either OSC0 or OSC1 can be used as the reference clock source for the PLL being used as MCGCLKOUT.
- Only OSC0 or the RTC OSC can be used as the FLL reference clock so one of those clock sources MUST be available to the MCG if using FEE, FBE, or BLPE clock modes or when transitioning from the reset default FEI mode to PBE mode (or any “external” clocked MCG mode). You must transition through FBE mode to enter PEE mode and use the PLL as the MCGCLKOUT source.
- If OSC1 is to be used it must be configured in MCG_C10 and enabled in OSC1_CR.
- If OSC1 is the only external clock source then the only MCG clock modes available are FEI, FBI and BLPI.

5.1.3 EXTAL32/XTAL32

The final clock is the 32 kHz oscillator. This input is primarily used as the reference clock for the real-time clock (RTC), but in some modes it can be used as the main reference for the entire processor. The schematic includes loading capacitors and a resistor for the crystal circuit (C77, C78, and R93), but these components are not populated (DNP). The loading caps are not required because the K70’s internal oscillators include programmable loading caps up to 30pF. In this case the internal loading caps can be used, and so the external caps are not necessary.

5.2 USB

In order to maximize the eye for the USB signals, it is important that the on-chip FS/LS transceiver signals (USB0_DP and USB0_DM) include 33 ohm series termination resistors. These resistors need to be placed as close to the processor as possible. The USB signals should also be routed as a 90 ohm differential pair.

6 Schematic Page 5 - K70 Processor (DDR signals and Power)

This page is the second and final part of the symbol for the K70 processor. This portion of the symbol includes all of the power and ground signals for the processor and the signals for the DDR memory interface. The DDR signals will be discussed later on the DDR memory page.

6.1 DDR_VDD

The DDR_VDD pins are used to power the I/O pads for the DDR signals. This net can be 1.8V or 2.5V nominal depending on the type of memory being used. 1.8V is used for DDR2 or LPDDR1. 2.5V is used for DDR1. The TWR-K70F120M uses DDR2 memory, so DDR_VDD is 1.8V nominal.

6.2 DDR_VREF

The DDR_VREF net is actually not used as a reference for the DDR pads on the processor. The DDR2 memory on the TWR-K70F120M does require DDR_VREF, so there is a special regulator included to generate this voltage (on page 11). For DDR1 and DDR2 designs, the DDR_VREF net can be tied to the VREF used for the memory.

For LPDDR1 designs, the memory does not need VREF, so the DDR_VREF net on the processor can be tied to VDD_DDR. A midpoint VREF voltage is not required.

6.3 VDD_INT

In order to allow for reduction of power without affecting the I/O rails, the K70 includes VDD_INT pins. The VDD_INT pins are used to supply power to the internal logic on the chip. J20 is provided so that the current draw on VDD_INT can be measured and/or a different voltage can be used to supply VDD_INT than what is being used for VDD.

In a typical design VDD_INT would be connected directly to its power supply circuit or the VDD rail.

6.4 VDD

The VDD pins are used to supply the power for the I/O pads on the processor with the exception of the DDR pads and the RTC/tamper pins. J8 is provided so that the current draw on VDD can be measured and/or a different voltage can be used to supply VDD than the 3.3V supply that is provided.

In a typical design VDD would be connected directly to the main power supply circuit. Separation of the power into P3V3 and P3v3_MCU nets is not recommended unless there is a specific need for separate nets.

6.5 AVDD/AVSS

The AVDD and AVSS pins are the power and ground for the analog blocks on the K70. In order to minimize noise to the analog blocks both AVDD and AVSS are a filtered nets derived from the main VDD and VSS nets for the processor.

6.6 VREGIN

The VREGIN pin is the input to the on-chip USB regulator. In this case the USB connector is off-board so the VREGIN net comes from the elevator connectors (page 8). A jumper is supplied so that VBUS can be disconnected and/or a voltage can be supplied directly.

For a typical USB device system, VREGIN would be connected to VBUS from the USB plug. The USB connector is subjected to ESD from users plugging/unplugging cables, so some ESD protection on USB signals including VBUS is strongly recommended.

For a USB host system, VREGIN would still connect to the USB plug, but as the host needs to supply power a 5V power source on the board would be used to power both VREGIN and the VBUS at the plug. ESD is still an issue for hosts, so again, ESD protection on the USB lines including VBUS is strongly recommended.



TIP:

VREGIN is used to provide power to the on-chip FS/LS transceiver. In order to use USB0_DP and USB0_DM VREGIN MUST be powered.

6.7 VOUT33

The VOUT33 pin is the output from the on-chip USB regulator. The USB regulator can supply 3.3V and up to 120mA that can be used as the main power for the processor (VDD) and powering the board. Because the total current for the tower system with peripheral cards plugged in can exceed 120mA, the tower board is not setup to be powered by VOUT33 by default. R88 can be populated to experiment with this feature.

6.8 VBAT

The final power domain for the K70 is the VBAT domain. The VBAT powers the RTC, DryIce, and a small register file. On the tower board the VBAT can be powered directly from the same supply as VDD or you can use the coin cell circuit. The diodes in the circuit allow the VBAT to be supplied by P3V3_MCU (VDD) when the net is powered or by the coin cell if the main power is not present. For a typical end application, only one approach is needed, so J17 would be removed and VBAT would be connected as needed for the specific system.

6.9 Decoupling/Bypass caps

The exact amount and value of decoupling/bypass caps required for a design will vary. The values used on the tower board should only be used as a reference. The value and quantity of bypass caps needed for your own design will most likely not be the same.

6.10 Test Points

The tower board is an evaluation system, so test points, jumpers, headers, and connectors are available on most signals to allow for monitoring and debugging. While some applications might not allow for liberal use of test points and other means of monitoring signals (especially if the application has size constraints), keeping test points on critical signals can make debugging a much smoother process.

7 Schematic Page 6 – OS-BDM/JTAG

This page is the open source JTAG circuit. This on-board debug circuit provides a JTAG debug interface and a power supply input through a single USB mini-B connector. The OS-JTAG also includes a virtual serial port.

For most designs inclusion of a full JTAG debugging circuit is not needed. A typical end application would only include a standard ARM JTAG header, and in many cases the header would not be populated on production units. ARM has standards for several different connectors in different form factors. The number of pins and size of the connector can be selected based on design constraints and debugging capability required for the application.

8 Schematic Page 7 – SD Card, IrDA, and Pushbuttons

8.1 SD Card

The SDHC module on the K70 can be used with either a full size SD connector or a micro connector. The TWR-K70F120M board has a micro SD card connector. The card detection is done using a GPIO signal. There is an erratum that affects detection of SD card insertion and removal, so use of a GPIO signal for card detection is recommended over using the card detection features of the SDHC module. Refer to device errata e6934 for more information.

8.2 IrDA

The TWR-K70F120M includes an IR transmitter and receiver. The PTD7 pin was selected for the IR transmitter specifically because there is an option in the processor for extra drive capability on this pin. The PTD7 pin is double bonded to two pads within the package, so it can be configured for dual-pad drive strength. This setting is configured using the SIM_SOPT2[CMTUARTPAD] bit.

8.3 Pushbuttons

There are two simple pushbuttons included on the board for use as general inputs to control an application. The signals used for the pushbuttons were selected to minimize conflicts with other functions of the pins being used elsewhere on the board. In general all GPIO pins have the same functionality, so any free GPIO would be suitable for use as a pushbutton input. Keep in mind that there is only one interrupt line per GPIO port, so when possible try to use GPIOs from different ports if interrupt capability is needed. This will prevent/reduce the need for polling inside of the interrupt handler to determine the specific pin that triggered the interrupt.

9 Schematic Page 8 – Elevator Connectors

While the TWR-K70F120M is designed so that it can be used by itself, the functionality of the board can be expanded by building a tower comprised of the MCU card and peripheral cards. The tower peripheral card schematics are useful references to see how peripheral circuitry that is not included on the main MCU card can be connected to the processor.

The backside of the elevator connectors provide excellent access to all Tower card signals to assist with hardware debugging. Note that the Kinetis K70 is highly integrated and uses signals on the secondary elevator card where many lower end devices do not.

10 Schematic Page 9 – Sensors

10.1 TWRPI connectors

In addition to adding tower peripheral boards, the tower functionality can also be expanded by adding tower system plug-in boards (TWRPIs). Like the tower peripheral cards, TWRPI boards can be a good reference to see how various sensors and other devices can be connected to the processor.

10.2 Sensors

The TWR-K70F120M includes an accelerometer and touch electrodes with LEDs.

The accelerometer communicates with the processor using an I2C interface. The I2C bus is designed as a multi-master/multi-slave bus, so the same I2C bus used to communicate with the accelerometer is also used for the TWRPI and the elevator connectors.

The touch electrodes used on the tower board are simple rectangular electrodes with a small hole in the middle so that an LED can be populated under the board to shine through the electrode. A large variety of electrode patterns and arrangements can be supported. Refer to AN3863 “Designing Touch Sensing Electrodes” for more examples and hardware guidelines for touch electrodes.

11 Schematic Page 10 – DDR and NAND

11.1 DDR2

The K70 includes an SDRAM controller that supports DDR2, LPDDR1, and DDR1. The tower board uses DDR2 memory, but in general the rules for connecting any of the three memory types are the same. Making the schematic connections for the memory is simple, but the layout can be tricky.

11.1.1 DDR Layout Recommendations

- Try to minimize the overall trace lengths. The DDR should be placed as close to the processor as possible.
- The data, DQS, and DQM signals for each byte lane should be matched. Ex: DDR_DQ[7:0], DDR_DQS0, and DDR_DM0 should be matched.
- Data bits can be swapped to make layout simpler, but any data line swaps must be within the same byte lane. You can swap DDR_DQ0 and DDR_DQ1, but not DDR_DQ0 and DDR_DQ8.
- The address and command signals should be matched--DDR_A[14:0], DDR_BA[2:0], DDR_CK, /DDR_CK, /DDR_CAS, /DDR_CS, /DDR_RAS, /DDR_WE, and DDR_ODT (if used).
- DDR_CK and /DDR_CK should be routed as a pair.

11.1.2 DDR Simulation

Freescale recommends using your board layout file, the processor IBIS model, and the memory IBIS model to perform signal integrity simulations of DDR signals whenever possible. These simulations are the best means of determining if termination resistors are required on any of the DDR lines before spinning a board.

11.1.3 Terminations

The exact terminations required for the DDR signals can vary depending on your specific board and the type of DDR that is being used. For many designs, especially if the overall DDR trace lengths are short (recommended less than 2 inches), terminations might not be required at all. NOTE: LPDDR1 designs should never need any parallel terminations. For longer trace lengths series terminations might be needed.

All parallel DDR termination resistors consume power, so elimination of external termination resistors is desired whenever possible. In addition to reducing power, removing parallel terminations also simplifies the BOM and the board layout. DDR1 designs might require parallel terminations on all signals (both data and address/control). DDR2 designs can make use of on-die terminations for the data, DQS, and DQM signals, so if parallel terminations are needed they would only be used on the address and control signals.



TIP:

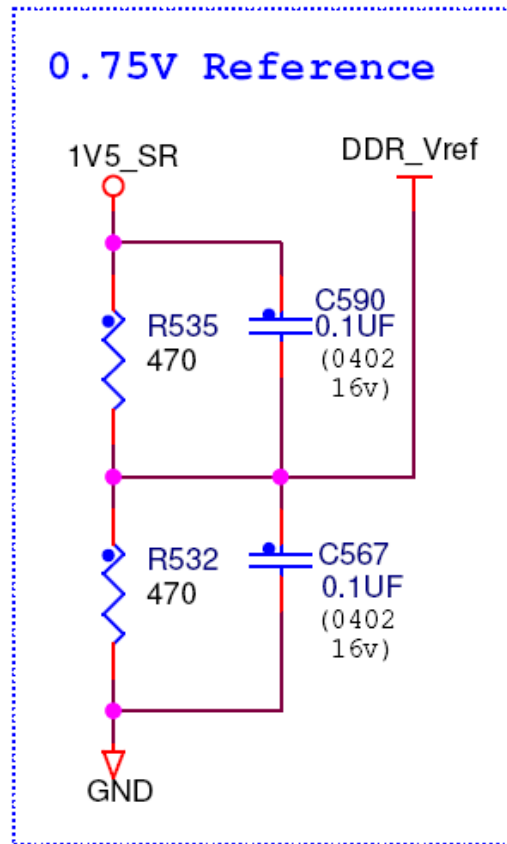
Keep the overall trace lengths short should be one of the key goals for the DDR layout. If the trace lengths are short, then the design most likely won't need any external termination resistors.

11.2 NAND

The K70 includes an on-chip NAND flash controller. The NAND signals are shared with the FlexBus interface; however, the processor can switch between functions dynamically. This means that a board can use the FlexBus and NAND with no pin conflicts, but you cannot access memories or devices on the FlexBus and the NAND simultaneously.

12 Schematic Page 11 – DDR Regulator

Use of a regulator specially designed to supply Vref and Vtt voltages is recommended for any DDR design that requires parallel terminations. Designs that do not require a Vtt voltage for parallel terminations can use a voltage divider circuit like the following:



TIP:

Never use the Vref net for parallel termination resistors. It is important to have very little noise on the Vref as this voltage reference is used by the DDR1 or DDR2 memory to determine if a signal is high or low.

The current draw through the parallel terminations will cause the Vref voltage to move and can cause signals to be incorrectly sampled by the memory.