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## Revision History

Rev 2.0	VER 0.0	30.01.06
Rev 2.0	VER 0.1	15.10.06
DDR2 + ECC , Spansion flash 256MBit		
Rev 2.0	VER 0.2	05.11.06
DDR2 detection fix		

### LEGEND :

- xx >> or >>x or <<< x On-page signal connection
- x <<< or <<<x or >>>x Off-page signal connections
- xx ↑ Signal has pull-up
- xx ↓ Signal has pull-down
- PU PD FPGA pins termination

PCB: 084-00219 -3

Freescle Semiconductor Israel Ltd.

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Title

**MPC8349EA\_MDS\_PB -TBGA**

Size  
A

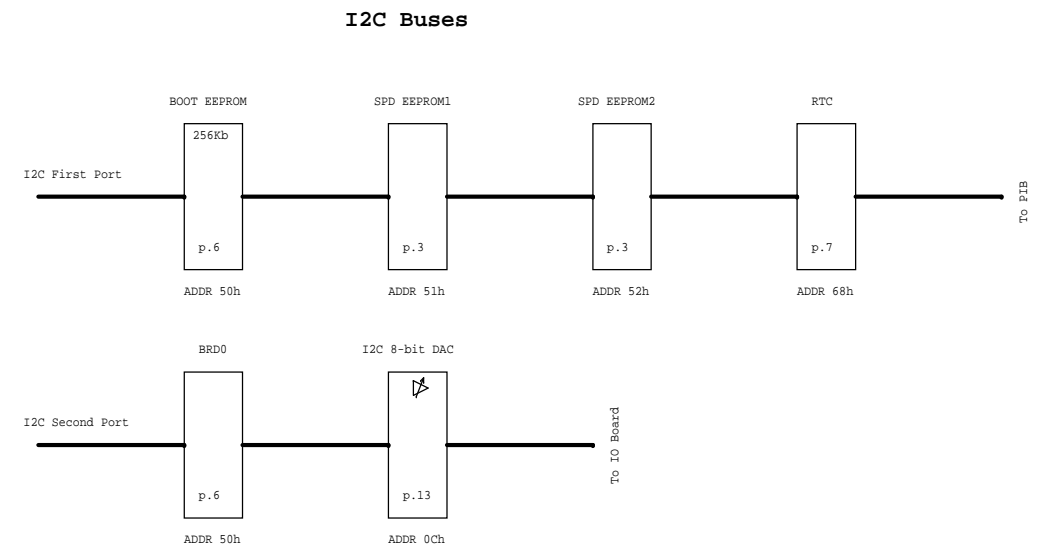
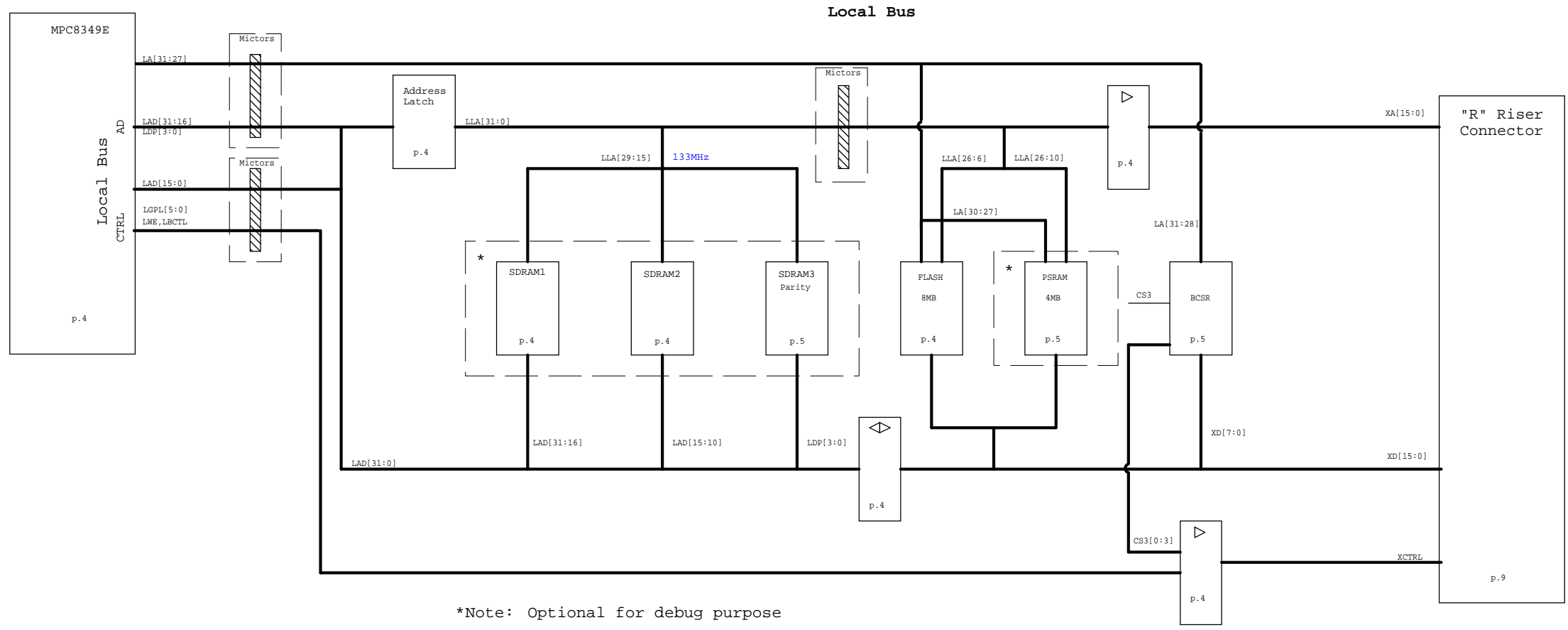
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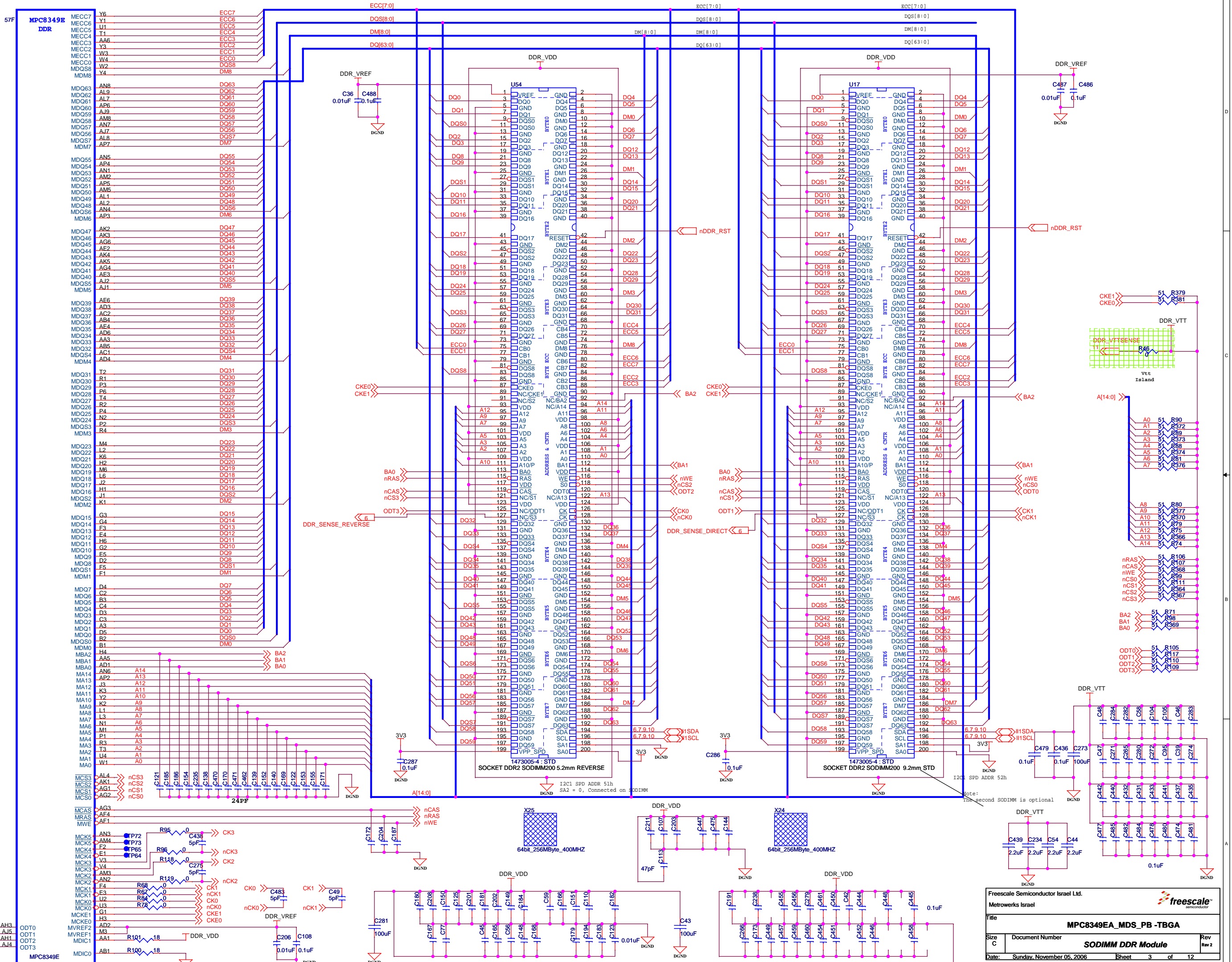
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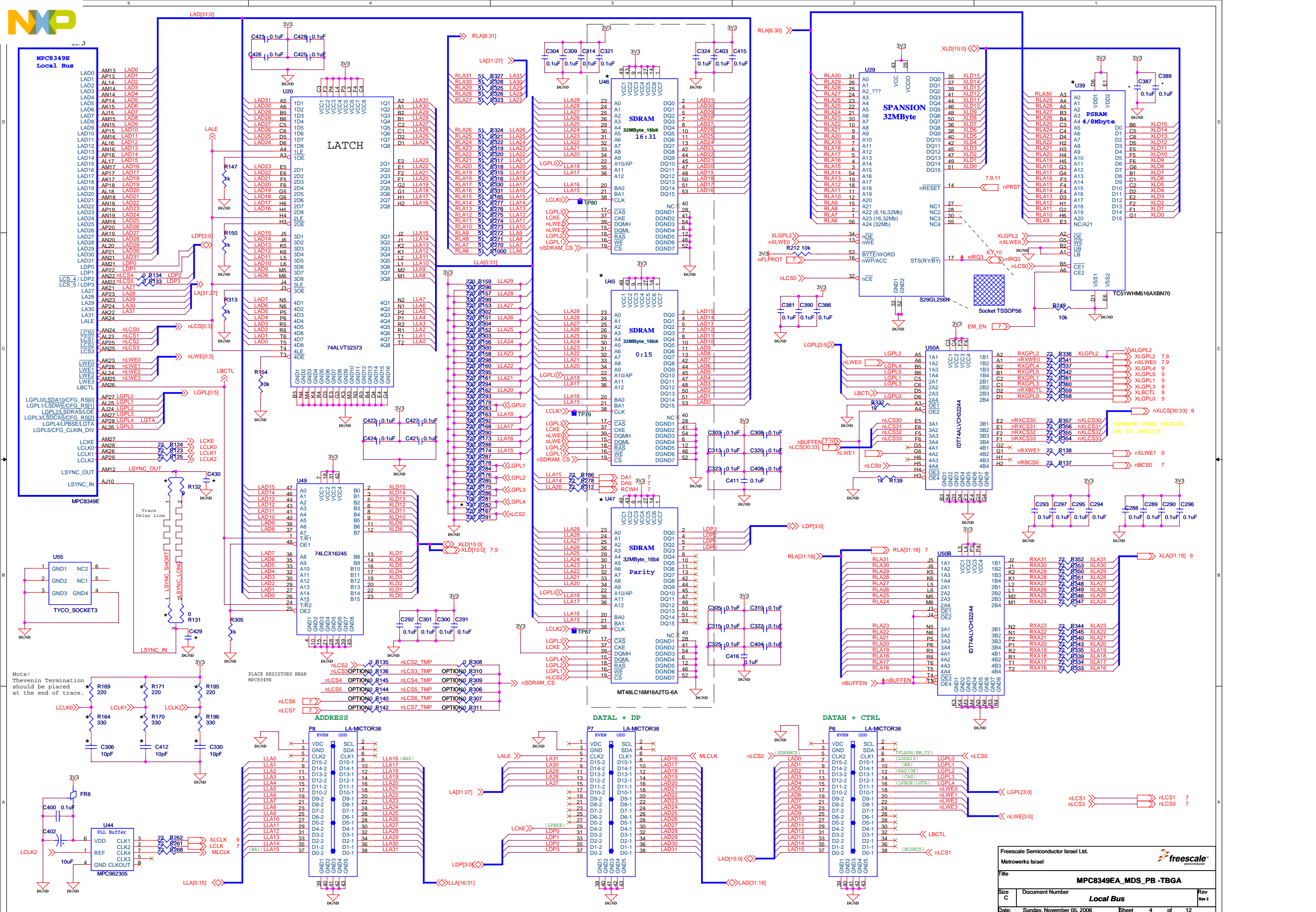
Rev  
Rev 2

Date: Sunday, November 05, 2006

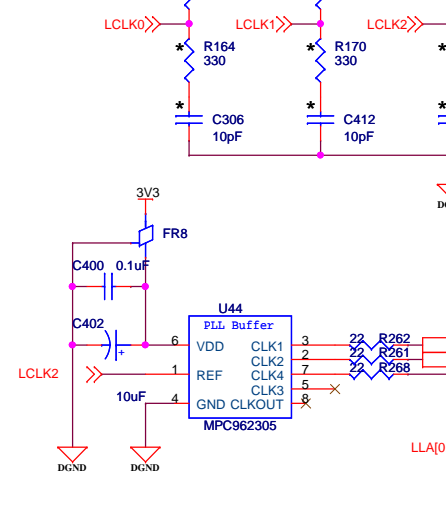
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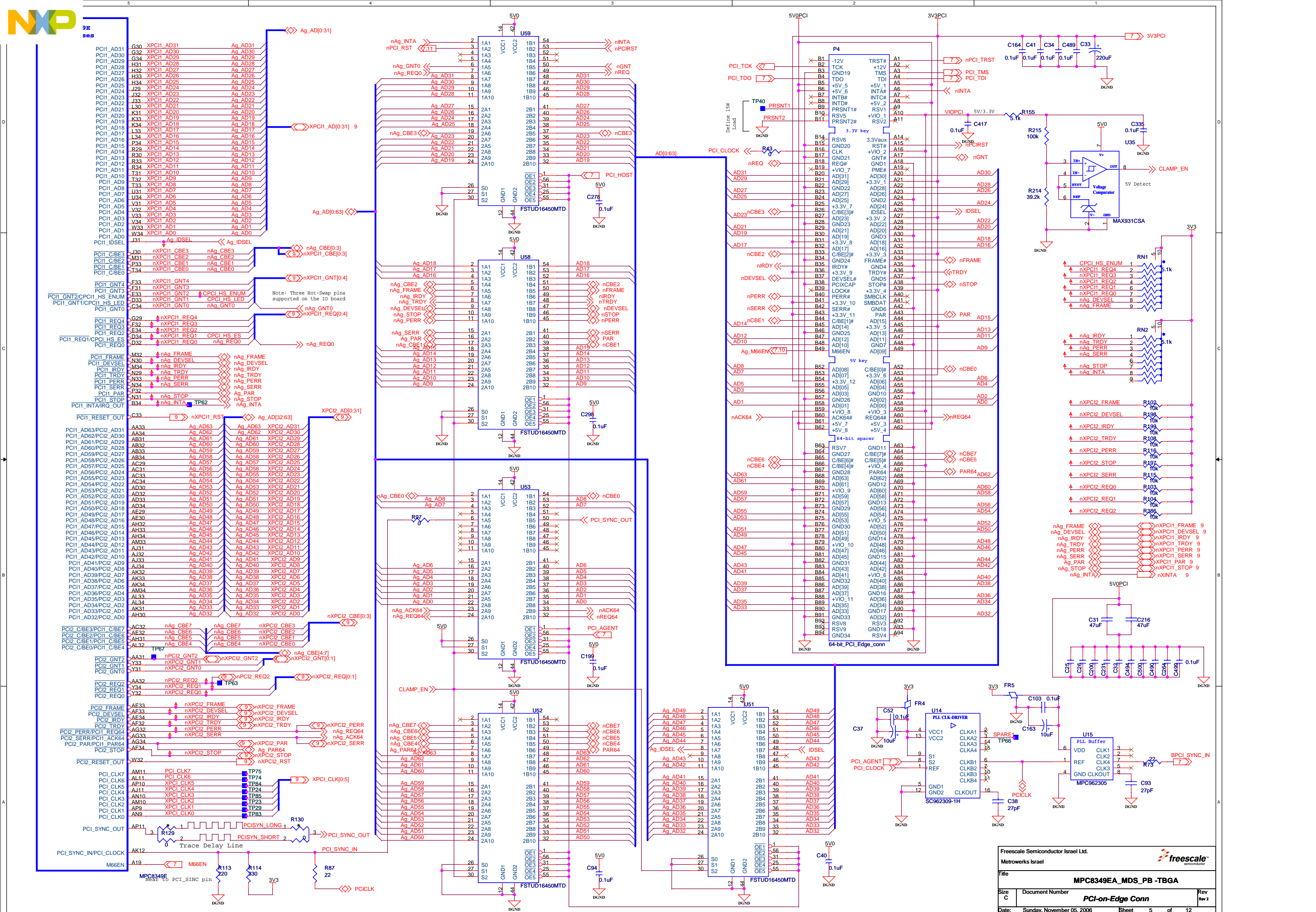


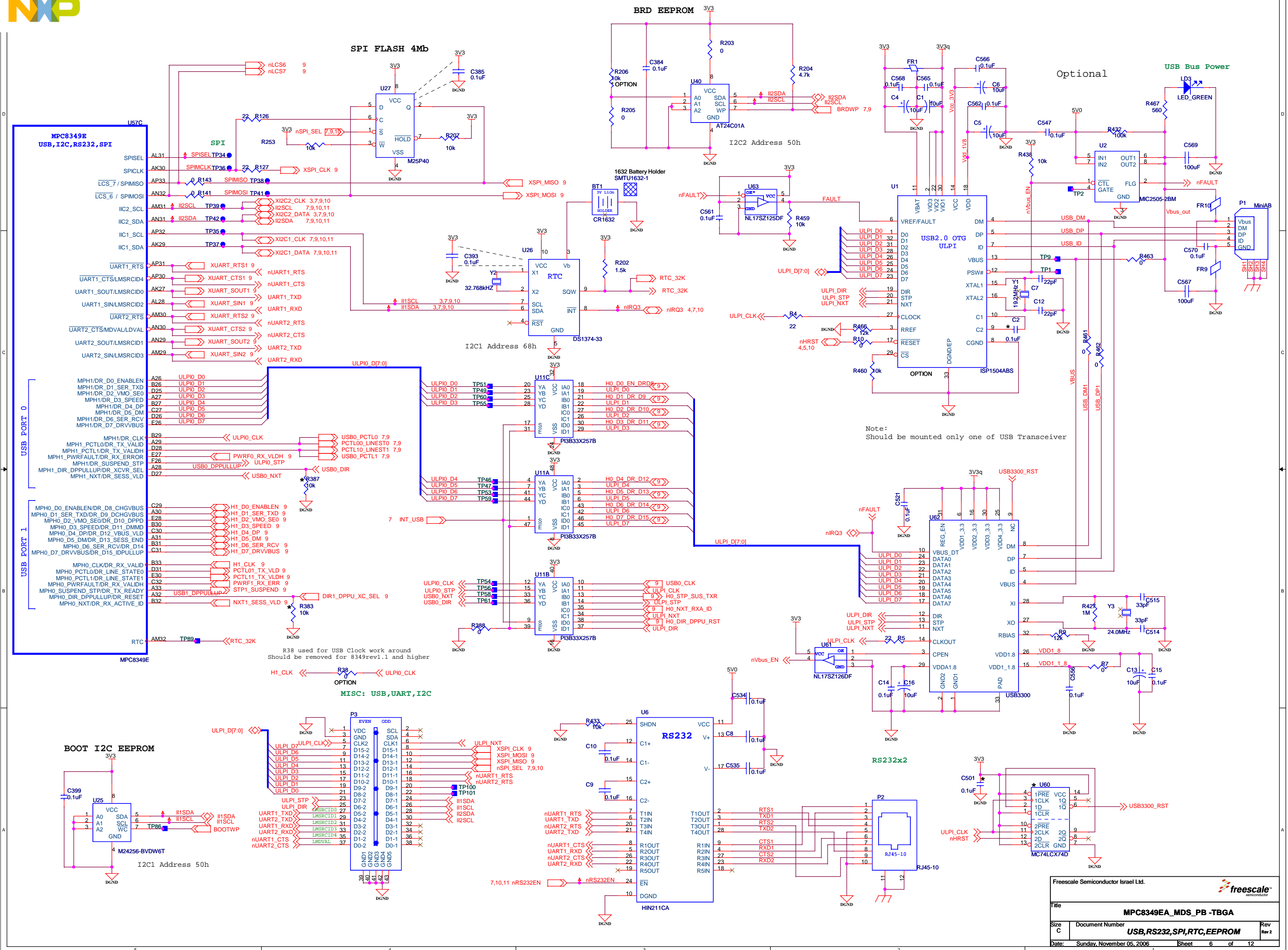


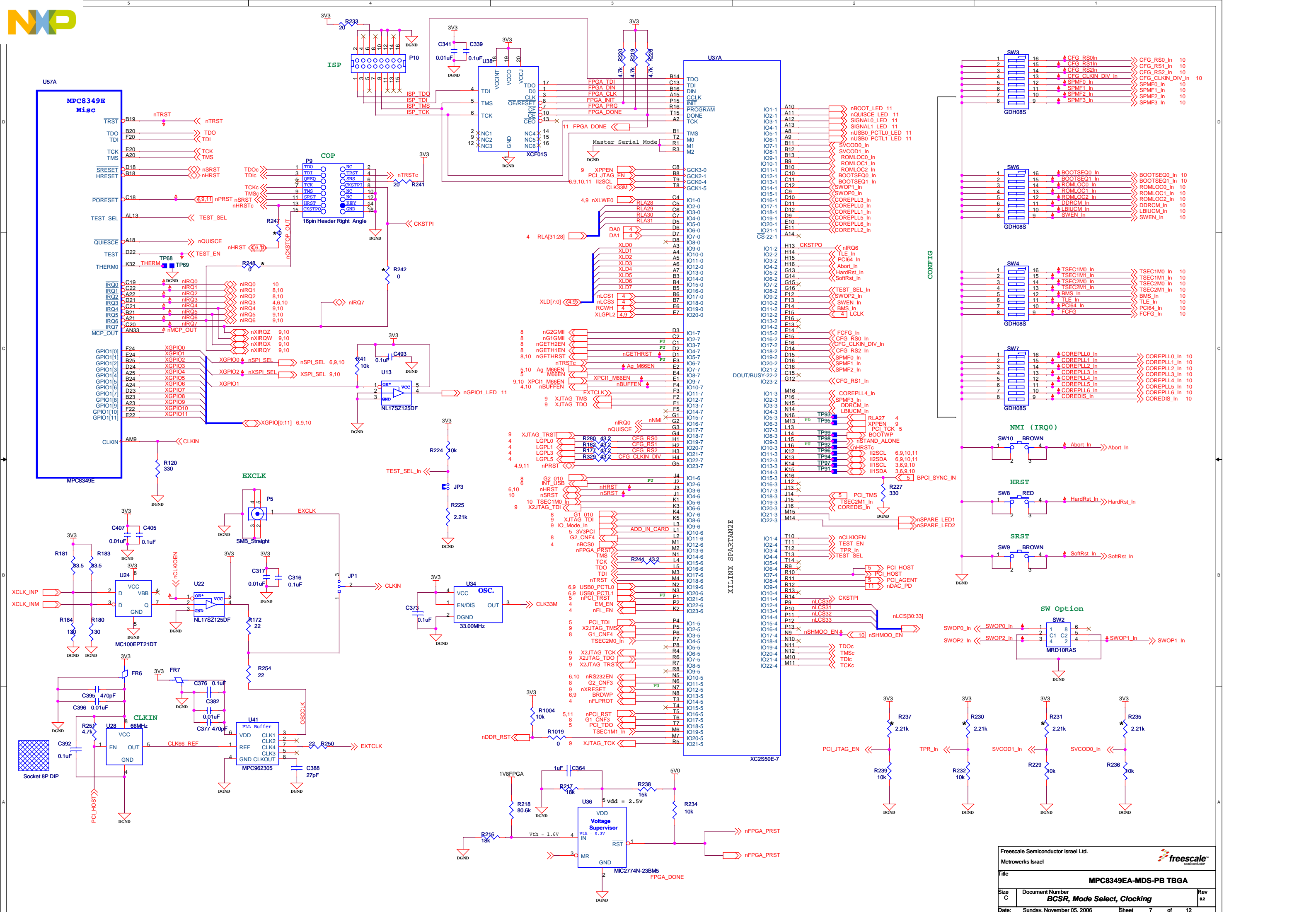


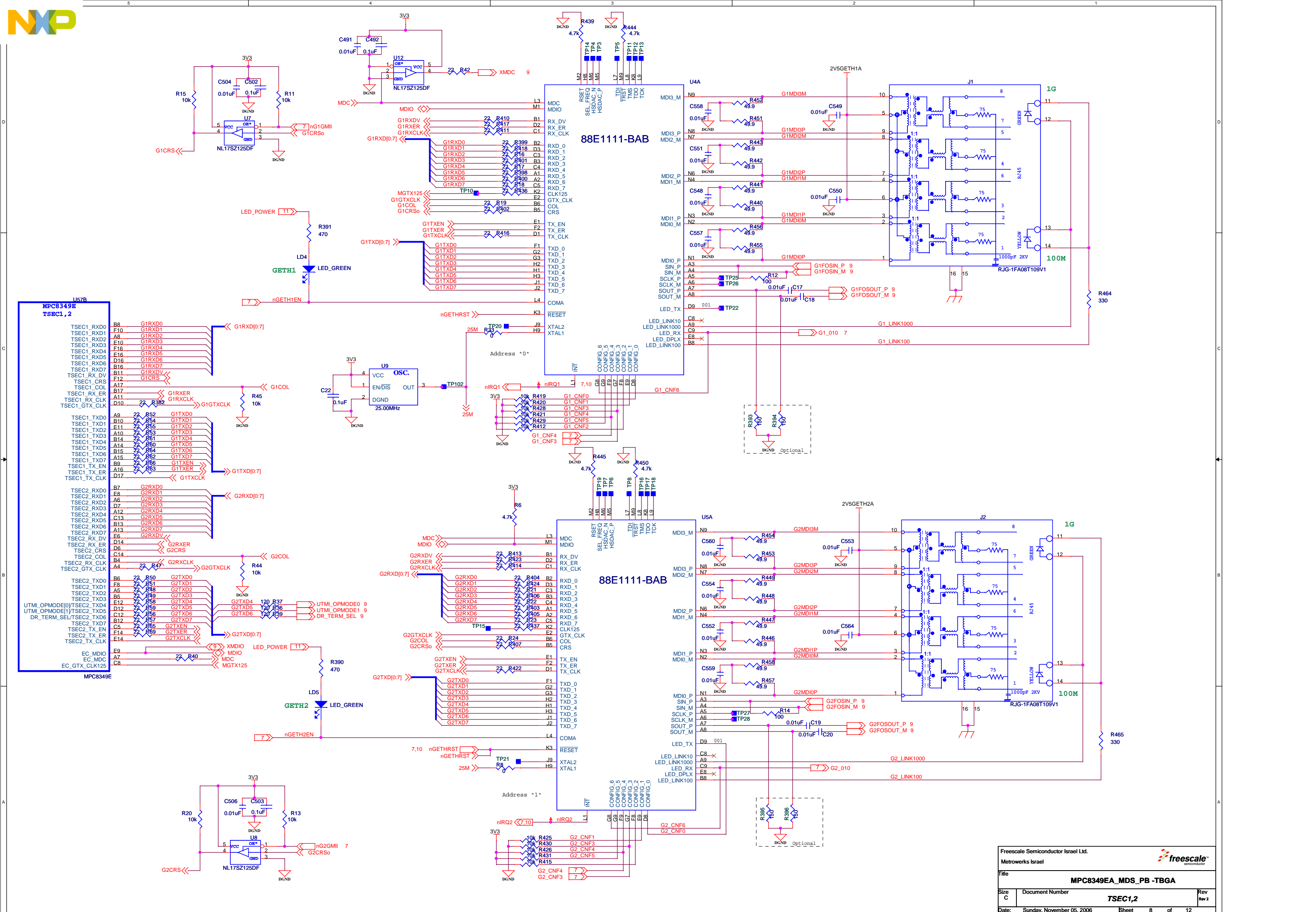
Note: Thevenin Termination should be placed at the end of trace.





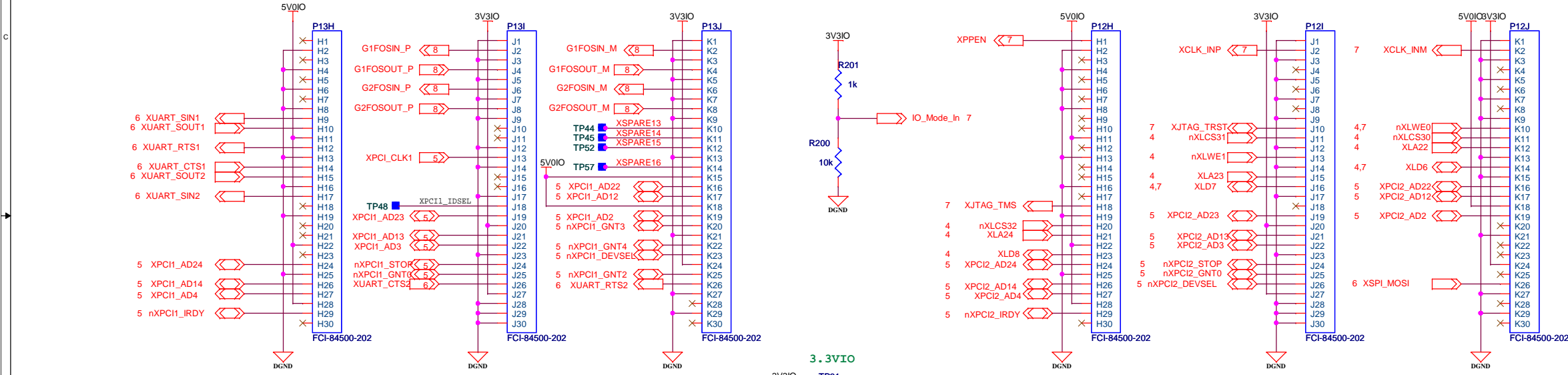
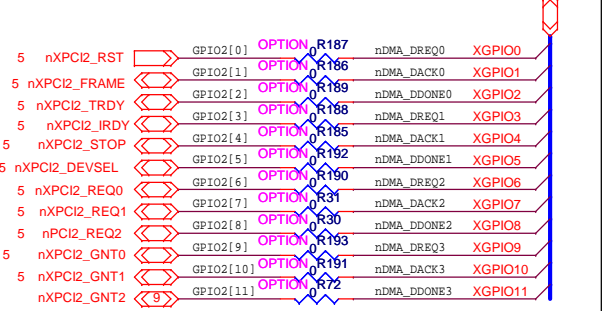
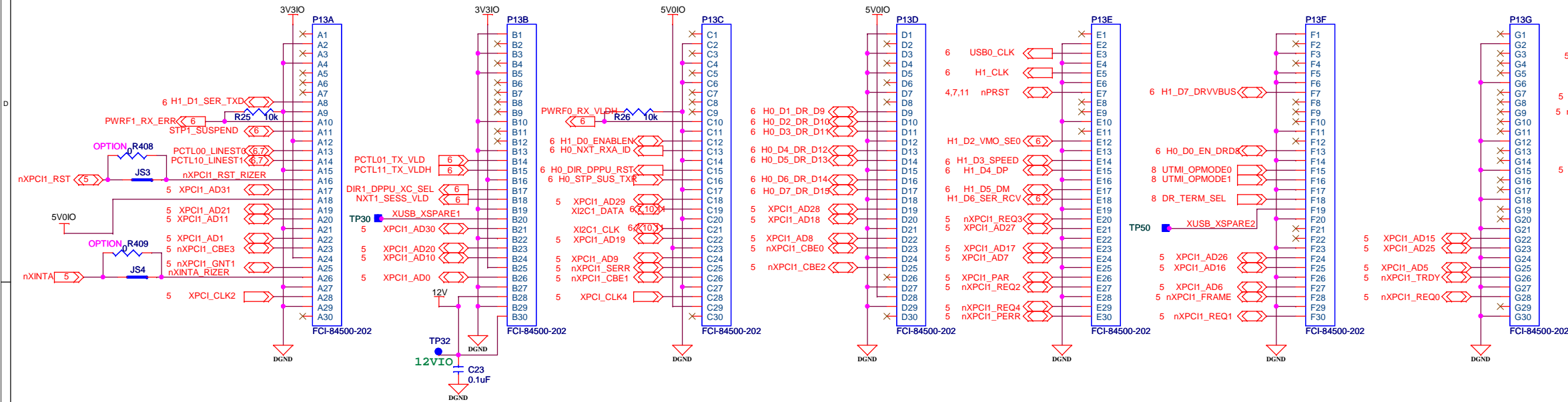




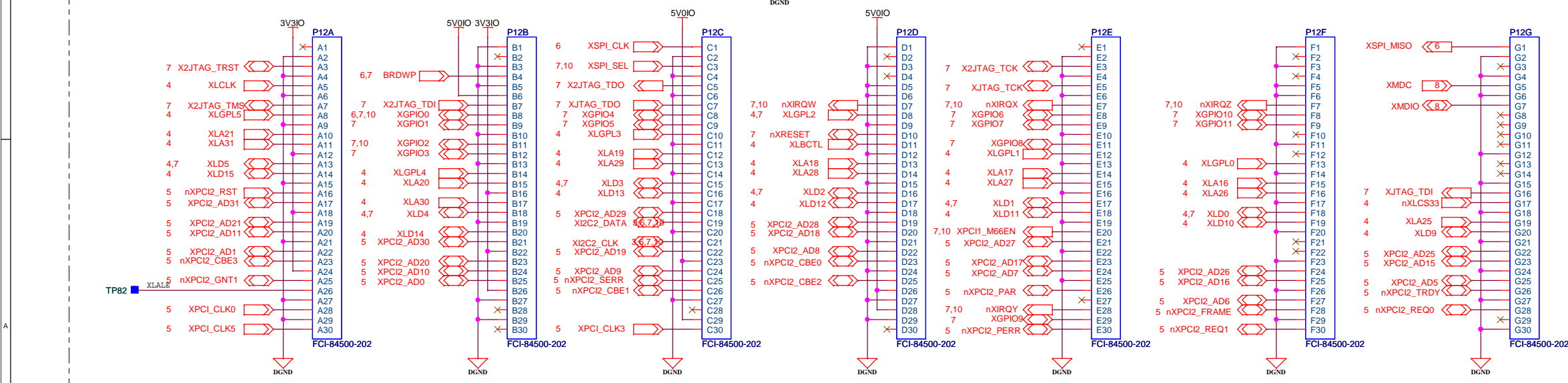




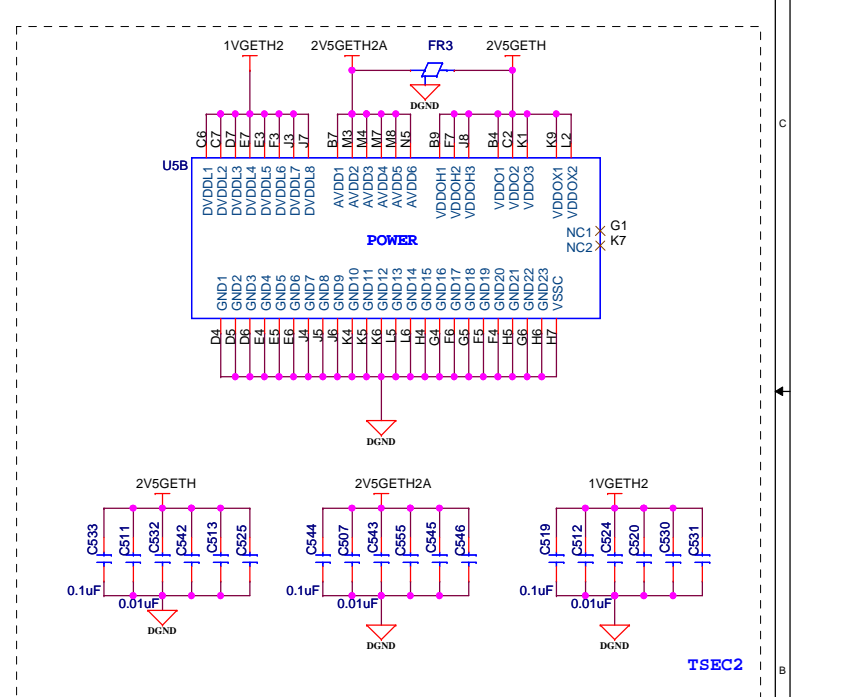
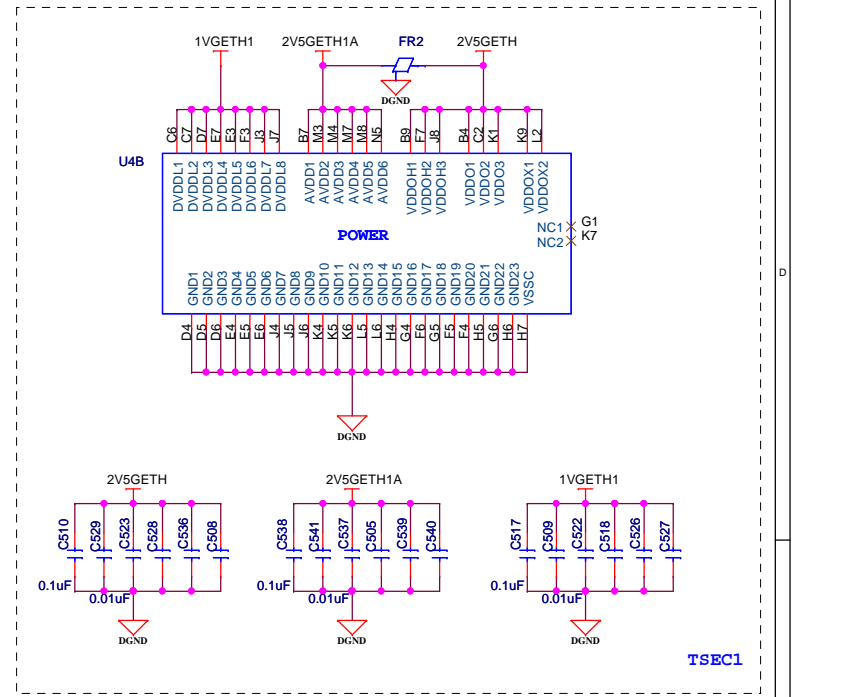
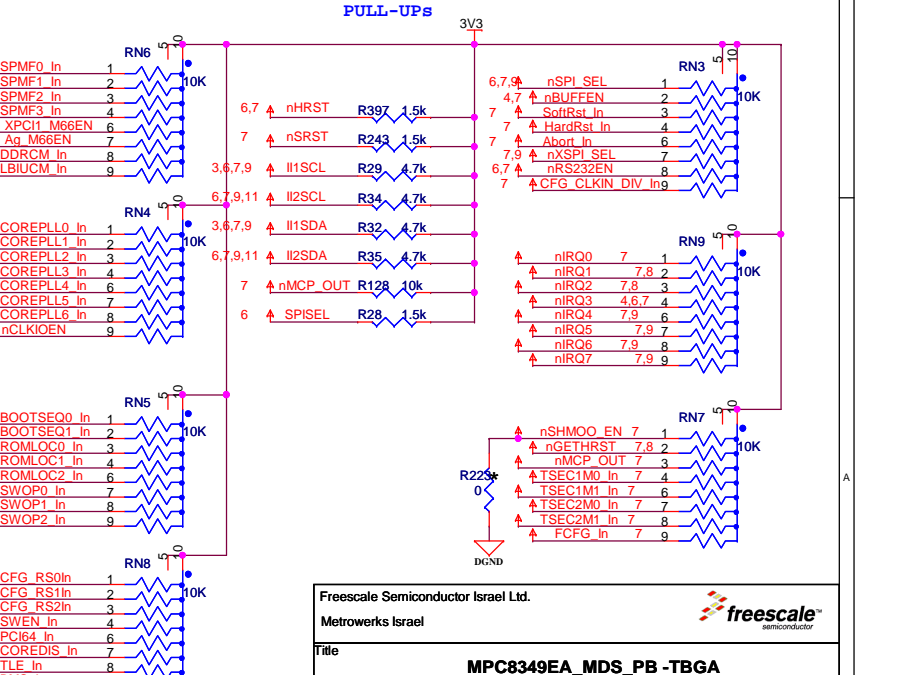
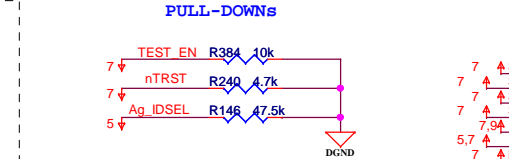
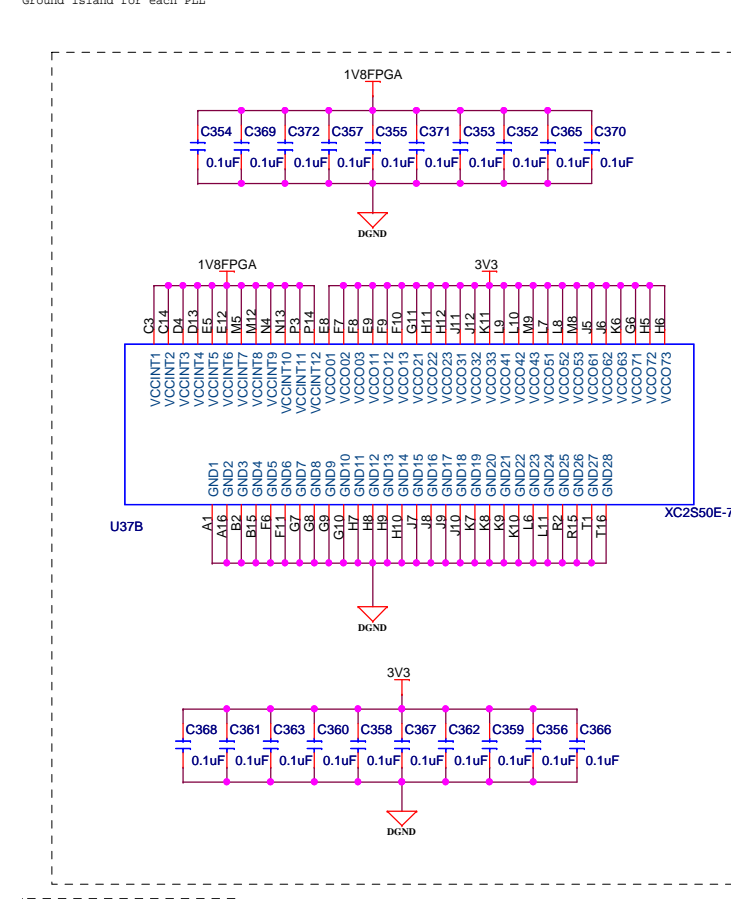
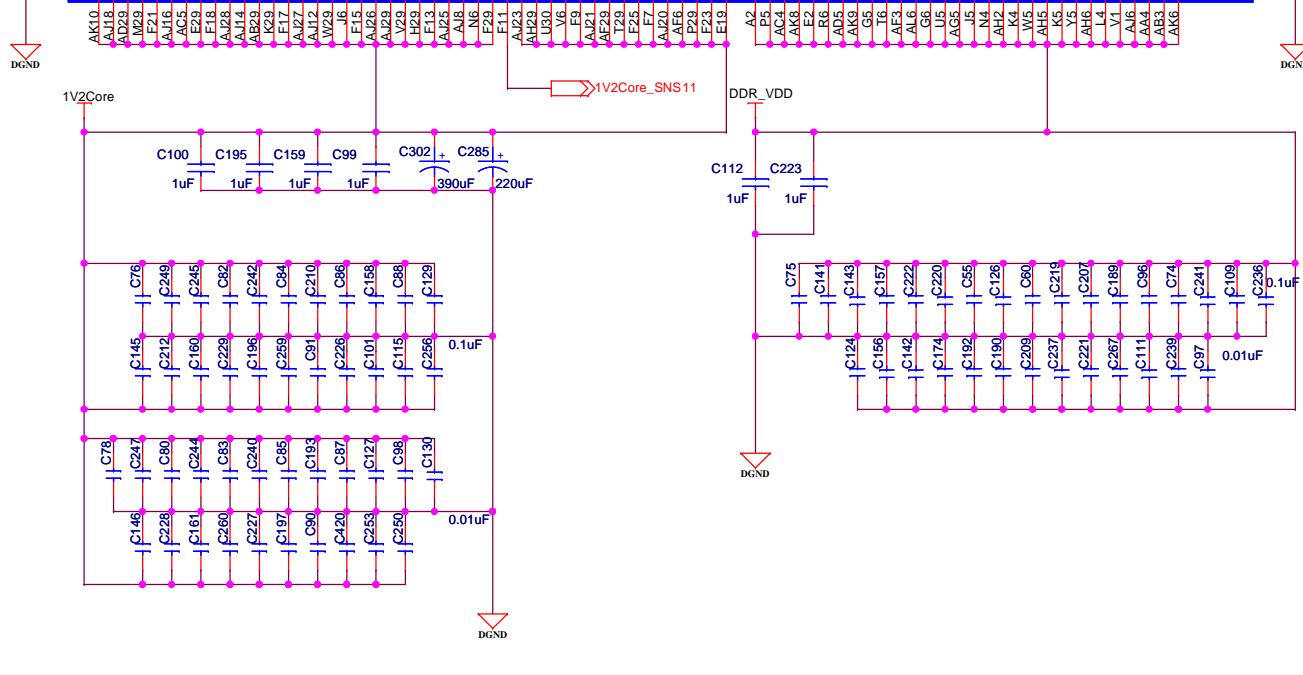
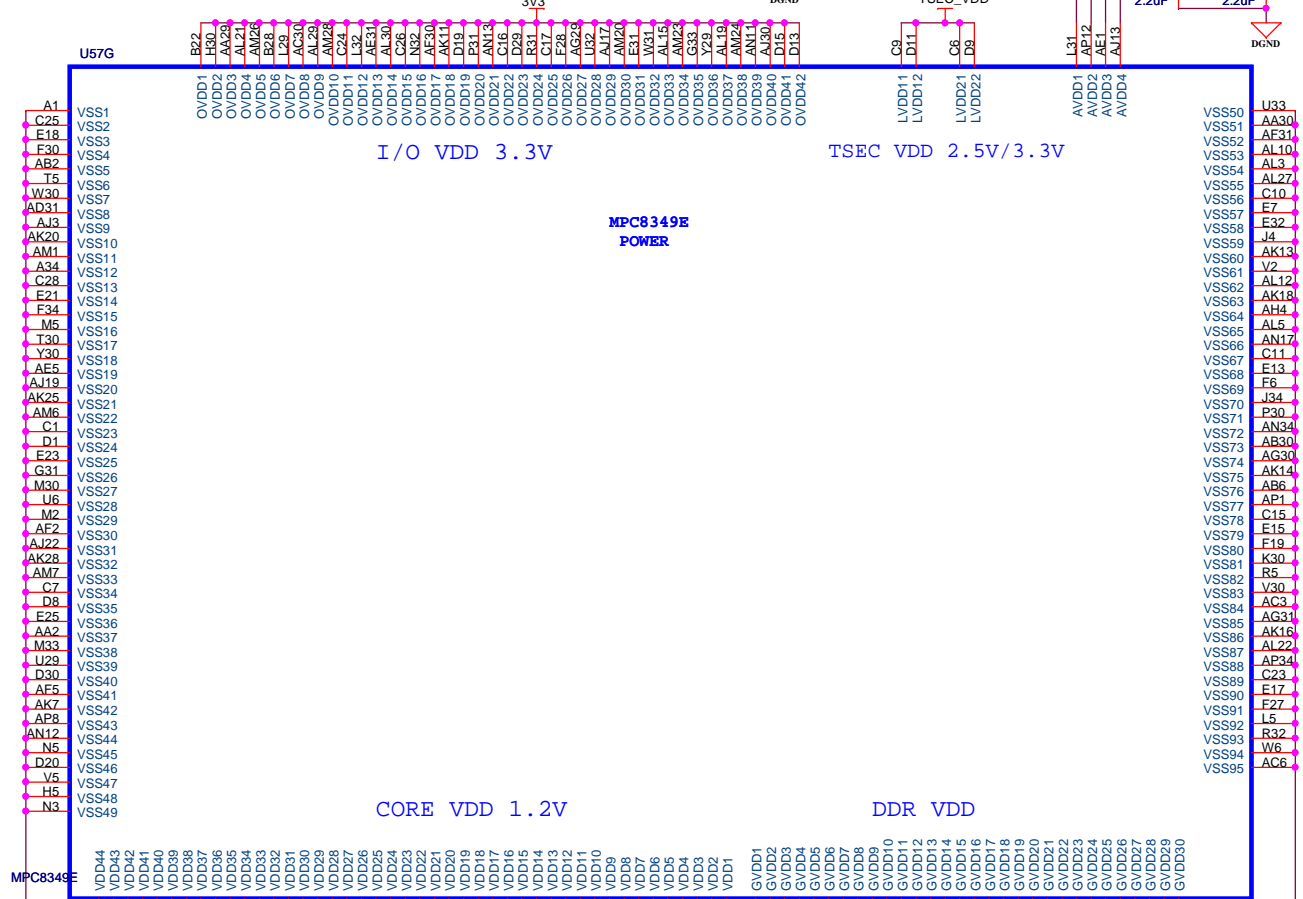
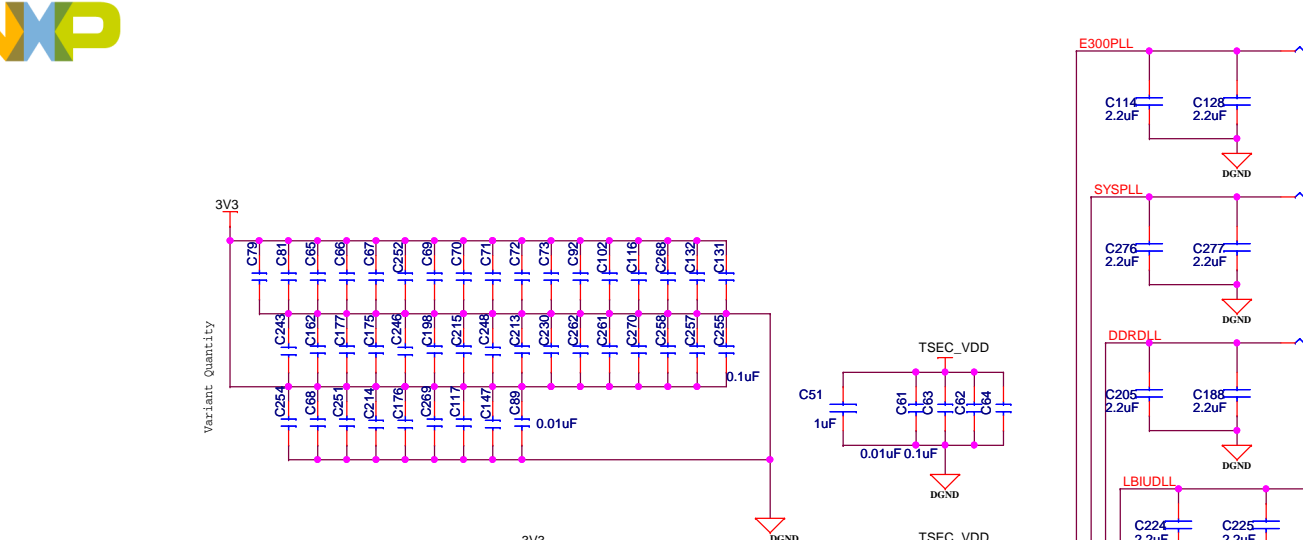
LEFT-LEFT Riser Connector



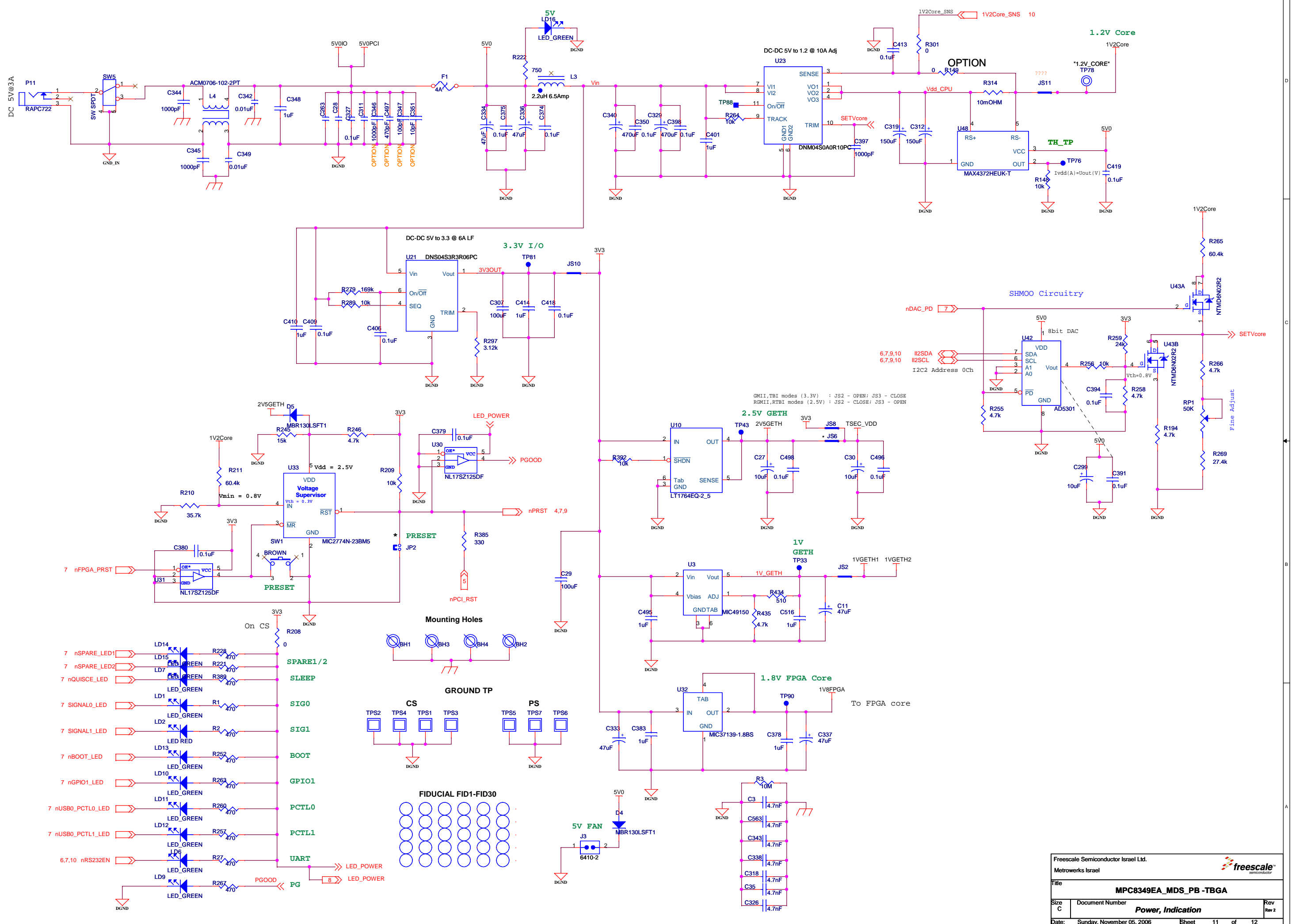
PCI2 Bus, Local Bus



RIGHT Riser Connector



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Title: <b>MPC8349EA_MDS_PB-TBGA</b>		
Size: C	Document Number: <b>Power Decoupling, Pull-Ups</b>	Rev: 2
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Title: <b>MPC8349EA_MDS_PB-TBGA</b>		
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D

D

C

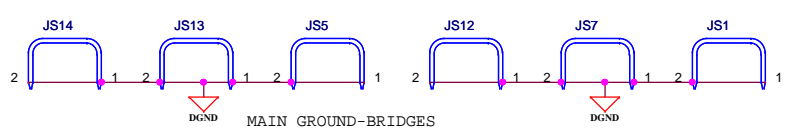
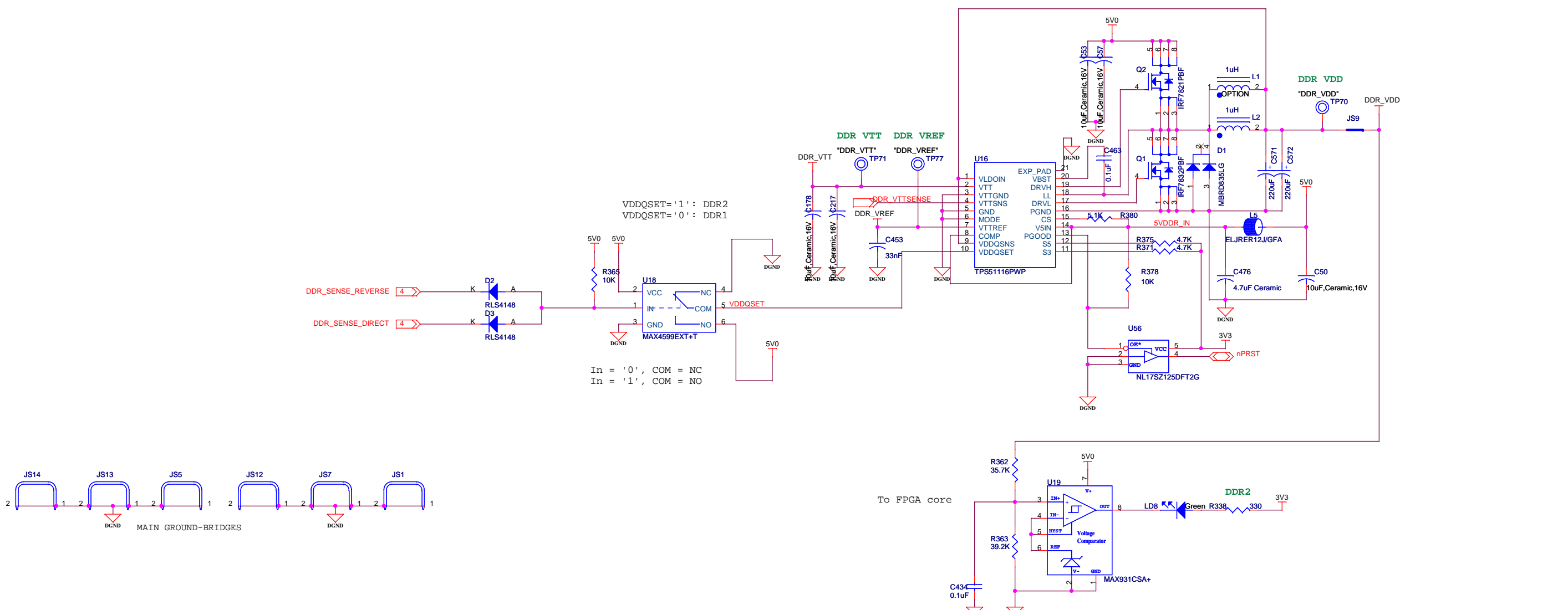
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B

B

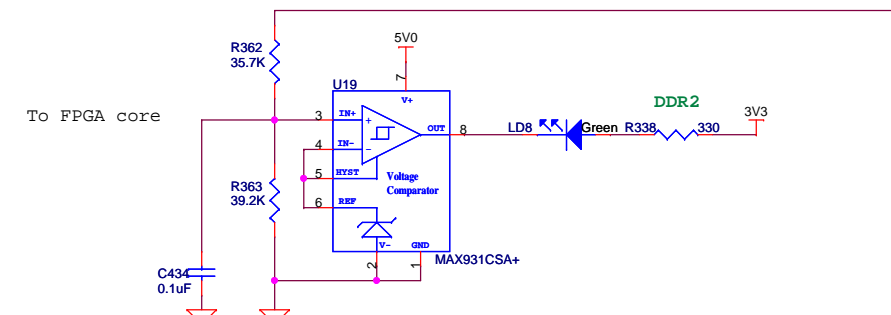
A

A



VDDQSET='1': DDR2  
VDDQSET='0': DDR1

In = '0', COM = NC  
In = '1', COM = NO



D-CAP MODE: VDDQ ADJUSTABLE, NON-TRACKING DISCHARGE  
MODE='0': Non Tracking Discharge  
S3, S5='1': VDDQ, VTTREF, VTT are ON  
VDDQSET='1': DDR2  
VDDQSET='0': DDR1