DWG. NO.	SH.	REV
LPCX5411x QFP64	1	A1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	- Chng R19 to 4.12ohm; sht 3. - Chng JS10 to R80 4.12ohm; sht 3. - Add hdr & shunt at JP3; sht 3. - Add JS28, JS29, JS30; sht 2.	04/20/2015	
A1	- Chng C8 to 2.2uF; sht 3.	05/06/2015	

ABLS2-12.000MHZ-D4Y-T

+2.5V_LINK

Fanout_TP Z4
Fanout_TP Z1
Fanout_TP Z3
Fanout_TP Z6
Fanout_TP Z5
nTRST_LINK2
SWDIO_LINK2
SWDCLK_LINK2
R52 12Kohms
R53 12Kohms
R54 12Kohms
R65 2.2Kohms
GND

U12
LPC4322JET100
LPC4322JET100

nTRST
STDI/TDI
TMS/SWDIO
TCK/SWDCLK
TDO/SWO
DBGEN
nRESET
VBAT
VDDREG_1
VDDREG_2
VDDREG_3
VDDIO_1
VDDIO_2
VDDA
XTAL1
XTAL2
RTCX1
RTCX2
RTC_ALARM
WAKEUP0
ADC0
ADC1
ADC2
ADC3
VSSA
VSSIO_1
VSSIO_2
VSSIO_3
VSSIO_4
VSSIO_5
VSSIO_6

Y2 12M
C30 27pF
C31 27pF
R55 100Kohms
Z7 Fanout_TP

FB1
3v3_LNK_CORE
C36 4.7uF 10v
C34 0.1uF
C35 0.01uF
C20 0.1uF
C12 0.01uF
C27 0.1uF
C29 0.1uF

SHT 4, 5 BRIDGE_SCL JS3
SHT 4, 5 BRIDGE_SDA-WAKEUP JS2
I2C0_SCL
I2C0_SDA

+2.5V_LINK
C19 10uF
C28 4.7uF 10v
C26 10uF
C33 0.1uF
C32 0.01uF

U12
LPC4322JET100
LPC4322JET100

CLK0_/EXTBUS_CLK0/CLKOUT
CLK2_/EXTBUS_CLK2/CLKOUT//SDIO_CLK/I2S0_TX_MCLK/I2S1_RX_CLK
USB0_DP
USB0_DM
USB0_VBUS
USB0_ID
USB0_VDDA3V3_DRVR
USB0_VDDA3V3
USB0_RREF
USB0_VSSA_TERM
USB0_VSSA_REF
USB1_DP
USB1_DM
I2C0_SCL
I2C0_SDA

USB_DP_LINK
USB_DM_LINK
USB_VBUS_LINK
USB_ID
R72 0ohms
R58 12Kohms

Power-On LED

VDD_LPC5411x
R75 100ohms
D3 LG L29K-G2J1-24-Z (Green)

Link +2.5V Power

U25 TLV70225DBVR 300mA
Vin Gnd Ena Vout nc
C53 4.7uF 10v
C64 0.1uF
C65 0.1uF
C54 4.7uF 10v
JS23

GND TP

TP1 DNI
HDR-1x02

Target +3.3V Power

U24 XC6227C331PR-G
CE VIN VROUT NC GND
C58 4.7uF 10v
C59 0.1uF
C60 0.1uF
C46 4.7uF 10v
JS21
+3.3V
M3
JP9
HDR-1x03
VDD_LPC5411x

LPC5411x VDD voltage select JP9

VDD = 3.3V; 2 - 3 (default)
VDD = 1.8V; 1 - 2

Target +1.8V Power

U23 LP5951MF-1.8 LP5951MF-1.8 150mA
VIN GND ENA VOUT NC
+1.8REG
C55 1uF 10V
C56 0.1uF
C57 0.1uF
C45 10uF
JS20
+1.8V
Fanout_TP Z8

USB Device Micro-B

U21 PRTR5V0U2X
I/O1 I/O2 GND VCC
R74 270ohms
FB3 220ohms
J7 ZX62D-B-5P8
SHLD1 SHLD2 SHLD3 SHLD4 SHLD5 SHLD6
VBUS D- D+ ID GND
USB_VBUS_LINK
USB_DM_LINK
USB_DP_LINK
USB_ID
C44 1uF 10V

CONTRACT NO.		LINK2 LPC43xx	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	5/6/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	05/06/15	SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV A1	
		SCALE	SHEET 1 OF 06

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U12
LPC4322JET100
LPC4322JET100

P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1
P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

TRACE_D0 G2
TRACE_D1 G1
SHT 3 CUR_MEAS_SEL H1
BOOT0_LED K2
BOOT1 K1
SHT 3 BRIDGE_L_MISO J1
SHT 3 BRIDGE_L_MOSI J2
TMS_SWDIO_TXEN J4
TMS_SWDIO K4
NC G4
NC H5
SHT 3 BRIDGE_L_INTR-ISP1 J5
H6
NC
SHT 3 BRDG_INTR-ISP1_DIR J7
TRACE_CLK K7
H8
NC J8
TDO_SWO K8
TRACE_D2 K8
TRACE_D3 H9
TCK_SWCLK H10
JTAG_TDI J10
SHT 3 BRIDGE_L_SCK K9
SHT 3 BRIDGE_L_SSEL K10

U12
LPC4322JET100
LPC4322JET100

P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4
P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
P3[3]_/SPI_SCK/SSP0_SCK/SPIFI_SCK
P3[4]_/GPIO1[14]///SPIFI_SIO3
P3[5]_/GPIO1[15]///SPIFI_SIO2
P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

TARGET_UART_RXD G10
TARGET_UART_TXD G7
TARGET_UART_CTRL F5
NC D8
NC D9
NC D10
JTAG_RESET
JTAG_RESET_TXEN G9
BOOT_FLASH C10
BOOT2 C6
BOOT3 B10
NC E8
ISP_CTRL A9
B9
IF_DETECT R29 NC A10
1.5Kohms
NC A8
NC F7
NC G6
SHT 3 SSP0_SCK_LINK A7
B8
NC B7
NC C7
SHT 3 SSP0_MISO_LINK D7
SHT 3 SSP0_MOSI_LINK E7
SHT 3 SSP0_SSEL_LINK E7

U12
LPC4322JET100
LPC4322JET100

NC H7
NC G5
J9
F6
NC F9
F8
C9
NC H4

P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

R45 DNI 2.2Kohms
R43 DNI 2.2Kohms
R44 DNI 2.2Kohms
R42 2.2Kohms
GND

+2.5V_LINK
R51 2.2Kohms
R40 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R41 2.2Kohms
R50 2.2Kohms
R71 2.2Kohms
D1
LS Q976-NR-1
default = Not shunted M6
JP5
BOOT_FLASH 2 1
HDR-1x02
Short JP5 to force DFU boot
(when internal flash is programmed)
GND GND GND

Link LPC4322 Boot mode

DFU USB0 = B3:0 = 0101

VDD_LPC5411x

Buffer Pwr Select (JP2)

On-board Target 1 - 2 (default)
Off-board Target 2 - 3

M1 1
JP2
HDR-1x03
2
3
NC

+2.5V_LINK

U8
1 VCCA VCCB 8
TCK_SWCLK 2 A0 B0 7
JTAG_TDI 3 A1 B1 6
R47 5 DIR GND 4
100Kohms
SN74AVC2T45DCTR
SN74AVC2T45DCTR
R32 100ohms VDD_TRGT_SWD
R46 100ohms IF_TCK_SWCLK
IF_JTAG_TDI
C13 0.1uF
GND GND

U13
74LVC1T45GW
1 VCCA VCCB 6
2 GND DIR 5
TDO_SWO 3 A B 4
74LVC1T45GW
C14 0.1uF
R59 100Kohms
IF_TDO_SWO
GND GND

U14
74LVC1T45GW
1 VCCA VCCB 6
2 GND DIR 5
TMS_SWDIO 3 A B 4
74LVC1T45GW
C21 0.1uF
R60 100Kohms
R61 100ohms IF_TMS_SWDIO-SPIFI_IO0
TMS_SWDIO_TXEN
GND GND

R66 2.2Kohms

U1
74LVC1T45GW
1 VCCA VCCB 6
2 GND DIR 5
JTAG_RESET 3 A B 4
74LVC1T45GW
C2 0.1uF
R10 100Kohms
R11 100ohms IF_RST
JTAG_RESET_TXEN
GND GND

R12 2.2Kohms
GND

+2.5V_LINK
U3 5 VCC
ISP_CTRL 2 A Y 4 R17 100ohms IF_ISPEN
GND
3 74LVC1G07GW
GND

Target SWD Debug

C6 10uF
GND

P1
1 3 5 7 9
1 3 5 7 9 2 4 6 8 10
2 IF_TMS_SWDIO-SPIFI_IO0
4 IF_TCK_SWCLK
6 IF_TDO_SWO
8 IF_JTAG_TDI
10 IF_RST
SHT 4, 6
FTSH-105-01-L-DV-K

IF_DETECT R18 0ohms
GND

U2
PESD3V3L5UK
1 IF_JTAG_TDI
3 IF_RST
2 4 IF_TDO_SWO
5 IF_TMS_SWDIO-SPIFI_IO0
6 IF_TCK_SWCLK
GND
3.3

JS28 IF_TCK_SWCLK TCK-SWDCLK_TRGT-SPIFI_IO1
JS29 IF_RST nRESET_ULP
JS30 IF_TDO_SWO TDO-SWO_TRGT-SPIFI_IO2

VDD_LPC5411x
C3 0.01uF
GND

U4
R16 100Kohms
VDD
IF_TCK_SWCLK 1 1Y0 1Z 16 NC
15 1Y1
IF_RST 5 2Y0 2Z 4 TCK-SWDCLK_TRGT-SPIFI_IO1 SHT 4, 6
3 2Y1
9 3Y0 3Z 8 nRESET_ULP SHT 4, 5, 6
7 3Y1
IF_TDO_SWO NC 13 4Y0 4Z 12 TDO-SWO_TRGT-SPIFI_IO2 SHT 4, 6
11 4Y1
2 S GND 6
NX3DV2567GU,115
GND

JP1
1
2
HDR-1x02
default = Not shunted M5
GND

Target to debug location (JP1)

On-board Target - open (default)
Off-board Target - short

TRACE_CLK R30 DNI 0ohms NC
TRACE_D0 R27 DNI 0ohms NC
TRACE_D1 R26 DNI 0ohms NC
TRACE_D2 R31 DNI 0ohms NC
TRACE_D3 R28 DNI 0ohms NC

LPC-5411x Target
does not have trace.

VDD_LPC5411x
U18
5 VDD
TARGET_UART_CTRL 6 SEL
SHT 5 P0_0-ISP_RX_FTDI 3 Y0 Z 4 TO_MUX_P0_0-ISP_RX SHT 4
TARGET_UART_RXD 1 Y1
GND
R67 2.2Kohms
2 74LVC1G3157GW
GND

+2.5V_LINK VDD_LPC5411x
U6
74LVC1T45GW
1 VCCA VCCB 6
TARGET_UART_TXD R56 100ohms 2 GND DIR 5
3 A B 4 P0_1-ISP_TX SHT 4, 5
74LVC1T45GW
C9 0.1uF
GND GND

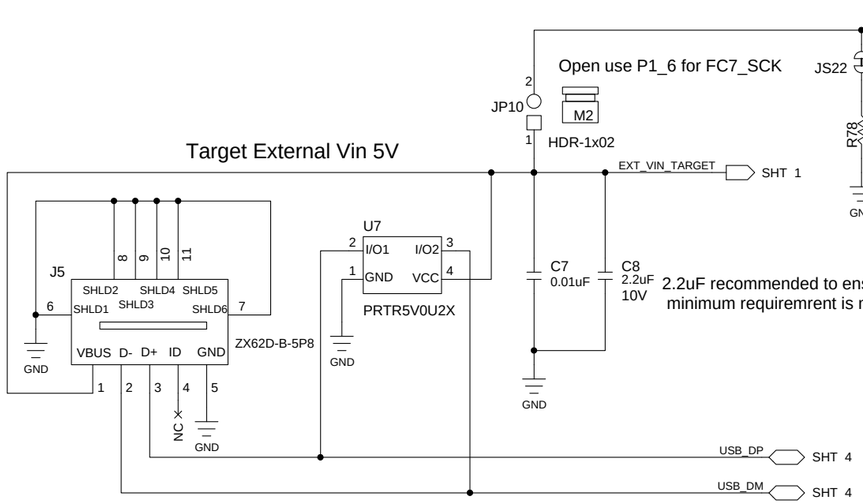
IF_ISPEN R13 0ohms P0_31-PDM0_CLK-ISP0_EN SHT 4, 5, 6

CONTRACT NO.		Link2 LPC43xx Peripheral	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	4/21/2015		
CHECKED			
ISSUED	05/06/15	SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV A1	
		SCALE	SHEET 2 OF 06

H=8ND; V=4LA

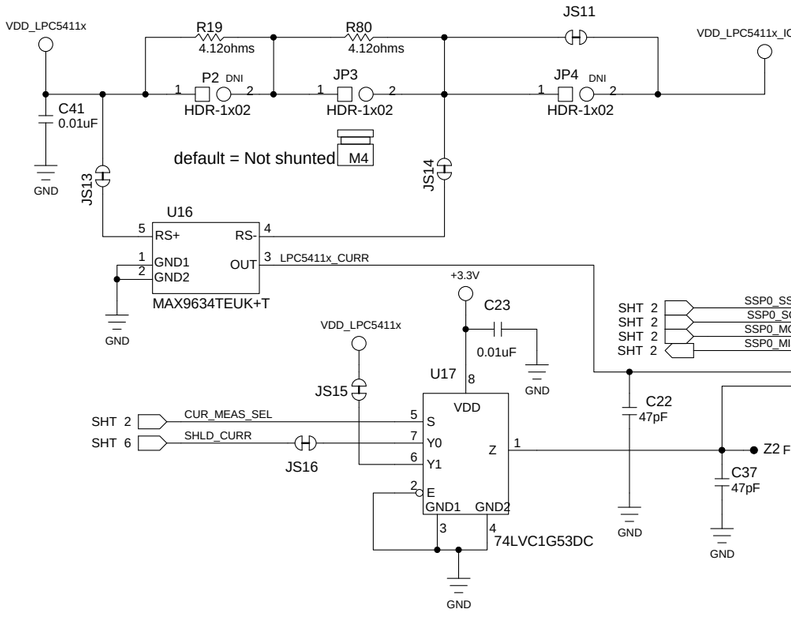
REVISIONS

REV	DESCRIPTION	DATE	APPROVED



LPC5411x Current measurement				
LPC5411x				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP3 open LPC5411x Current 1-lsb	JP3 shunted LPC5411x Current 1-lsb	maximum current	ADC input 1- lsb
32uV	3.88uA	7.77uA	16mA	800uV

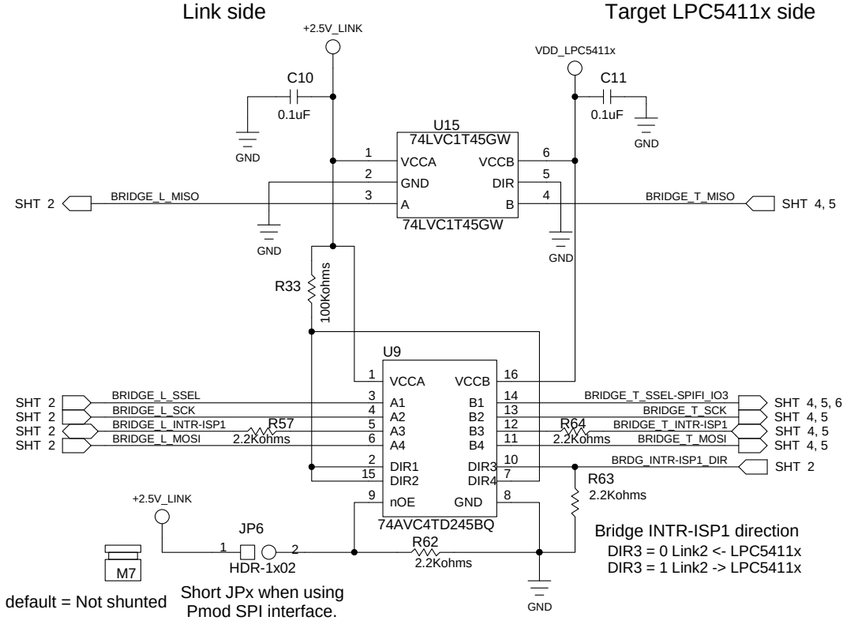
(1) Vsense voltage is between U16 RS+ to RS-. Total Rvsense = R19 + (JS10 || JP3).



JP3 Setting

VDD LPC5411x (volts)	JP3	Total Rvsense (ohms)
3.3V	open	8.24
1.8V	shunted	4.12

Isolate Bridge SPI interface
(minimize leakage current)



CONTRACT NO.		LPC5411x current measurement; Link2 SPI isolation transceiver	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	5/6/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	05/06/15	SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV A1	
		SCALE	SHEET 3 OF 06

H=8ND, V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

ISP0 Bootload Enable

KMR221GLFS SW2 — Shld, 5, 2, 3, 4, 1 — GND, GND, NC, NC — R3 2.2Kohms — P0_31-PDM0_CLK-ISP0_EN

ISP1 Bootload Enable

KMR221GLFS SW3 — Shld, 5, 2, 3, 4, 1 — GND, GND, NC, NC — R4 2.2Kohms — BRIDGE_T_INTR-ISP1

Boot Modes	ISP0 (P0.31)	ISP1 (P0.4)	VBUS (P1.6)
I2C/SPI boot	0	0	X
UART boot	0	1	0
USB MSC boot	0	1	1
FLASH boot	1	X	X

RESET

VDD_LPC5411x — R76 100ohms — D4 LG L29K-G2J1-24-Z (Green) — nRESET_ULP — R77 100ohms — C47 0.01uF — GND

SW4 KMR221GLFS — Shld, 1, 4, 3, 2, 5 — NC, NC, GND

RGB LED

+3.3V — JP8 DNI HDR-1x02 — JS19

D2 WR-PA3528UEUGUB-S-MMM

P1_9-BLUE_LED	R68 750ohms	3	Blue
P1_10-SCT4-LED_GREEN	R69 1.5Kohms	4	Green
P0_29-CT32B0_MAT3-RED	R73 750ohms	1	Red

TP2 DNI 5011 — GND TP 1 — GND

TP3 DNI — Test point 0.036

JS18 — Y1 SSPT7F-12.5PF20-R 32.768k — C25 18pF 50V 5% — C24 18pF 50V 5% — GND

JS17

WAKEUP

KMR221GLFS SW1 — Shld, 5, 2, 3, 4, 1 — GND, GND, NC, NC

VDD_LPC5411x — DNI R2 100Kohms — R1 100ohms — BRIDGE_SDA-WAKEUP

VDD_LPC5411x_IC — JS9 — JP7 DNI HDR-1x02 — R20 DNI 100Kohms — nRESET_ULP — nRESET_TRGT

U11 — LPC5411x_LQFP64_USB / LPC5411x_LQFP64

SHT 2	TO_MUX_P0_0-ISP_RX	31	P0_0/FC0_RXD_SDA_/FC3_CTS_SDA_SSELN0/CT0CAP0/SCT0_OUT3
SHT 2, 5	P0_1-ISP_TX	32	P0_1/FC0_TXD_SCL_MISO/FC3_RTS_SCL_SSELN1/CT0CAP1/SCT0_OUT1
SHT 6	P0_2-GPIO_SPI_CS	36	P0_2/FC0_CTS_SDA_SSELN0/FC2_SSELN3/CT2CAP1
SHT 6	P0_3-GPIO_SPI_CS	37	P0_3/FC0_RTS_SCL_SSELN1/FC2_SSELN2/CT1MAT3
SHT 3, 5	BRIDGE_T_INTR-ISP1	38	P0_4/FC0_SCK/FC3_SSELN2/CT0CAP2
SHT 6	P0_5-FC6_RXD_SDA_MOSI_DATA	39	P0_5/FC6_RXD_SDA_MOSI/SCT0_OUT6/CT0MAT0
SHT 6	P0_6-FC6_TXD_SCL_MISO_FRAME	40	P0_6/FC6_TXD_SCL_MISO//CT0MAT1/UTICK_CAP0
SHT 6	P0_7-FC6_SCK	41	P0_7/FC6_SCK/SCT0_OUT0/CT0MAT2/CT0CAP2
SHT 6	P0_8-FC2_RXD_SDA_MOSI	43	P0_8/FC2_RXD_SDA_MOSI/SCT0_OUT1/CT0MAT3
SHT 6	P0_9-FC2_TXD_SCL_MISO	44	P0_9/FC2_TXD_SCL_MISO/SCT0_OUT2/CT3CAP0/FC3_CTS_SDA_SSELN0
SHT 6	P0_10-FC2_SCK-CT32B3_MAT0	45	P0_10/FC2_SCK/SCT0_OUT3/CT3MAT0
SHT 6	BRIDGE_T_SCK	46	P0_11/FC3_SCK/FC6_RXD_SDA_MOSI/CT2MAT1
SHT 3, 5	BRIDGE_T_MOSI	47	P0_12/FC3_RXD_SDA_MOSI/FC6_TXD_SCL_MISO/CT2MAT3
SHT 3, 5	BRIDGE_T_MISO	48	P0_13/FC3_TXD_SCL_MISO/SCT0_OUT4/CT2MAT0
SHT 3, 5	BRIDGE_T_SSEL-SPIFI_IO3	49	P0_14/FC3_CTS_SDA_SSELN0/SCT0_OUT5/CT2MAT1/FC1_SCK//SPIFI_
SHT 3, 5, 6	TDO-SWO_TRGT-SPIFI_IO2	50	P0_15/FC3_RTS_SCL_SSELN1/SWO/CT2MAT2/FC4_SCK//SPIFI_IO2
SHT 2, 6	TCK-SWDCLK_TRGT-SPIFI_IO1	52	P0_16/FC3_SSELN2/FC6_CTS_SDA_SSELN0/CT3MAT1/SWCLK//SPIFI_1
SHT 2, 6	IF_TMS_SWDIO-SPIFI_IO0	53	P0_17/FC3_SSELN3/FC6_RTS_SCL_SSELN1/CT3MAT2/SWDIO//SPIFI_0
SHT 2, 6	P0_18-FC5_TXD_SCL_MISO	58	P0_18/FC5_TXD_SCL_MISO/SCT0_OUT0/CT0MAT0
SHT 5, 6	P0_19-FC5_SCK-SPIFI_CSn	59	P0_19/FC5_SCK/SCT0_OUT1/CT0MAT1///SPIFI_CSN
SHT 5, 6	P0_20-FC5_RXD_SDA_MOSI	60	P0_20/FC5_RXD_SDA_MOSI/FC0_SCK/CT3CAP0
SHT 5, 6	P0_21-CLKOUT-SPIFI_CLK	61	P0_21/CLKOUT/FC0_TXD_SCL_MISO/CT3MAT0///SPIFI_CLK
SHT 6	P0_22-BRIDGE_GPIO	63	P0_22/CLKIN/FC0_RXD_SDA_MOSI/CT3MAT3
SHT 5	BRIDGE_SCL	1	P0_23/FC1_RTS_SCL_SSELN1//CT0CAP0/UTICK_CAP1
SHT 1, 5	BRIDGE_SDA-WAKEUP	2	P0_24/FC1_CTS_SDA_SSELN0//CT0CAP1/CT0MAT0
SHT 1, 5	P0_25-FC4_SCLX	3	P0_25/FC4_RTS_SCL_SSELN1/FC6_CTS_SDA_SSELN0/CT0CAP2/CT1CP1
SHT 5, 6	P0_26-FC4_SDAX	4	P0_26/FC4_CTS_SDA_SSELN0//CT0CAP3
SHT 3	USB_DP	5	USB_DP
SHT 3	USB_DM	6	USB_DM
SHT 6	P0_29-CT32B0_MAT3-RED	11	P0_29/FC1_RXD_SDA_MOSI/SCT0_OUT2/CT0MAT3/CT0CAP1//CT0MAT1
SHT 6	P0_30-ADC1	12	P0_30/FC1_TXD_SCL_MISO/SCT0_OUT3/CT0MAT2/CT0CAP2
SHT 2, 5, 6	P0_31-PDM0_CLK-ISP0_EN	13	P0_31/PDM0_CLK/FC2_CTS_SDA_SSELN0/CT2CAP2/CT0CAP3/CT0MAT3

R49 33ohms — R35 33ohms

		33	RTCXIN
		35	RTCXOUT
P1_0/PDM0_DATA/FC2_RTS_SCL_SSELN1/CT3MAT1//CT0CAP0	P1_0-PDM0_DATA-CT32B3_MAT1	14	SHT 6
P1_1//SWO/SCT0_OUT4/FC5_SSELN2/FC4_TXD_SCL_MISO	P1_1-FC5_SSEL2	15	SHT 6
P1_2/MCLK/FC7_SSELN3/SCT0_OUT5/FC5_SSELN3/FC4_RXD_SDA_MOSI	P1_2-FC5_SSEL3	16	SHT 5, 6
P1_3//FC7_SSELN2/SCT0_OUT6//FC3_SCK/CT0CAP1/USB0_LEDN	P1_3-FC7_SSEL2-CT32B0_CAP1	17	SHT 6
P1_4/PDM1_CLK/FC7_RTS_SCL_SSELN1/SCT0_OUT7//FC3_TXD_SCL_MISO/	P1_4-ADC7-PDM1_CLK-FC7_RTS-FC3_TXD	18	SHT 6
P1_5/PDM1_DATA/FC7_CTS_SDA_SSELN0/CT1CAP0//CT1MAT3/PVT_AM0_ALRT/	P1_5-ADC8-PDM1_DAT-FC7_CTS	19	SHT 6
P1_6//FC7_SCK/CT1CAP2//CT1MAT2/PVT_RED0_ALERT/USB0_VBUS	P1_6-FC7_SCK-USB_VBUS	26	SHT 6
P1_7//FC7_RXD_SDA_MOSI/CT1MAT2//CT1CAP2/PVT_AMBER1_ALERT	P1_7-FC7_RXD_SDA_MOSI_DATA	27	SHT 3, 6
P1_8//FC7_TXD_SCL_MISO/CT1MAT3//CT1CAP3/PVT_RED1_ALERT	P1_8-ADC11-FC7_TXD_SCL_MISO_FRAME	28	SHT 6
P1_9//FC3_RXD_SDA_MOSI/CT0CAP2///USB0_LEDN/USB0_CONNECTN	P1_9-BLUE_LED	29	SHT 6
P1_10//FC6_TXD_SCL_MISO/SCT0_OUT4/FC1_SCK///USB0_FRAME	P1_10-SCT4-LED_GREEN	30	SHT 6
P1_11//FC6_RTS_SCL_SSELN1/CT1CAP0/FC4_SCK///USB0_VBUS	P1_11-FC6_RTS_SSEL1-MAG_DRDY	42	SHT 6
P1_12//FC5_RXD_SDA_MOSI/CT1MAT0/FC7_SCK/UTICK_CAP2	P1_12-CT32B1_MAT0-ACCI_INT1	51	SHT 6
P1_13//FC5_TXD_SCL_MISO/CT1MAT1/FC7_RXD_SDA_MOSI	P1_13-CT32B1_MAT1	54	SHT 6
P1_14//FC2_RXD_SDA_MOSI/SCT0_OUT7/FC7_TXD_SCL_MISO	P1_14-SCTO7	57	SHT 6
P1_15/PDM0_CLK/SCT0_OUT5/CT1CAP3/FC7_CTS_SDAX_SSELN0	P1_15-SCTO5-FC7_CTS	62	SHT 6
P1_16/PDM0_DATA/CT0MAT0/CT0CAP0/FC7_RTS_SCLX_SSELN1	P1_16-CT32B0_MAT0-GYRO_INT1	7	SHT 6
P1_17////MCLK/UTICK_CAP3	P1_17-IR_LEARN_EN	10	SHT 6
VDD_0		8	
VDD_1		24	
VDD_2		34	
VDD_3		56	
VDDA		23	
VREFP		22	
VSS_0		9	
VSS_1		25	
VSS_2		55	
VSSA		20	
VREFN		21	

VDD_LPC5411x_IC — FB2 — C5 0.01uF — C51 47pF — C16 0.01uF — C40 0.1uF — C17 1uF — C50 0.1uF — C49 0.01uF — SJ2 — GND

SJ1 — C48 0.01uF — GND

P4 DNI HDR-1x03

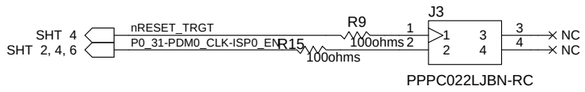
VDD_LPC5411x — P0_26-FC4_SDAX — R8 2.2Kohms — P0_25-FC4_SCLX — R7 2.2Kohms

CONTRACT NO.	Target LPC5411x LQFP64
APPROVALS / DATE	**NXP** Semiconductors
DRAWN d.consiglio 4/21/2015	411 E. Plumeria Dr
CHECKED	San Jose, CA 95134
ISSUED 05/06/15	www.standardics.nxp.com/microcontrollers/
SIZE D / FSCM NO. / DWG. NO. LPCX5411x QFP64 / REV A1	
SCALE	SHEET 4 OF 06

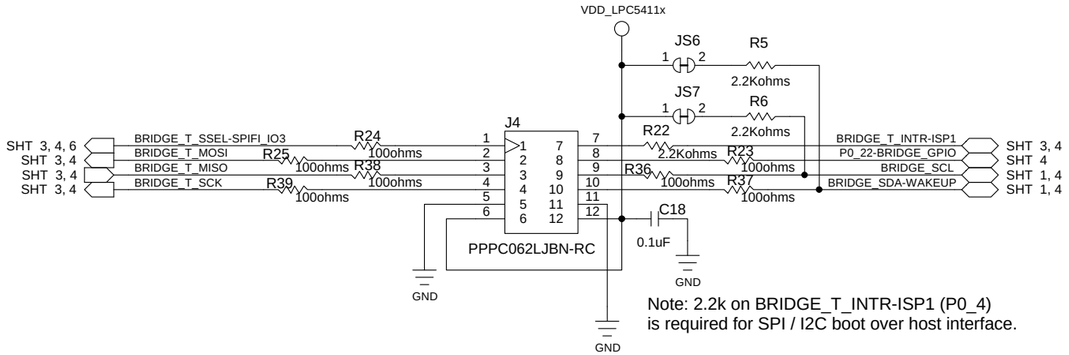
H=8ND; V=4LA

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

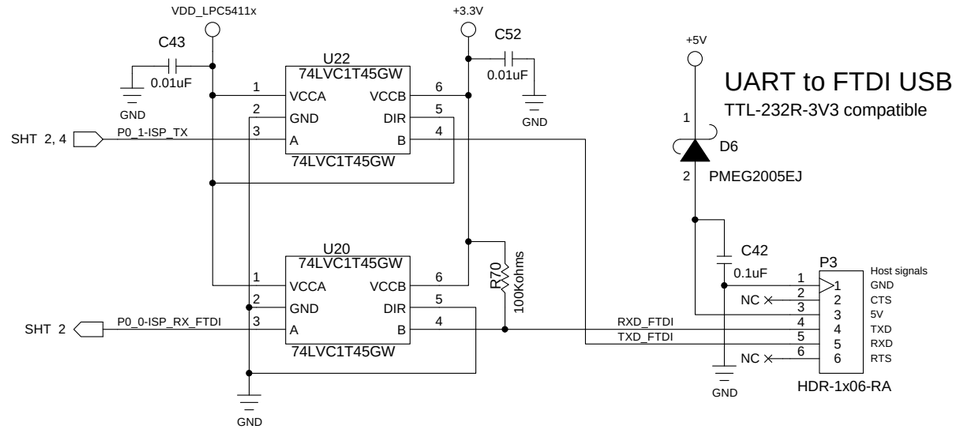
LPC5411x AP control port
(AP must drive open-drain)



SPI / I2C bridge header (Pmod compatible)



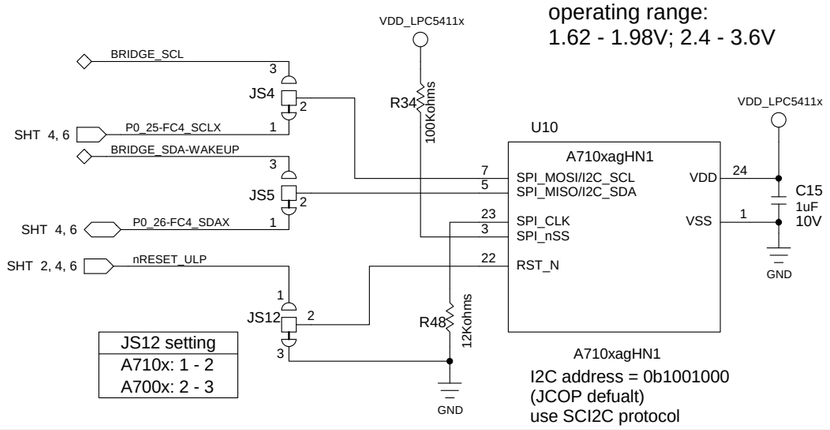
Note: 2.2k on BRIDGE_T_INTR-ISP1 (P0_4)
is required for SPI / I2C boot over host interface.



UART to FTDI USB
TTL-232R-3V3 compatible

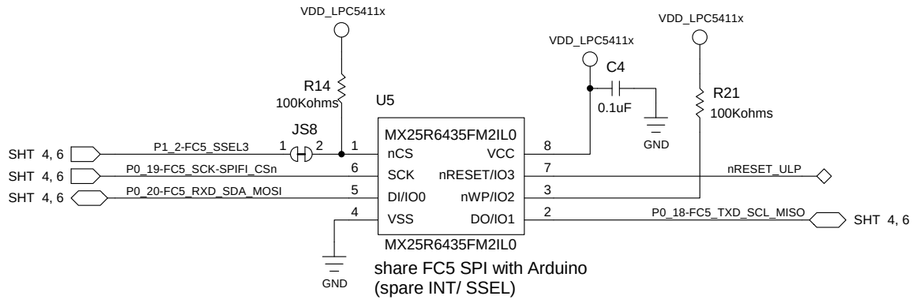
NXP A700x / A71x secure MCU

operating range:
1.62 - 1.98V; 2.4 - 3.6V



JS12 setting
A710x: 1 - 2
A700x: 2 - 3

A710xagHN1
I2C address = 0b1001000
(JCOP defualt)
use SCI2C protocol



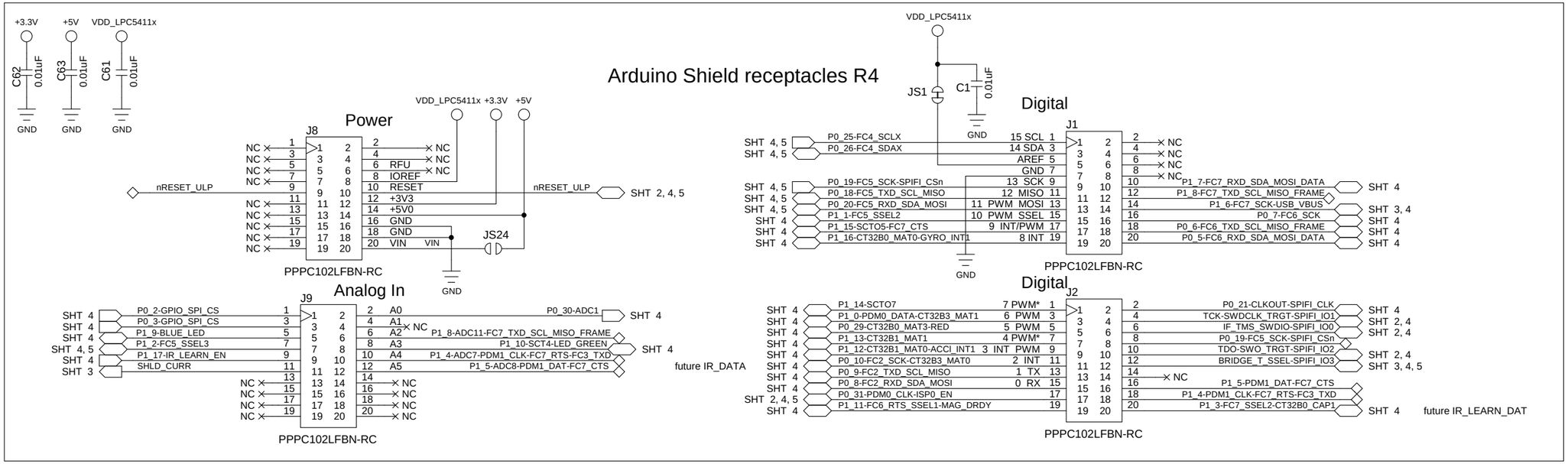
share FC5 SPI with Arduino
(spare INT/ SSEL)

CONTRACT NO.		Pmod / FTDI / SecElem / SPI Flash
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
DRAWN d.consiglio	4/21/2015	
CHECKED		
ISSUED	05/06/15	SIZE D | FSCM NO. | DWG. NO. LPCX5411x QFP64 | REV A1
		SCALE | SHEET 5 OF 06

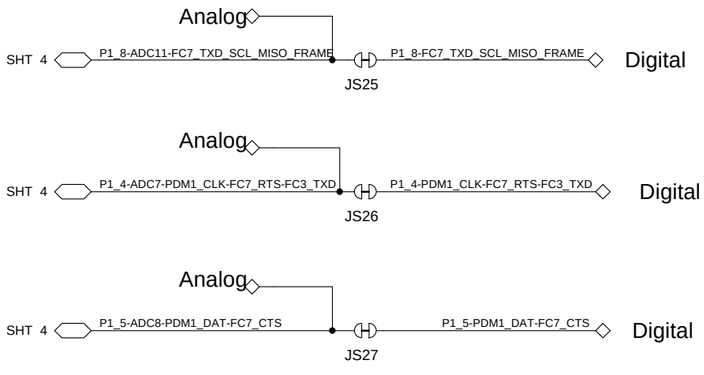
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

Arduino Shield receptacles R4



Board solder jumpers
Digital function by default



CONTRACT NO.		Arduino Interface
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	4/21/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	05/06/15	SIZE D | FSCM NO. | DWG. NO. LPCX5411x QFP64 | REV A1
		SCALE | SHEET 6 OF 06

H=8ND; V=4LA