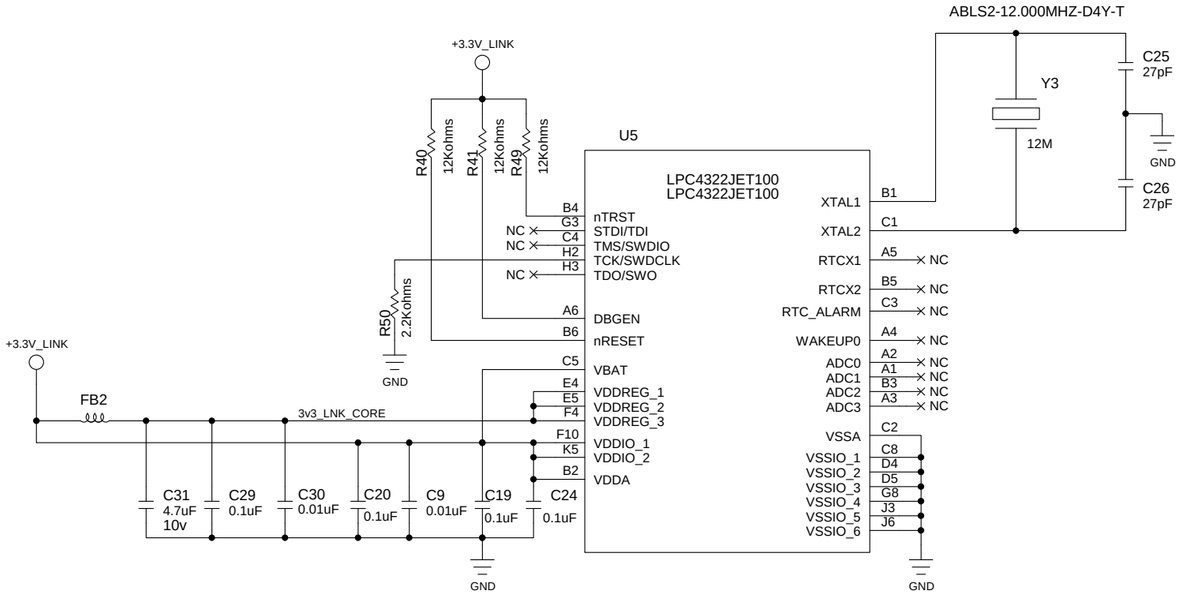
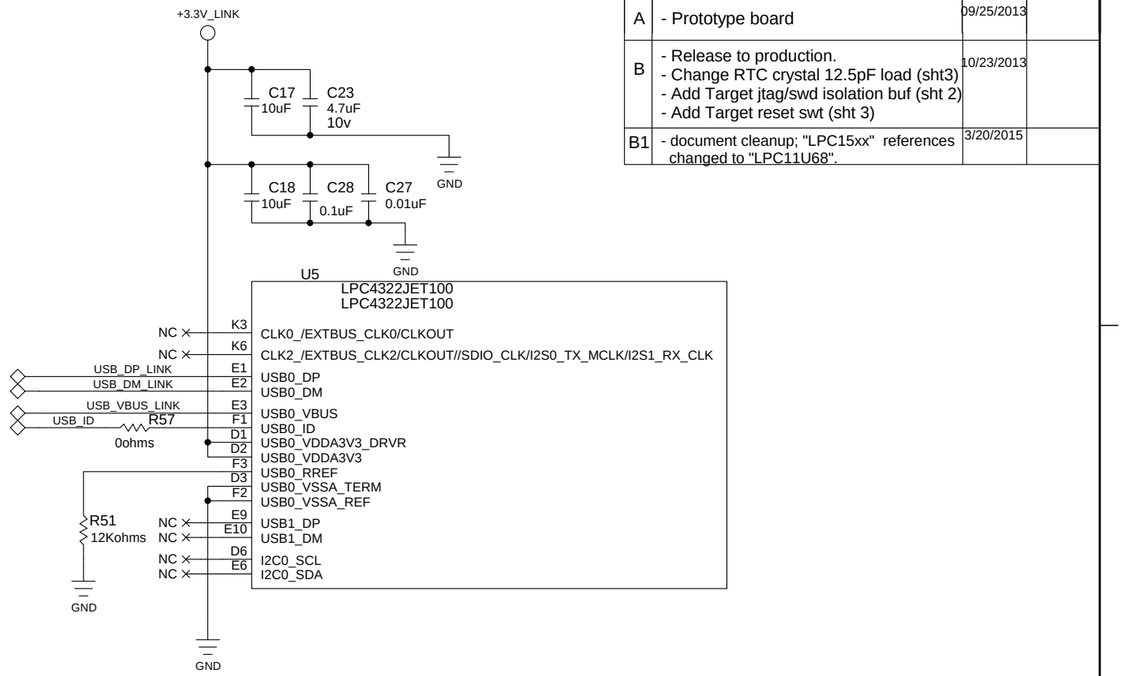
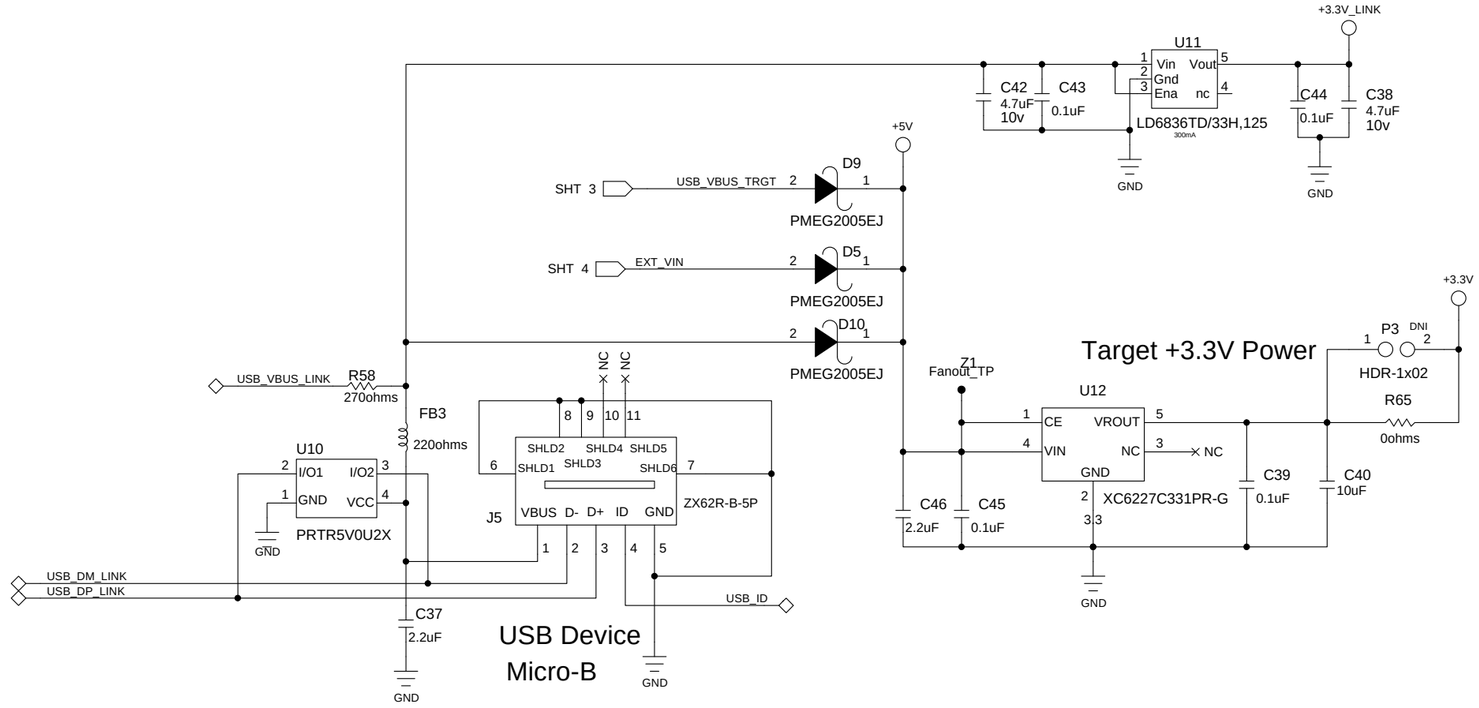
DWG. NO.	SH.	REV
Xpresso-LPC11U68	1	B

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	- Prototype board	09/25/2013	
B	- Release to production. - Change RTC crystal 12.5pF load (sht3) - Add Target jtag/swd isolation buf (sht 2) - Add Target reset swt (sht 3)	10/23/2013	
B1	- document cleanup; "LPC15xx" references changed to "LPC11U68".	3/20/2015	







CONTRACT NO.		LINK2 LPC4322
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
DRAWN d.consiglio	3/20/2015	
CHECKED		
ISSUED	10/23/13	SIZE D | FSCM NO. | DWG. NO. Xpresso-LPC11U68 | REV B
		SCALE | SHEET 1 OF 04

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U5
LPC4322JET100
LPC4322JET100

P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1
P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

TRACE_D0 G2
TRACE_D1 G1
NC H1
BOOT0_LED K2
BOOT1 K1
NC J1
NC J2
TMS_SWDIO_TXEN J4
TMS_SWDIO K4
NC G4
NC H5
NC J5
NC H6
NC J7
TRACE_CLK K7
NC H8
TDO_SWO J8
TRACE_D2 K8
TRACE_D3 H9
TCK_SWCLK H10
JTAG_TDI J10
NC K9
NC K10

U5
LPC4322JET100
LPC4322JET100

P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4
P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
P3[3]_//SPI_SCK/SSP0_SCK/SPIFI_SCK
P3[4]_/GPIO1[14]///SPIFI_SIO3
P3[5]_/GPIO1[15]///SPIFI_SIO2
P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

TARGET_UART_RXD G10
TARGET_UART_TXD G7
TARGET_UART_CTRL F5
ISP_CTRL D8
NC D9
JTAG_RESET D10
JTAG_RESET_TXEN G9
BOOT_FLASH C10
BOOT2 C6
BOOT3 B10
NC E8
NC A9
NC B9
IF_DETECT R16 1.5Kohms NC A10
NC A8
NC F7
NC G6
NC A7
NC B8
NC B7
NC C7
NC D7
NC E7

U5
LPC4322JET100
LPC4322JET100

P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

NC H7
NC G5
NC J9
NC F6
NC F9
F8
C9
NC H4

R42 DNI 2.2Kohms
R29 DNI 2.2Kohms
R30 DNI 2.2Kohms
R28 2.2Kohms
GND

+3.3V_LINK
R39 DNI 2.2Kohms
R22 2.2Kohms
R24 DNI 2.2Kohms
R26 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R38 2.2Kohms
R21 DNI 2.2Kohms
R23 2.2Kohms
R25 DNI 2.2Kohms
R27 2.2Kohms
BOOT_FLASH
JP3
HDR-1x02
D2
LS Q976-NR-1
GND

LPC4322 Boot mode
DFU USB0 = B3:0 = 0101

Short JP3 to force DFU boot
(when internal flash is programmed)

Buffer Pwr Select (JP2)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

+3.3V_LINK
R8 100Kohms
U4
VCCA VCCB
A0 B0
A1 B1
DIR GND
SN74AVC2T45DCTR
SN74AVC2T45DCTR
TCK_SWCLK
JTAG_TDI
R31 100ohms IF_SWCLK
R32 100ohms IF_JTAG_TDI
C10 0.1uF
GND

+3.3V
M1
JP2
HDR-1x03
D1
PMEG1020EJ

U6
74LVC1T45GW
VCCA VCCB
GND DIR
A B
74LVC1T45GW
TDO_SWO
C14 0.1uF
R44 100Kohms
IF_SWO

U8
74LVC1T45GW
TMS_SWDIO
C15 0.1uF
R52 100Kohms
R53 100ohms IF_SWDIO

TMS_SWDIO_TXEN
R54 2.2Kohms

U1
74LVC1T45GW
JTAG_RESET
C1 0.1uF
R1 100Kohms
R2 100ohms IF_RST

JTAG_RESET_TXEN
R3 2.2Kohms

Target (LPC11U68)
SWD Debug

C5 10uF
P1
FTSH-105-01-L-DV-K
IF_SWDIO
IF_SWCLK
IF_SWO
IF_JTAG_TDI
IF_RST
IF_DETECT
R7 0ohms

+3.3V_LINK
U2
VCC
ISP_CTRL
R6 100ohms IF_ISPEN
SHT 3, 4
74LVC1G07GW

+3.3V
R18 100Kohms
U13
VDD
1S 1Z SWCLK-PIO0_10 SHT 3
1Y0 1Y1
2S 2Z RESET-PIO0_0 SHT 3, 4
2Y0 2Y1
GND
IF_SWCLK
IF_RST
JP1
HDR-1X02
NX3L2267GU,115

Target to debug location (JP1)
On-board Target - open (default)
Off-board Target - short

+3.3V
U9
VDD
SEL
Y0
Y1
GND
Z
TARGET_UART_CTRL
PIO0_18-ISP_RX
TARGET_UART_RXD
SHT 4
TO_MUX_PIO0_18-ISP_RX SHT 3
R55 2.2Kohms
74LVC1G3157GW

TRACE_CLK R13 DNI 0ohms NC
TRACE_D0 R12 DNI 0ohms NC
TRACE_D1 R11 DNI 0ohms NC
TRACE_D2 R14 DNI 0ohms NC
TRACE_D3 R15 DNI 0ohms NC

LPC11U68 Target
does not have trace.

TARGET_UART_TXD R43 100ohms PIO0_19-ISP_TX SHT 3, 4

CONTRACT NO.		LINK LPC4320	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	3/20/2015		
CHECKED			
ISSUED	10/23/13	SIZE D / FSCM NO. / DWG. NO. Xpresso-LPC11U68 / REV B	
		SCALE	SHEET 2 OF 04

H=8N0; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

USB Device Micro-B

J3 ZX62R-B-5P — GND, ID, D+, D-, VBUS; SHLD1–SHLD6; NC

U3 PRTR5V0U2X — I/O2, I/O1, VCC, GND

R48 470ohms — PIO0_3-VBUS

C13 0.1uF, R37 2.2Kohms

SHT 1 USB_VBUS_TRGT

RESET-PIO0_0

U7 LPC11U68JBD100 LPC11U68JBD100

NC	88	nRSTOUT
RESET-PIO0_0	8	RESETn/PIO0_0
	38	USB_DM
	39	USB_DP
SHT 2 SWCLK-PIO0_10	60	SWCLK/PIO0_10//
SHT 2 IF_SWDIO	81	SWDIO/PIO0_15//
	11	VSSIO_1
	53	VSSIO_2
	70	VSSIO_3
	91	GND_1
	7	GND_2
	74	VREFN
	85	VSSA
	12	PIO2_0/XTALIN
	13	PIO2_1/XTALOUT
	5	RTCXIN
	6	RTCXOUT
	14	VDDIO_1
	71	VDDIO_2
	54	VDDIO_3
	93	VDDIO_4
	92	VDDMAIN_EXT
	73	VREFP
	84	VDDA
	99	VBAT

ABLS2-12.000MHZ-D4Y-T — Y1 12M; C3 27pF; C2 27pF

SSPT7F-12.5PF20-R — Y2 32.768k; C6 18pF 50V 5%; C4 18pF 50V 5%

R5 0ohms

C21 0.1uF, C7 0.01uF, C8 0.1uF, C33 0.01uF, C12 0.1uF, C16 0.01uF, C32 0.1uF, C34 0.01uF

FB1; +3.3VA; C35 0.1uF, C36 10uF

C11 0.1uF; +3.3VBAT

D4 1N4448WS-7-F; D3 1N4448WS-7-F; VBAT; SHT 4

R67 12Kohms, R66 2.2Kohms, D6 LS Q976-NR-1 (Red), R19 100ohms; SHT 2, 4 RESET-PIO0_0; C41 0.1uF

SW3 KMR221GLFS

R4 2.2Kohms, R10 2.2Kohms

U7 LPC11U68JBD100 LPC11U68JBD100

SHT 2, 4	IF_ISPEN	9
SHT 4	PIO0_2-SSP0_SSEL	19
	PIO0_3-VBUS	30
	PIO0_4-I2C_SCL	31
SHT 4	PIO0_5-I2C_SDA	32
SHT 4	PIO0_6	44
SHT 4	PIO0_7	45
SHT 4	PIO0_8-SSP0_MISO	58
SHT 4	PIO0_9-SSP0_MOSI	59
SHT 4	PIO0_11-ADC_9	64
SHT 4	PIO0_12-ADC_8	66
SHT 4	PIO0_13-ADC_7	68
SHT 4	PIO0_14-ADC_6	69
	PIO0_16-WAKEUP	82
	PIO0_17	90
SHT 4	TO_MUX_PIO0_18-ISP_RX	94
SHT 2	PIO0_19-ISP_TX	95
SHT 2, 4	PIO0_20	17
SHT 4	PIO0_21	33
SHT 4	PIO0_22	62
SHT 4	PIO0_23-ADC_1	83

		PIO0_1/CLKOUT/CT32B0_MAT2/USB_FTOGGLE
		PIO0_2/SSP0_SSEL/CT16B0_CAP0/R_0
		PIO0_3/USB_VBUS/R_1
		PIO0_4/I2C0_SCL/R_2
		PIO0_5/I2C0_SDA/R_3
		PIO0_6/USB_CONNECTn/SSP0_SCK/R_4
		PIO0_7/U0_CTSn/R_5/I2C1_SCL
		PIO0_8/SSP0_MISO/CT16B0_MAT0/R_6
		PIO0_9/SSP0_MOSI/CT16B0_MAT1/R_7
		TDI/PIO0_11/ADC_9/CT32B0_MAT3/U1_RTSn/U1_SCLK
		TMS/PIO0_12/ADC_8/CT32B1_CAP0/U1_CTSn
		TDO/PIO0_13/ADC_7/CT32B1_MAT0/U1_RXD
		TRSTn/PIO0_14/ADC_6/CT32B1_MAT1/U1_TXD
		PIO0_16/ADC_2/CT32B1_MAT3/R_8/WAKEUP
		PIO0_17/U0_RTSn/CT32B0_CAP0/U0_SCLK
		PIO0_18/U0_RXD/CT32B0_MAT0
		PIO0_19/U0_TXD/CT32B0_MAT1
		PIO0_20/CT16B1_CAP0/U2_RXD
		PIO0_21/CT16B1_MAT0/SSP1_MOSI
		PIO0_22/ADC_11/CT16B1_CAP1/SSP1_MISO
		PIO0_23/ADC_1/R_9/U0_nRI/SSP1_SSEL

U7 LPC11U68JBD100 LPC11U68JBD100

SHT 4	PIO1_0	97
SHT 4	PIO1_1	28
SHT 4	PIO1_2	55
SHT 4	PIO1_3	72
SHT 4	PIO1_4	23
SHT 4	PIO1_5	47
SHT 4	PIO1_6	98
SHT 4	PIO1_7	10
SHT 4	PIO1_8	61
SHT 4	PIO1_9-ADC_0	86
SHT 4	PIO1_10	18
SHT 4	PIO1_11-I2C1_SCL	65
SHT 4	PIO1_12	89
SHT 4	PIO1_13	78
SHT 4	PIO1_14-I2C_SDA	79
SHT 4	PIO1_15	87
SHT 4	PIO1_16	96
SHT 4	PIO1_17	34
SHT 4	PIO1_18	43
SHT 4	PIO1_19	4
SHT 4	PIO1_20-SSP1_SCK	29
SHT 4	PIO1_21-SSP1_MISO	56
SHT 4	PIO1_22-SSP1_MOSI	80
SHT 4	PIO1_23-SSP1_SSEL	35
SHT 4	PIO1_24-CT32B0_MAT0	42
SHT 4	PIO1_25	100
SHT 4	PIO1_26-CT32B0_MAT2	20
SHT 4	PIO1_27-CT32B0_MAT3	22
SHT 4	PIO1_28	46
SHT 4	PIO1_29-SSP0_SCK	63
SHT 4, 4	PIO1_30	67
SHT 4	PIO1_31	48

		PIO1_0/CT32B1_MAT0/R_10/U2_TXD
		PIO1_1/CT32B1_MAT1/R_11/U0_DTRn
		PIO1_2/CT32B1_MAT2/R_12/U1_RXD
		PIO1_3/CT32B1_MAT3/R_13/I2C1_SDA/ADC_5
		PIO1_4/CT32B1_CAP0/R_14/U0_DSRn
		PIO1_5/CT32B1_CAP1/R_15/U0_DCDn
		PIO1_6/R_16/U2_RXD/CT32B0_CAP1
		PIO1_7/R_17/U2_CTSn/CT16B1_CAP0
		PIO1_8/R_18/U1_TXD/CT16B0_CAP0
		PIO1_9/U0_CTSn/CT16B1_MAT1/ADC_0
		PIO1_10/U2_RTSn/U2_SCLK/CT16B1_MAT0
		PIO1_11/I2C1_SCL/CT16B0_MAT2/U0_Rin
		PIO1_12/SSP0_MOSI/CT16B0_MAT1/R_21
		PIO1_13/U1_CTSn/SCT0_OUT3/R_22
		PIO1_14/I2C1_SDA/CT32B1_MAT2/R_23
		PIO1_15/SSP0_SSEL/CT32B1_MAT3/R_24
		PIO1_16/SSP0_MISO/CT16B0_MAT0/R_25
		PIO1_17/CT16B0_CAP1/U0_RXD/R_26
		PIO1_18/CT16B1_CAP1/U0_TXD/R_27
		PIO1_19/U2_CTSn/SCT0_OUT0/R_28
		PIO1_20/U0_DSRn/SSP1_SCK/CT16B0_MAT0
		PIO1_21/U0_DCDn/SSP1_MISO/CT16B0_CAP1
		PIO1_22/SSP1_MOSI/CT32B1_CAP1/ADC_4/R_29
		PIO1_23/CT16B1_MAT1/SSP1_SSEL/U2_TXD
		PIO1_24/CT32B0_MAT0/I2C1_SDA
		PIO1_25/U2_RTSn/U2_SCLK/SCT0_IN0/R_30
		PIO1_26/CT32B0_MAT2/U0_RXD/R_19
		PIO1_27/CT32B0_MAT3/U0_TXD/R_20/SSP1_SCK
		PIO1_28/CT32B0_CAP0/U0_SCLK/U0_RTSn
		PIO1_29/SSP0_SCK/CT32B0_CAP1/U0_DTRn/ADC_10
		PIO1_30/I2C1_SCL/SCT0_IN3/R_31
		PIO1_31

U7 LPC11U68JBD100 LPC11U68JBD100

SHT 4	PIO2_2-SCT0_OUT1	21
SHT 4	PIO2_3-CT32B0_MAT1	36
SHT 4	PIO2_4	41
SHT 4	PIO2_5	15
SHT 4	PIO2_6	37
SHT 4	PIO2_7-SCT0_OUT2	40
SHT 4	PIO2_8	2
SHT 4	PIO2_9	3
SHT 4	PIO2_10	16
SHT 4	PIO2_11	24
SHT 4	PIO2_12	25
SHT 4	PIO2_13	26
SHT 4	PIO2_14	27
SHT 4	PIO2_15	49
SHT 4	PIO2_16-SCT1_OUT0	50
SHT 4	PIO2_17-SCT1_OUT1	51
SHT 4	PIO2_18-SCT1_OUT2	52
SHT 4	PIO2_19-SCT1_OUT3	57
SHT 4	PIO2_20	75
SHT 4	PIO2_21	76
SHT 4	PIO2_22	77
SHT 4	PIO2_23	1

		PIO2_2/U3_RTSn/U3_SCLK/SCT0_OUT1
		PIO2_3/U3_RXD/CT32B0_MAT1
		PIO2_4/U3_TXD/CT32B0_MAT2
		PIO2_5/U3_CTSn/SCT0_IN1
		PIO2_6/U1_RTSn/U1_SCLK/SCT0_IN2
		PIO2_7/SSP0_SCK/SCT0_OUT2
		PIO2_8/SCT1_IN0
		PIO2_9/SCT1_IN1
		PIO2_10/U4_RTSn/U4_SCLK
		PIO2_11/U4_RXD
		PIO2_12/U4_TXD
		PIO2_13/U4_CTSn
		PIO2_14/SCT1_IN2
		PIO2_15/SCT1_IN3
		PIO2_16/SCT1_OUT0
		PIO2_17/SCT1_OUT1
		PIO2_18/SCT1_OUT2
		PIO2_19/SCT1_OUT3
		PIO2_20
		PIO2_21
		PIO2_22
		PIO2_23

RGB LED

D8 LED_RGB_PLCC4 (Blue, Green, Red); +3.3V

PIO2_18-SCT1_OUT2 — R61 270ohms

PIO2_16-SCT1_OUT0 — R59 270ohms

PIO2_17-SCT1_OUT1 — R60 1.5Kohms

WAKEUP

KMR221GLFS SW1; R63 100Kohms; R62 100ohms; PIO0_16-WAKEUP

Bootload Enable

KMR221GLFS SW2; R64 100ohms; IF_ISPEN

ISP Boot Modes		
Mode	PIO0_1	PIO0_3
No ISP (Flash)	high	X
USB	low	high
UART0	low	low

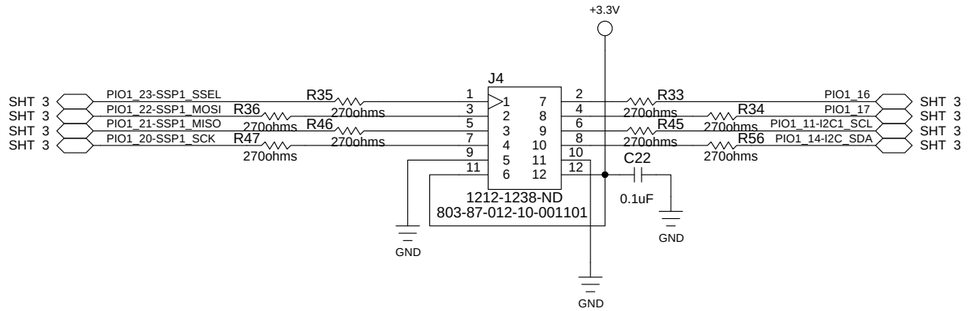
CONTRACT NO.		Target LPC1U68	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	3/20/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED			
ISSUED	10/23/13	SIZE D / FSCM NO. / DWG. NO. Xpresso-LPC11U68 / REV B	
		SCALE	SHEET 3 OF 04

H=8ND; V=4LA

REVISIONS

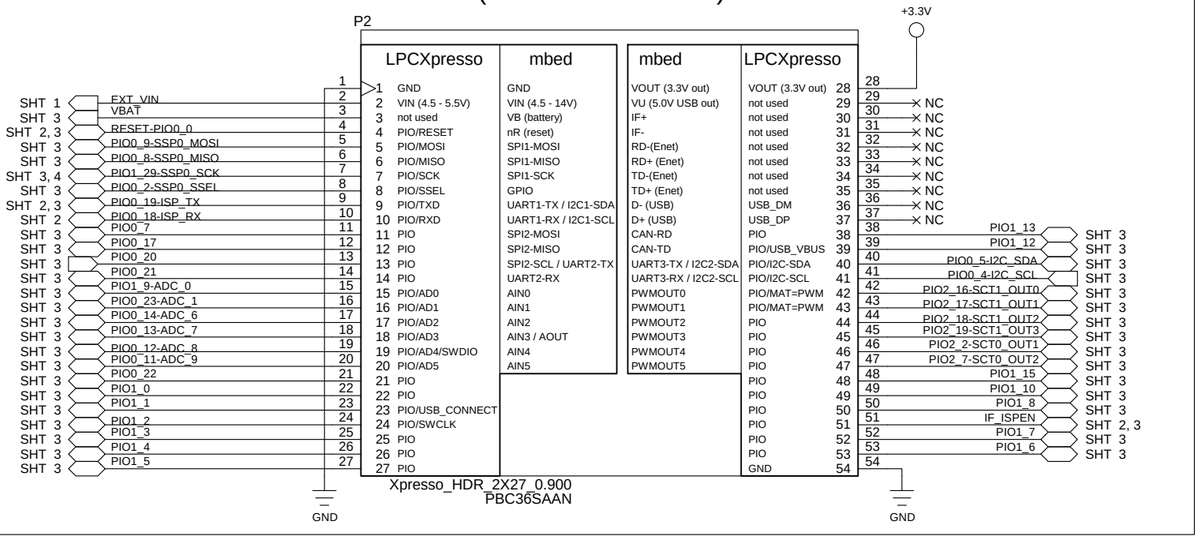
REV	DESCRIPTION	DATE	APPROVED

PMOD compatible header

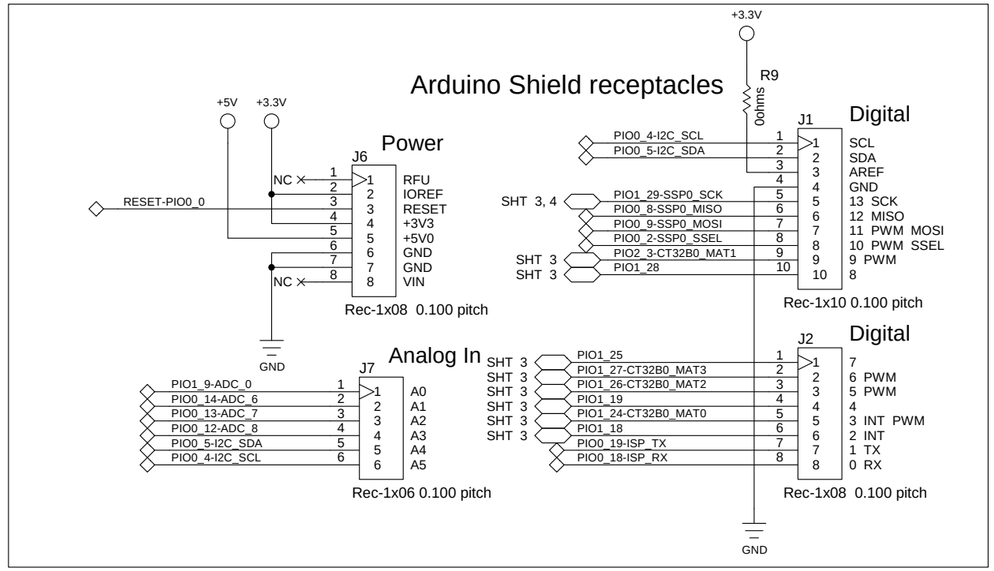


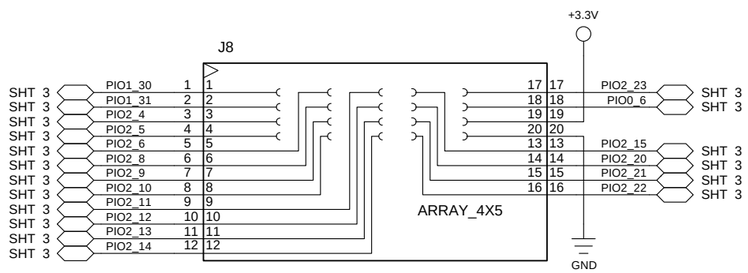
PMOD pin function	LPC11U68 supported function
Pin 1: GPIO/SPI-SSEL(out)/UART-CTS(in)	GPIO/SPI-SSEL(out)
Pin 2: GPIO/SPI-MOSI(out)/UART-TXD(out)	GPIO/SPI-MOSI(out)
Pin 3: GPIO/SPI-MISO(in)/UART-RXD(in)	GPIO/SPI-MISO(in)
Pin 4: GPIO/SPI-SCK(out)/UART-RTS(out)	GPIO/SPI-SCK(out)
Pin 5: GND	GND
Pin 6: VCC(3.3V)	VCC(3.3V)
Pin 7: GPIO/INT(in)	GPIO/INT(in)
Pin 8: GPIO/RESET(out)	GPIO/RESET(out)
Pin 9: GPIO	GPIO
Pin 10:GPIO	GPIO
Pin 11:GND	GND
Pin 12:VCC(3.3V)	VCC(3.3V)

LPCXpresso brd header (Bottom side of PCB)



Arduino Shield receptacles





CONTRACT NO.		Xpresso MC/Arduino/PMOD headers	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	3/20/2015		
CHECKED			
ISSUED	10/23/13	SIZE D / FSCM NO. / DWG. NO. Xpresso-LPC11U68	REV B
		SCALE	SHEET 4 OF 04

H=8N0; V=4LA