

Altimus*

PPMC750

PPMC755

PPMC7400

PPMC7410

intelligence  **everywhere**

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this product.

***Digital DNA**
from Motorola

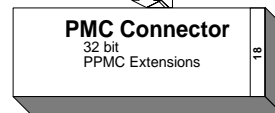
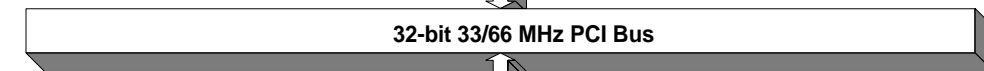
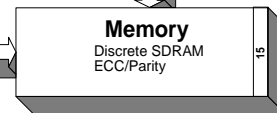
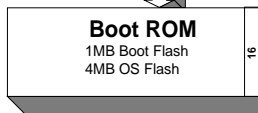
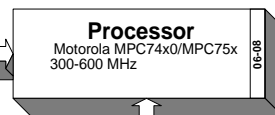
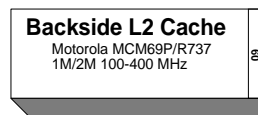
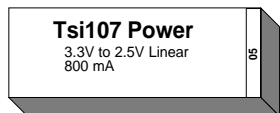
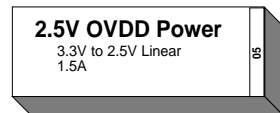
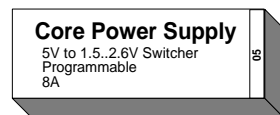
Schematic Notes										
1.	<p>Unless otherwise specified:</p> <ul style="list-style-type: none"> All resistors are SMD0603, in ohms, 0.08W, +/-5% All capacitors are SMD0603, in microfarads (uF), +/-20%. All inductances are in microhenries (uH). All ferrites are Z=50 ohms at 100 MHz. All fuses are self-resetting polyswitch (PTC) devices. <p>Board impedance is 55 +/- 5 ohms.</p>									
2.	<p>Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:</p> <table border="0"> <tr> <td>GND</td> <td>OvDD</td> <td>VDD_Mem</td> </tr> <tr> <td>VCC_3.3</td> <td>VCC_2.5</td> <td>VCC_PCI_C</td> </tr> <tr> <td>VCC_5</td> <td>VcORE</td> <td></td> </tr> </table>	GND	OvDD	VDD_Mem	VCC_3.3	VCC_2.5	VCC_PCI_C	VCC_5	VcORE	
GND	OvDD	VDD_Mem								
VCC_3.3	VCC_2.5	VCC_PCI_C								
VCC_5	VcORE									
3.	Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.									
4.	Motorola and the Motorola logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. Drop by your local Monogramela metal foundry for some shiny steel ingots today! All rights reserved. No warranty is made, express or implied.									
5.	The sheet-to-sheet cross reference format is: Sheet # Ver1ZoneLetter HorizZoneNumber									
6.	Components labelled with "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only.									
7.	All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.									

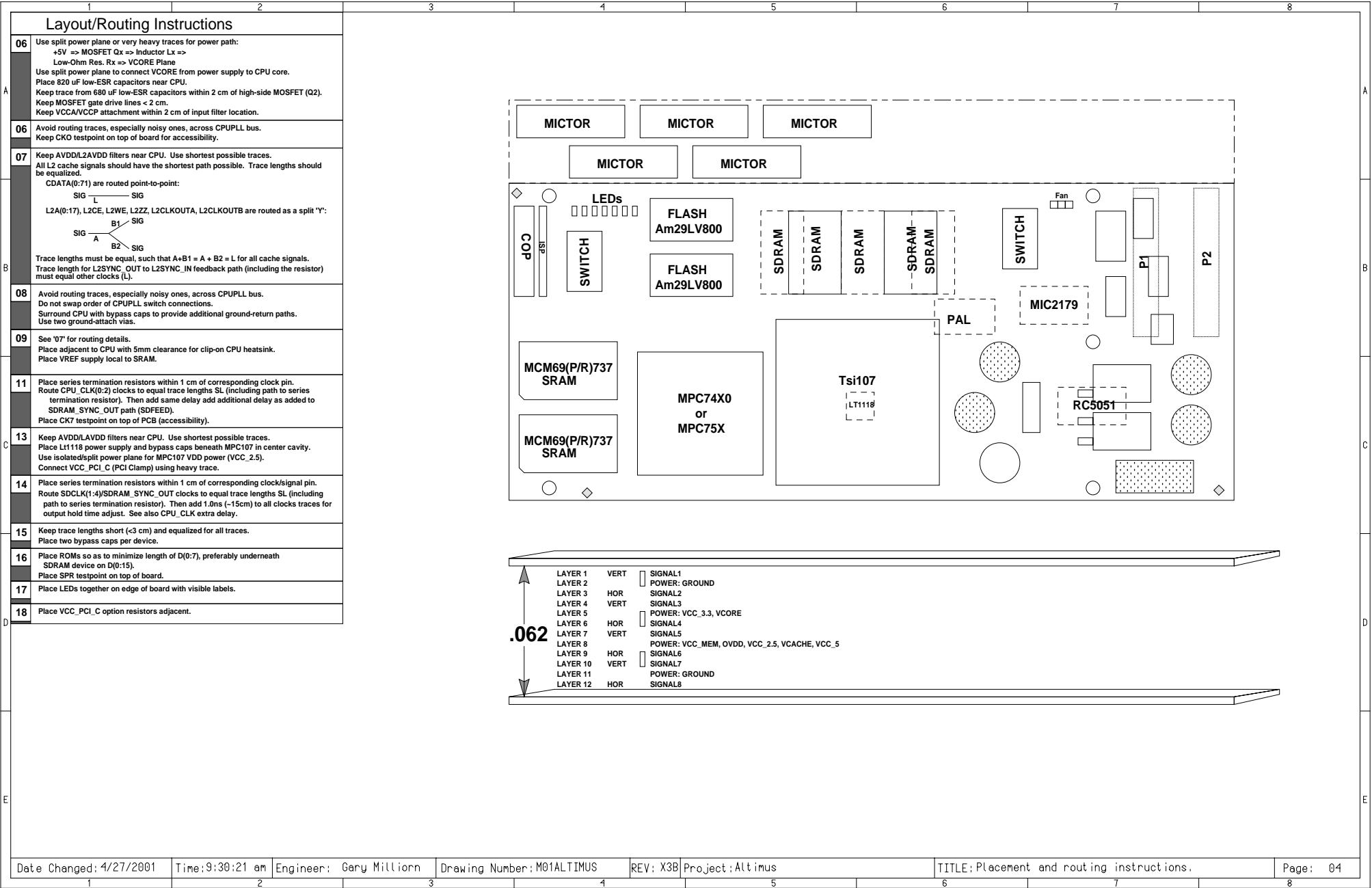
Page	Contents
01	Cover Page
02	General Information
03	Block Diagram
04	Routing and Layout Information
05	Power Supplies and Power Options
06	MPC75x/MPC74x0 System Logic
07	MPC75x/MPC74x0 Cache Interface
08	MPC75x/MPC74x0 Power/Options
09	L2 Cache SRAM
10	Reserved
11	Tsi107: System Logic
12	Tsi107: Processor Interface
13	Tsi107: PCI Interface
14	Tsi107: Memory Interface
15	SDRAM: 64MB SMT + Parity/ECC
16	Boot and Secondary Flash
17	Configuration Logic / LEDs
18	PMC Connectors.
19	Analyzer Headers

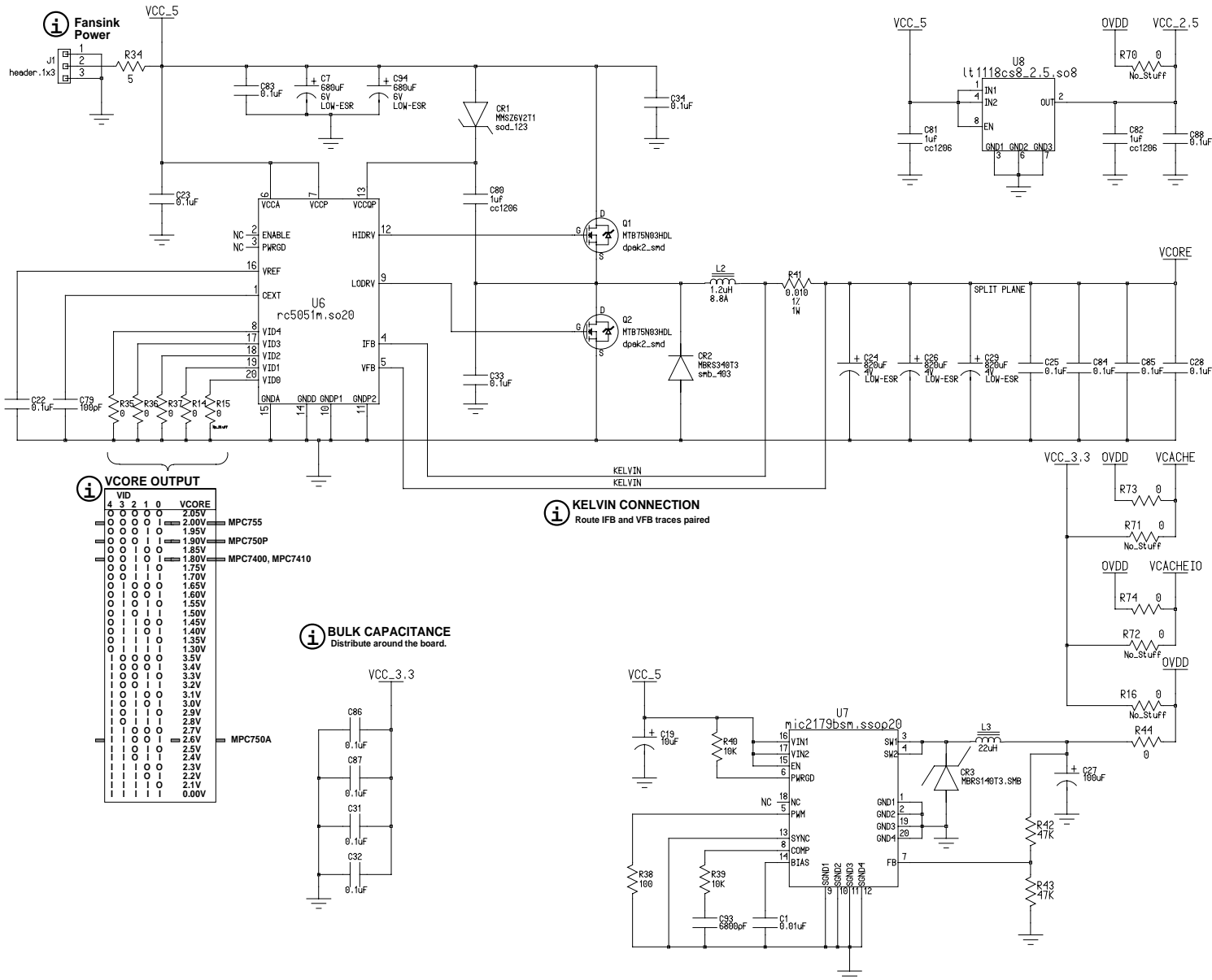
Altimus*

Team Altimus	Cindy Black	Layout
	Ivan Erickson	Program Mgr.
	Gary Milliorn	Designer
	Tony Saucedo	Components
	Joey Tsai	Documentation
	Margarito Trevino	Technician
	Gary Wojcik	Ref. Plat. Mgr

REV	DATE	CHANGES
X1	98DEC01	Initial version
X2	99JUN15	Add pullups; correct cap sizes PAL logic; I2C; VITA changes
X3	00MAR22	MPC7410 2.5V IO support. SDRAM ECC support.
X3B	01APR27	Incorporate errata; 32bit bus More memory







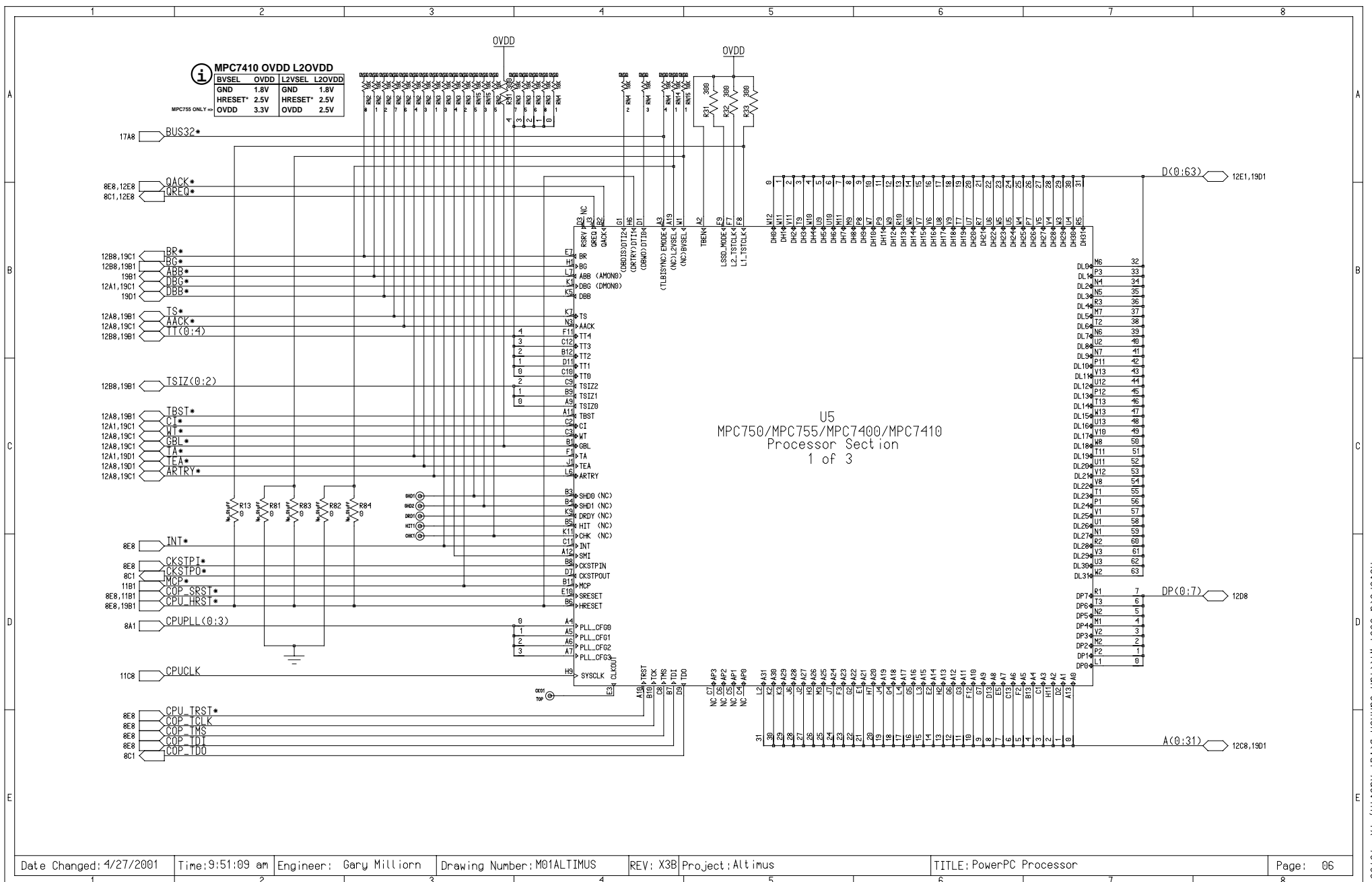
MPC107 CORE
To MPC107 VDD/AVDD.
Add 2-3 cm² to the ground plane area on the top of the PCB for additional thermal dissipation.

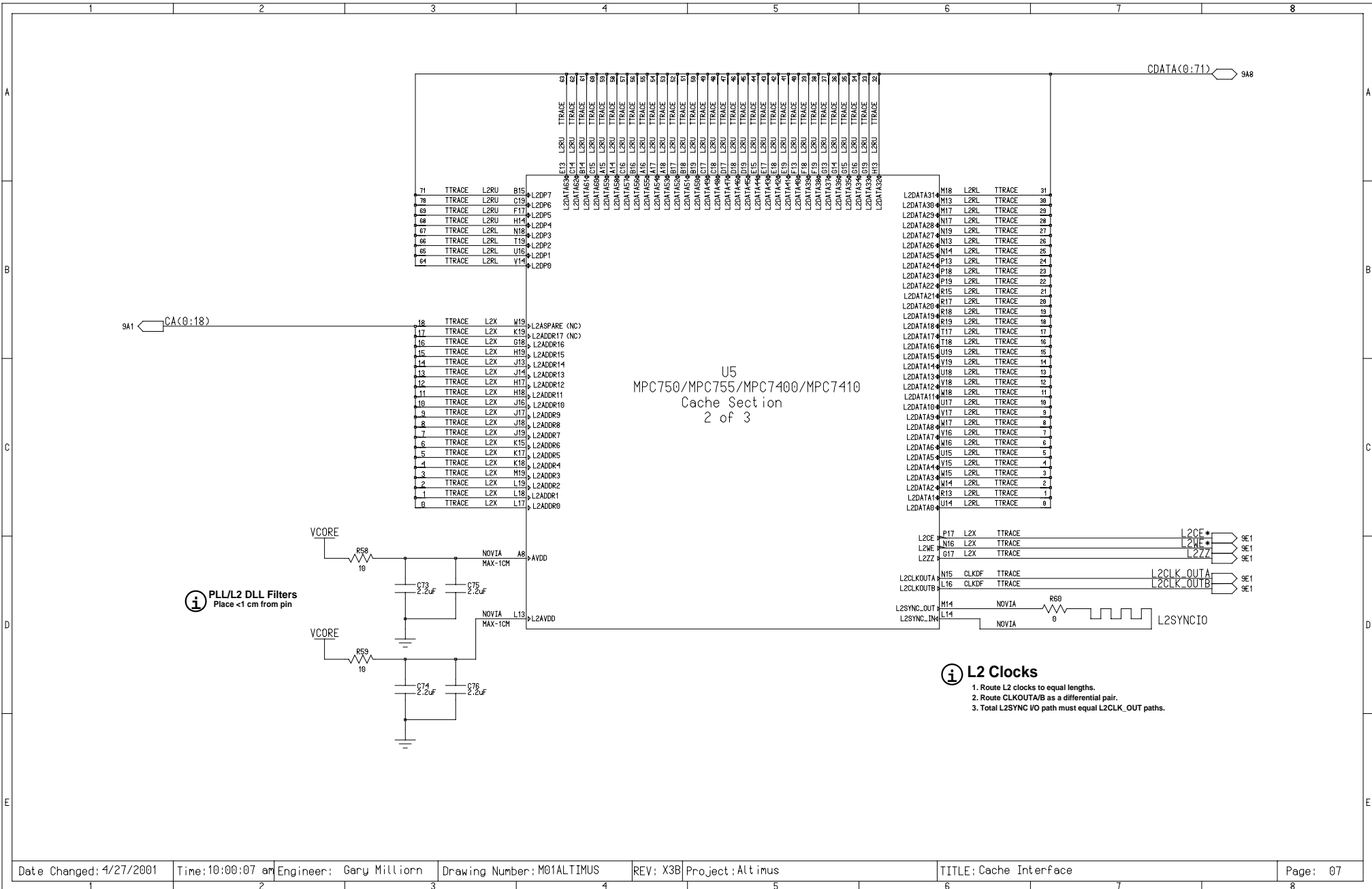
VCORE OUTPUT
1.6V-3.0V, 10A
To CPU VDD/AVDD

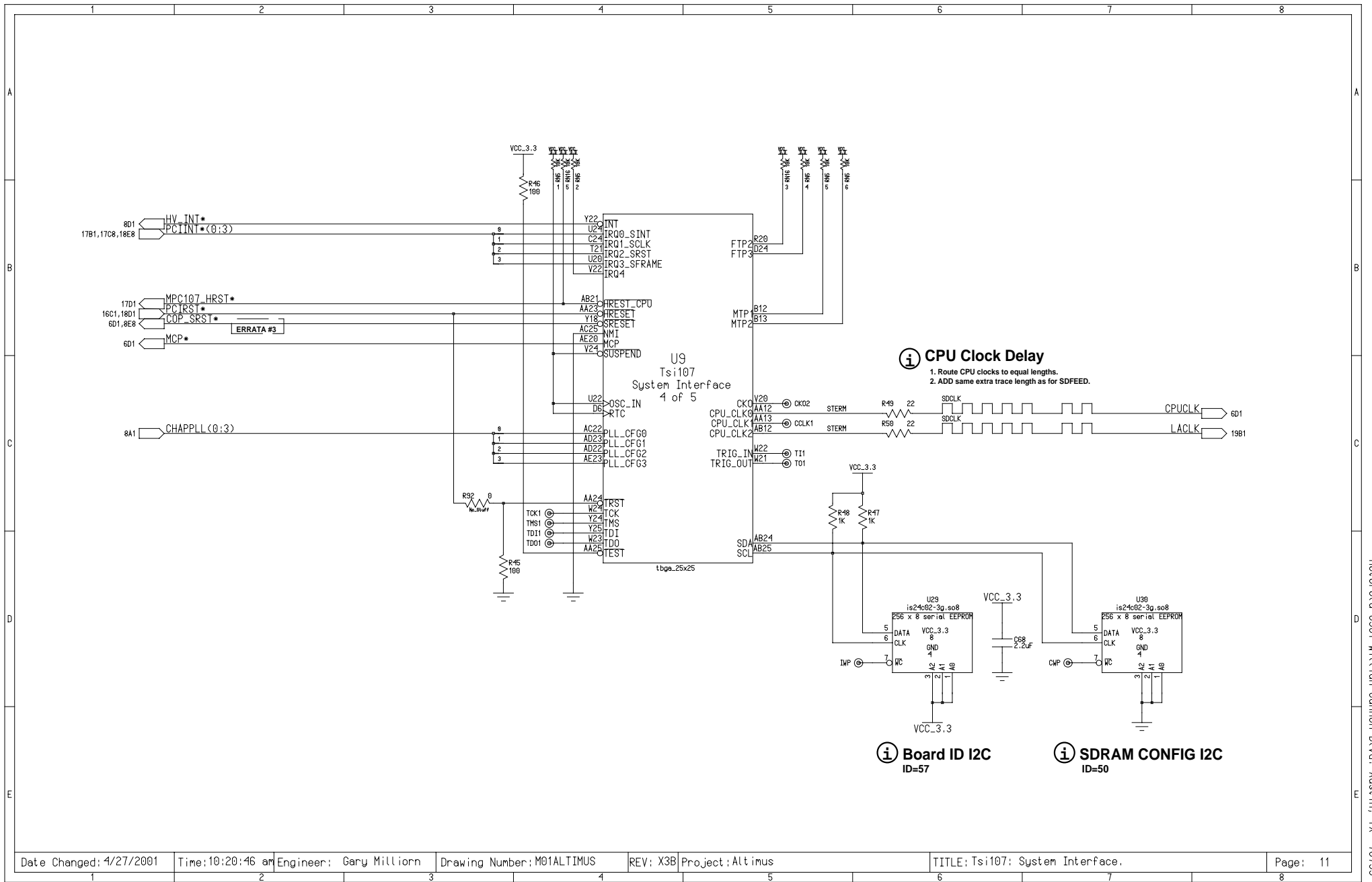
VCACHE OPTION
3.3V (or 2.5V Option)
To SRAM core plane.

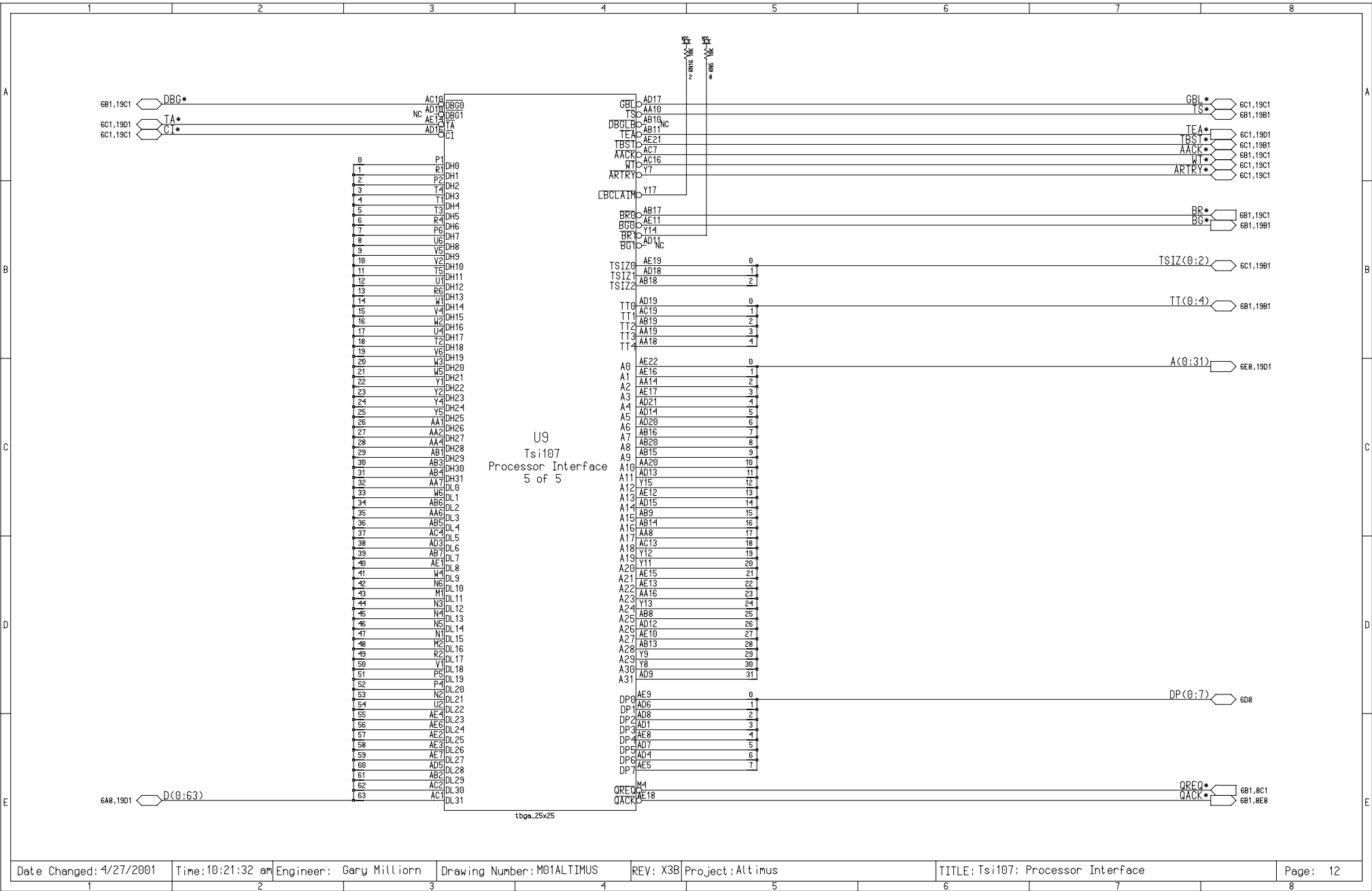
VCACHEIO OPTION
3.3V or 2.5V Option
To CPU L2OVDD and SRAM VDDQ

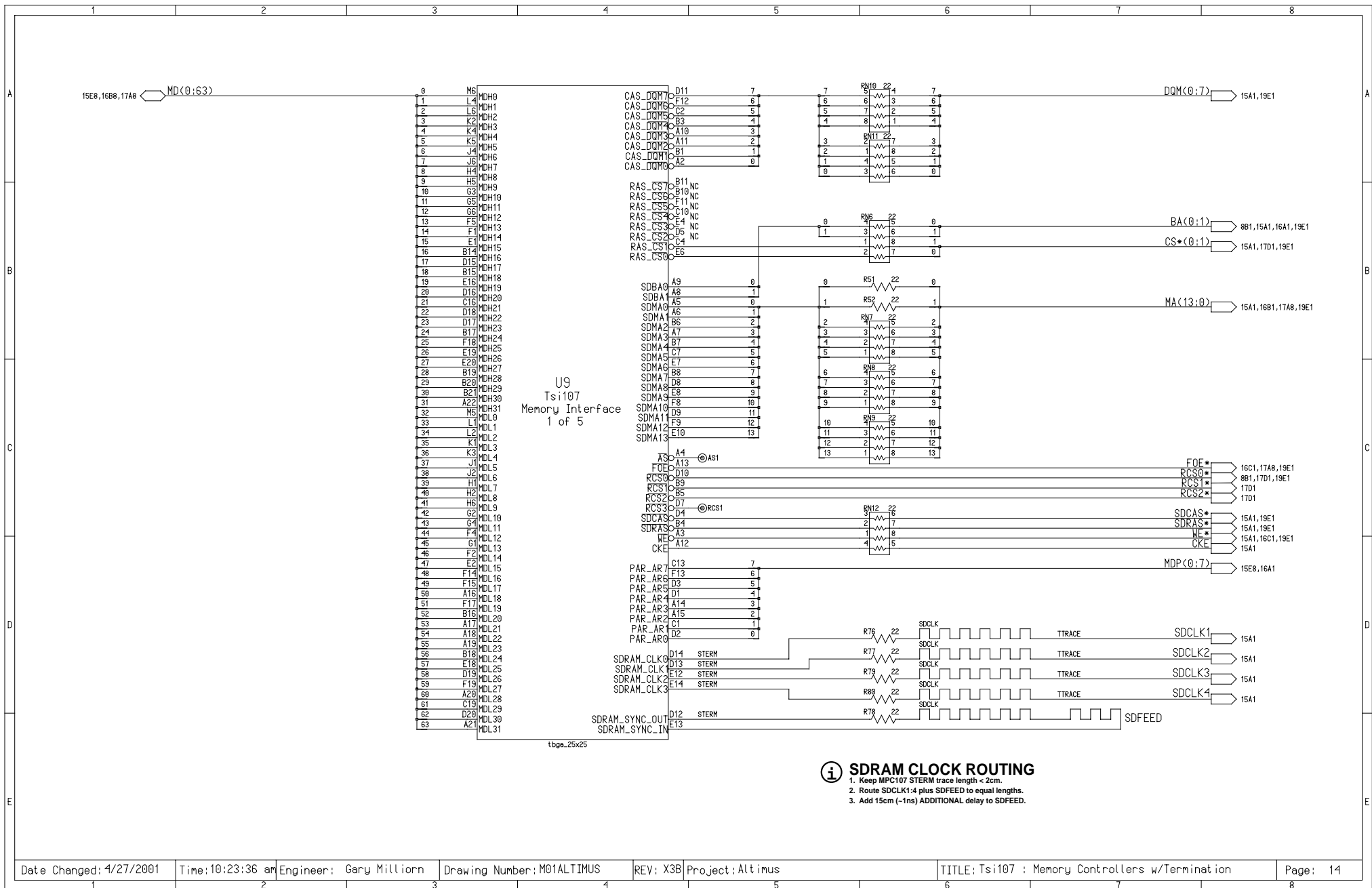
OVDD OUTPUT
3.3V or 2.5V Option
To CPU OVDD and MPC107 BVDD

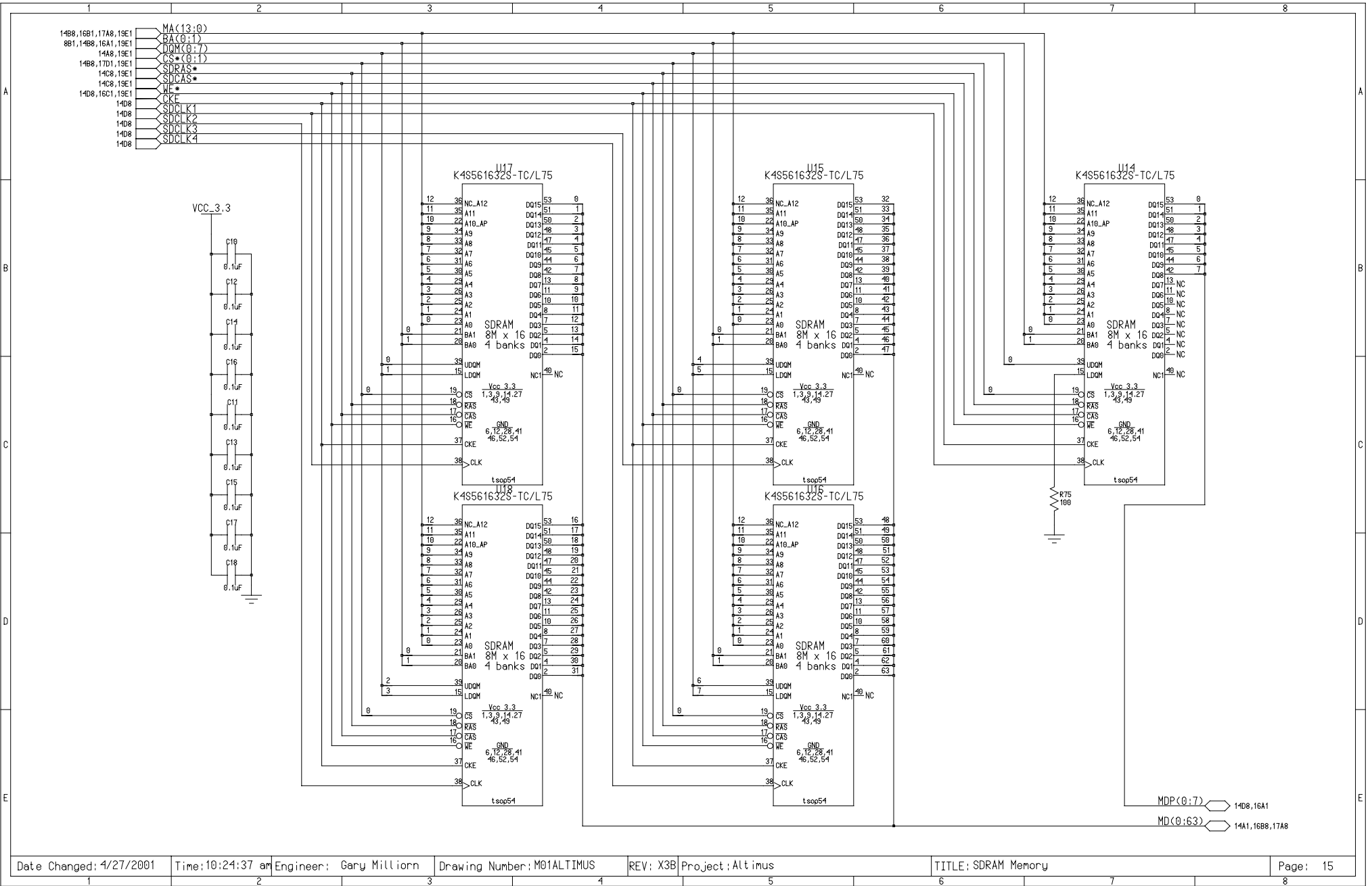




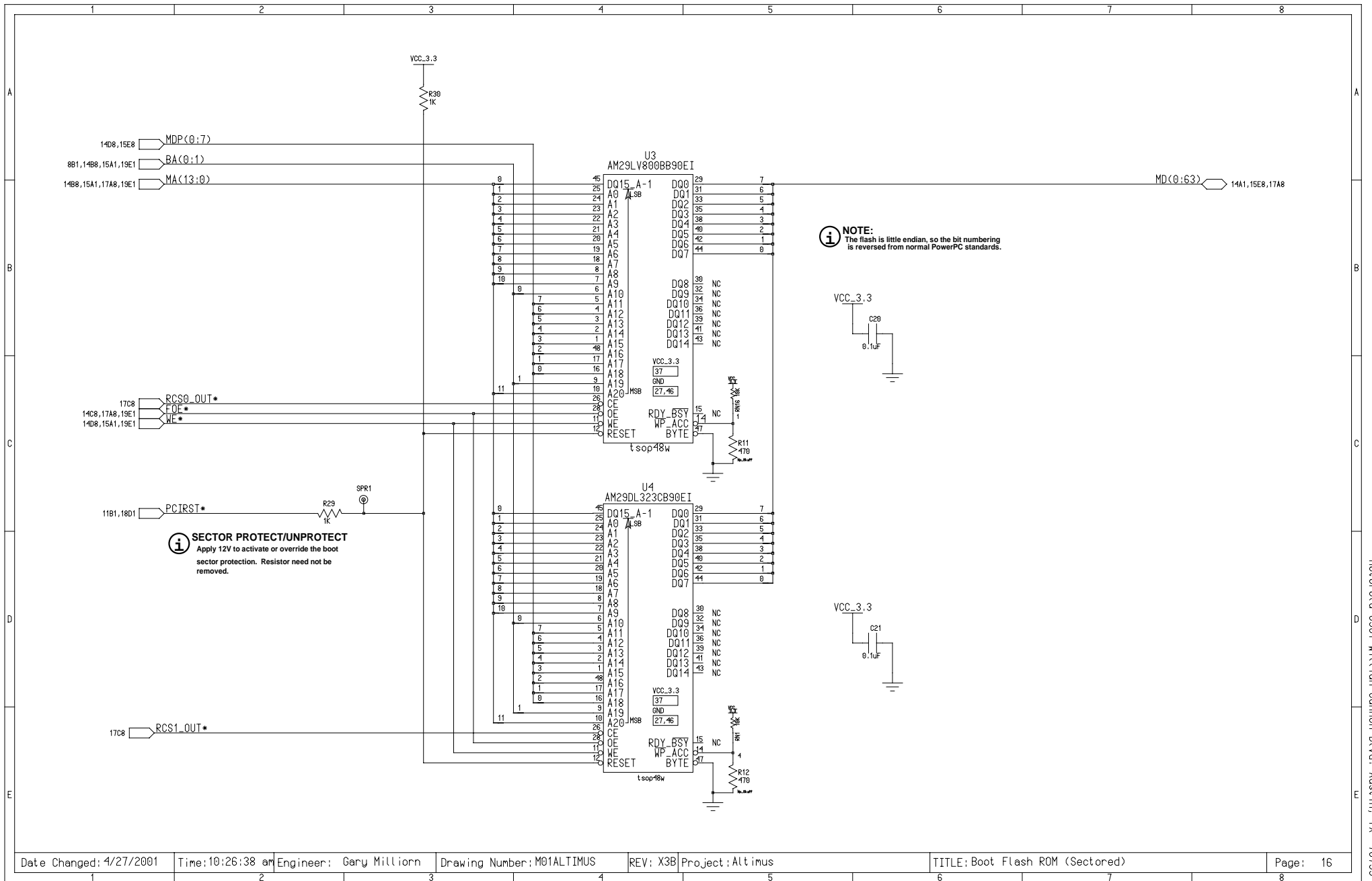


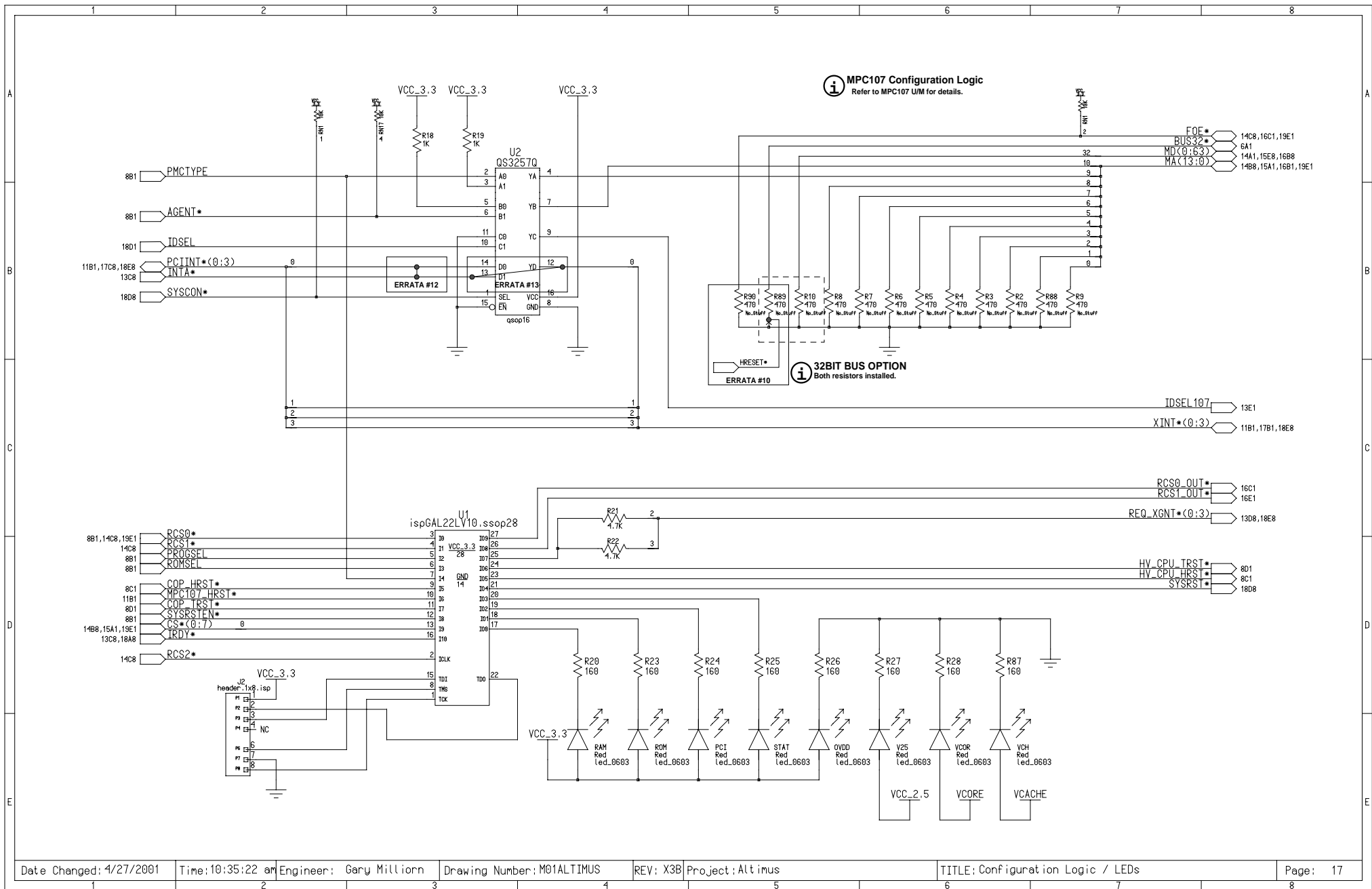




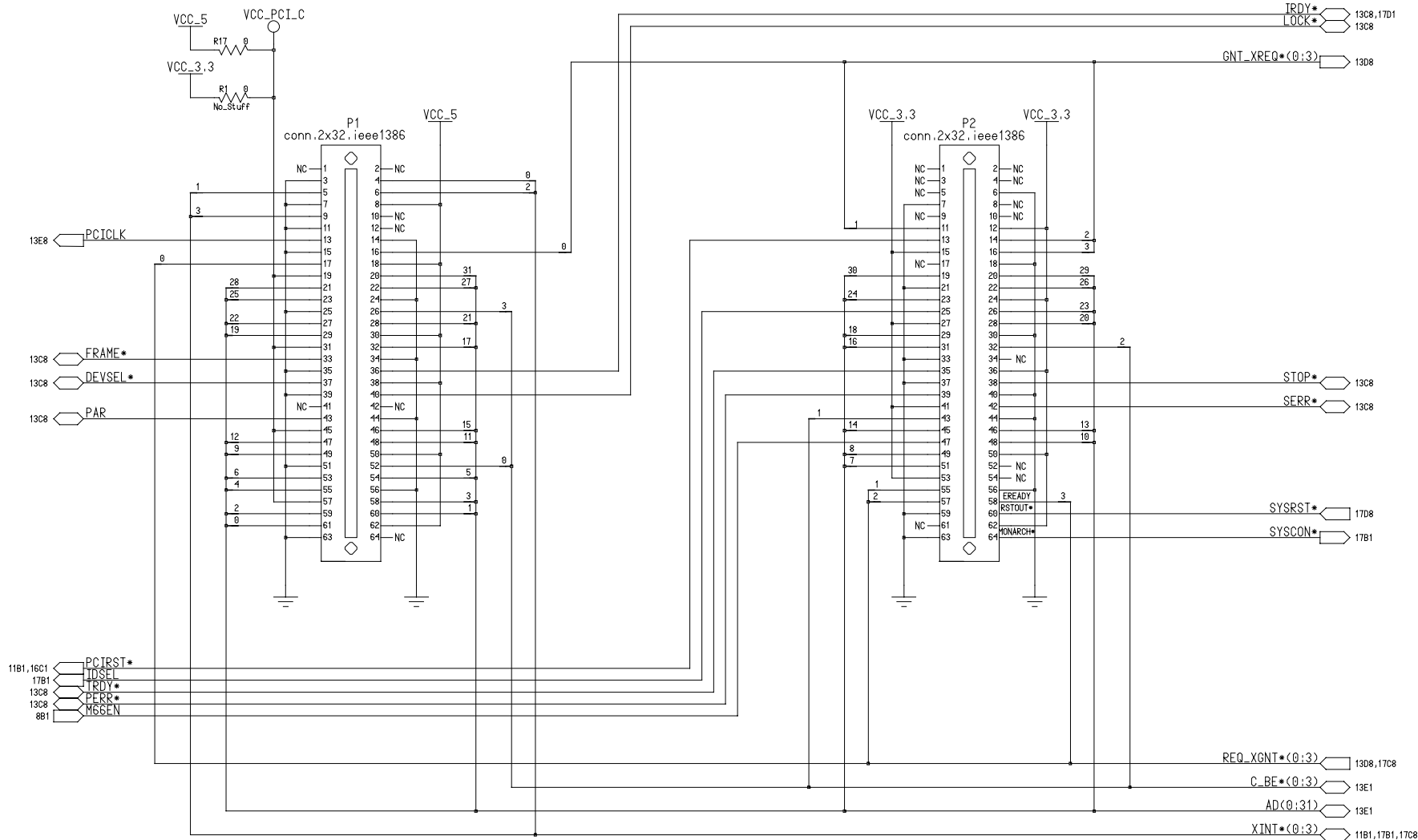


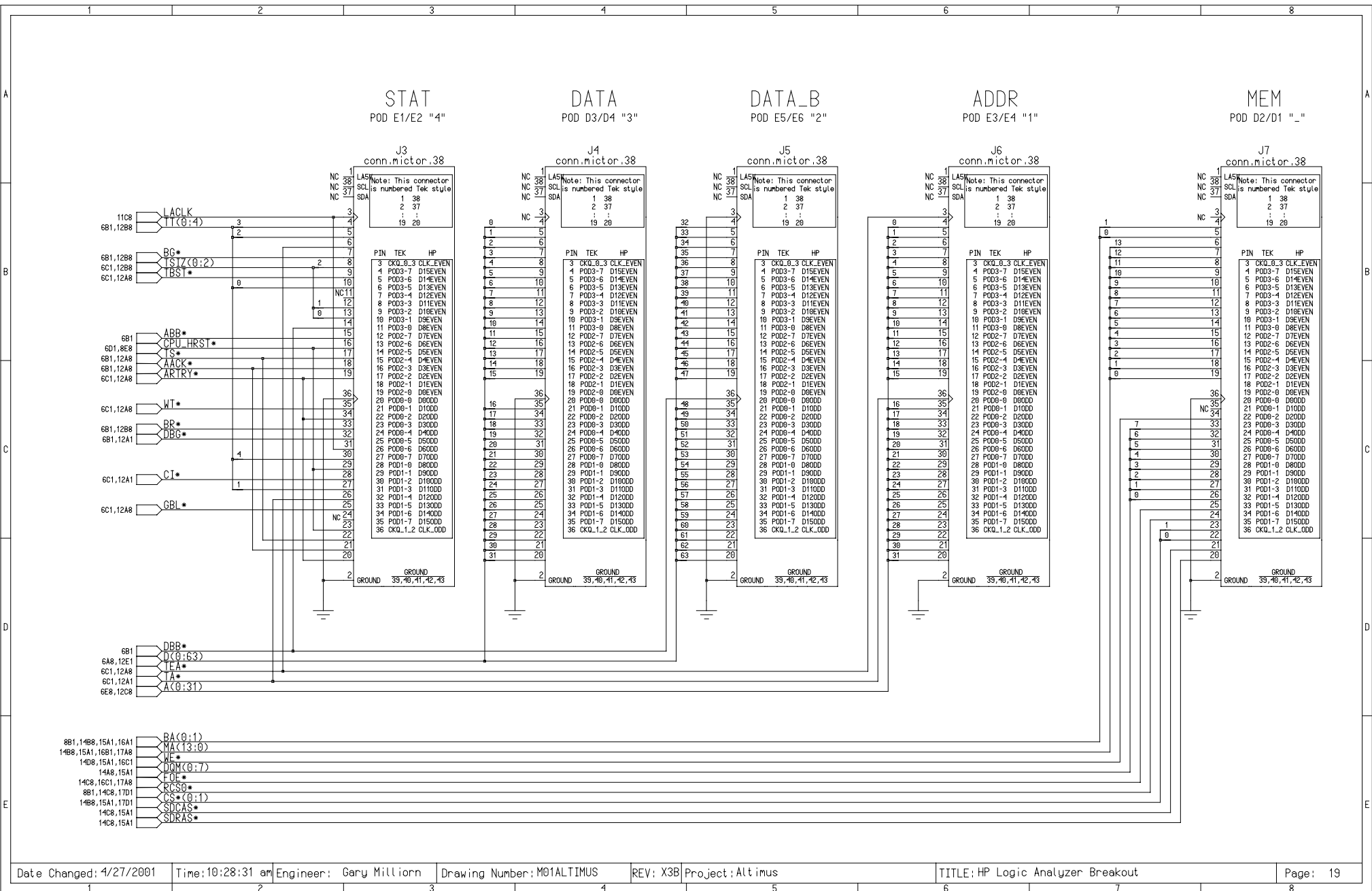
Motorola 6501 William Cannon Blvd. Austin, TX 78735





i V(I/O) SELECTION
 Select 3.3V or 5V V(I/O) option.
 ONE ONLY!
 MUST match Sandpoint configuration





1	2	3	4	5	6	7	8												

	1	2	3	4	5	6	7	8								
A																
B	<table><tr><th>REFDES</th><th>GND</th><th>OVD0</th><th>VCC.3.3</th></tr><tr><td>J3 J4 J5 J6 J7 RN1 RN5 RN13 RN16 RN17 RN2 RN3 RN4 RN14 RN15 U1 U3 U4 U9 U11 U12 U13 U14 U15 U16 U17 U18 U29 U30</td><td>39 40 41 42 43 14 27 46 C3 C6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K6 K20 L3 L7 L19 M23 N7 N19 P3 R7 R19 R23 T6 T20 U3 V7 V19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 ACS AC8 AD11 AD14 AD17 AG20 AG23 AD24 AE25 46 39 34 28 21 15 10 4 D3 D5 E3 E5 F3 F5 H3 H5 K3 K5 M3 M5 N3 N5 P3 P5 54 52 46 41 28 12 6 4</td><td>9 10 9 10 28 37</td><td>9 10 28 37 49 43 27 14 9 3 1 8</td></tr></table>								REFDES	GND	OVD0	VCC.3.3	J3 J4 J5 J6 J7 RN1 RN5 RN13 RN16 RN17 RN2 RN3 RN4 RN14 RN15 U1 U3 U4 U9 U11 U12 U13 U14 U15 U16 U17 U18 U29 U30	39 40 41 42 43 14 27 46 C3 C6 C9 C12 C15 C18 C21 C23 E3 F6 F10 F16 F20 F23 G8 G11 G13 G15 G18 H3 H7 H19 J23 K6 K20 L3 L7 L19 M23 N7 N19 P3 R7 R19 R23 T6 T20 U3 V7 V19 V23 W8 W11 W13 W15 W18 Y3 Y6 Y10 Y16 Y19 Y20 AA21 AB22 AC3 ACS AC8 AD11 AD14 AD17 AG20 AG23 AD24 AE25 46 39 34 28 21 15 10 4 D3 D5 E3 E5 F3 F5 H3 H5 K3 K5 M3 M5 N3 N5 P3 P5 54 52 46 41 28 12 6 4	9 10 9 10 28 37	9 10 28 37 49 43 27 14 9 3 1 8
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C																
D																
E																
Date Changed: 4/27/2001 Time:9:27:42 am Engineer: Gary Million Drawing Number: M01ALTIMUS REV: X3B Project: Altimus TITLE: Power/Ground Table Page: 21																

	1	2	3	4	5	6	7	8											
A																			
B																			
C																			
D																			
E																			

A