

T2080PCle

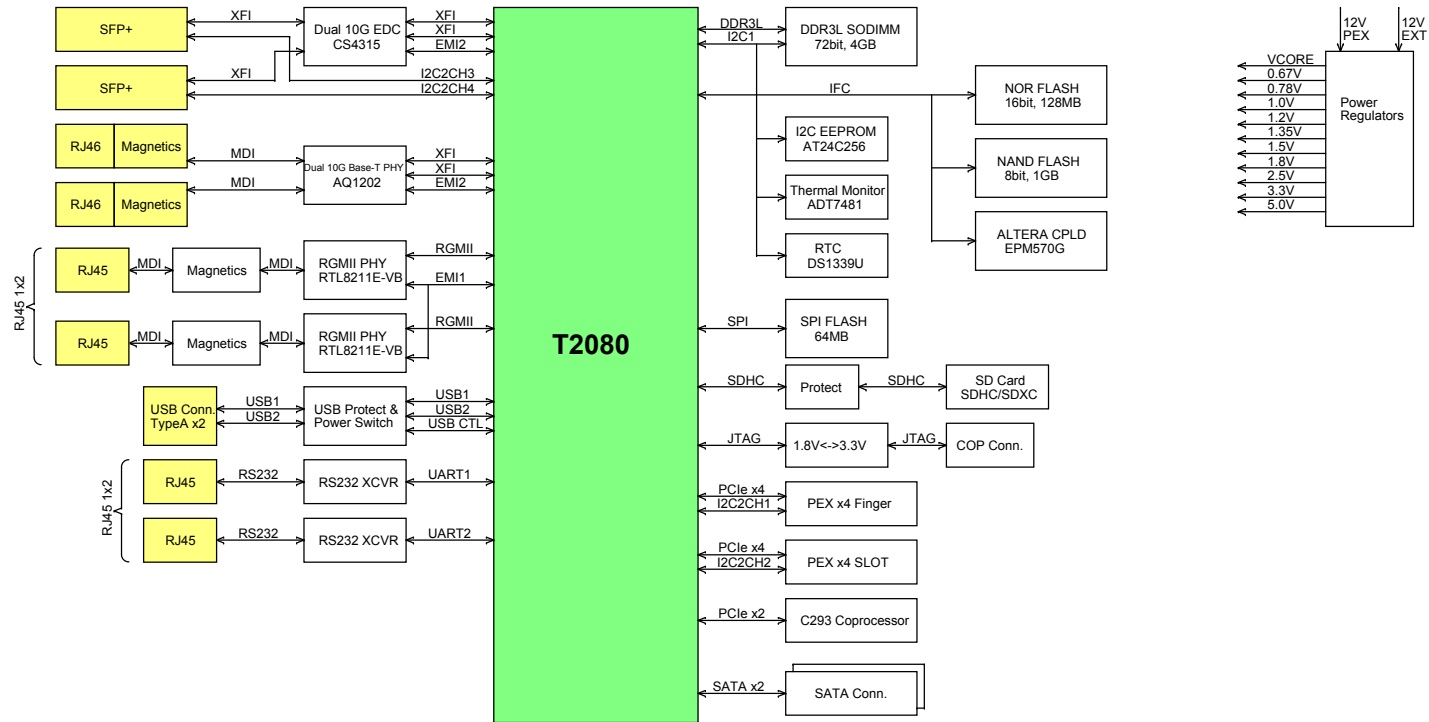
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Version Control		
Version	Date	Modifications
V0.1	2013/06	First release of Schematics
V1.0	2013/12	Released to Manufacturing
V2.0	2014/03	Change TF card socket with CD pin and move close to T2080 Add power-on 2 pin remote connector Add AQ1202 heatsink mounting hole and fan connector
V3.0	2014/04	Swap PCIe finger and PCIe slot SerDes lanes Add clock buffer for PCIe SerDes clock

All information is subject to change without notice.
No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your Freescale representative to obtain the latest information on this product.

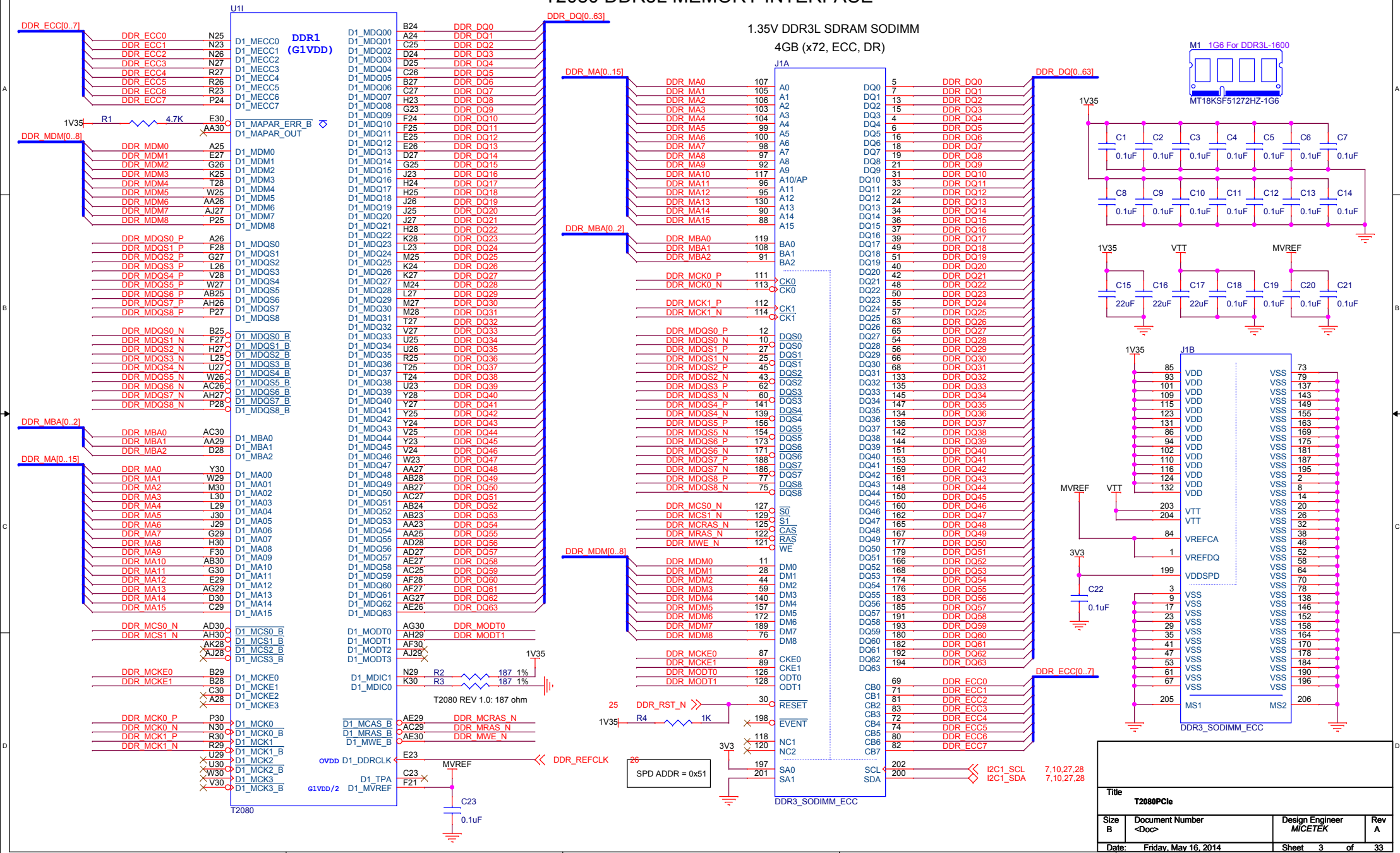
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SYSTEM BLOCK DIAGRAM



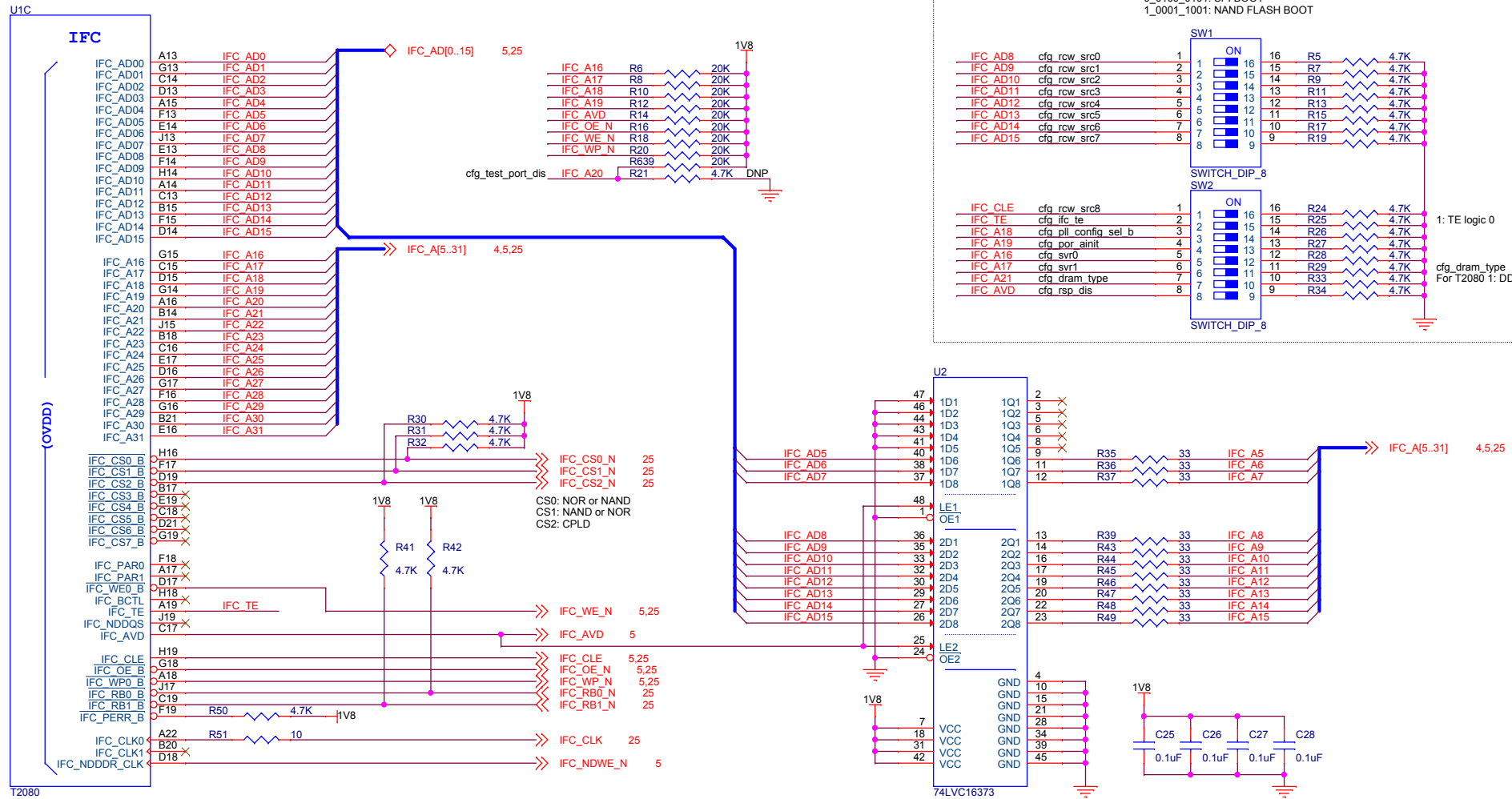
Title			
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T2080 DDR3L MEMORY INTERFACE



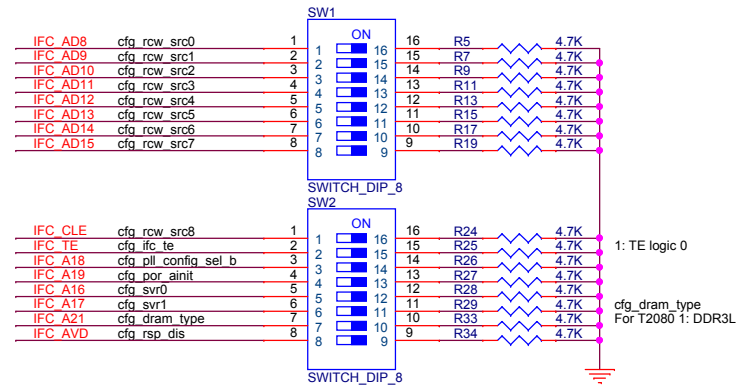
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T2080 IFC INTERFACE



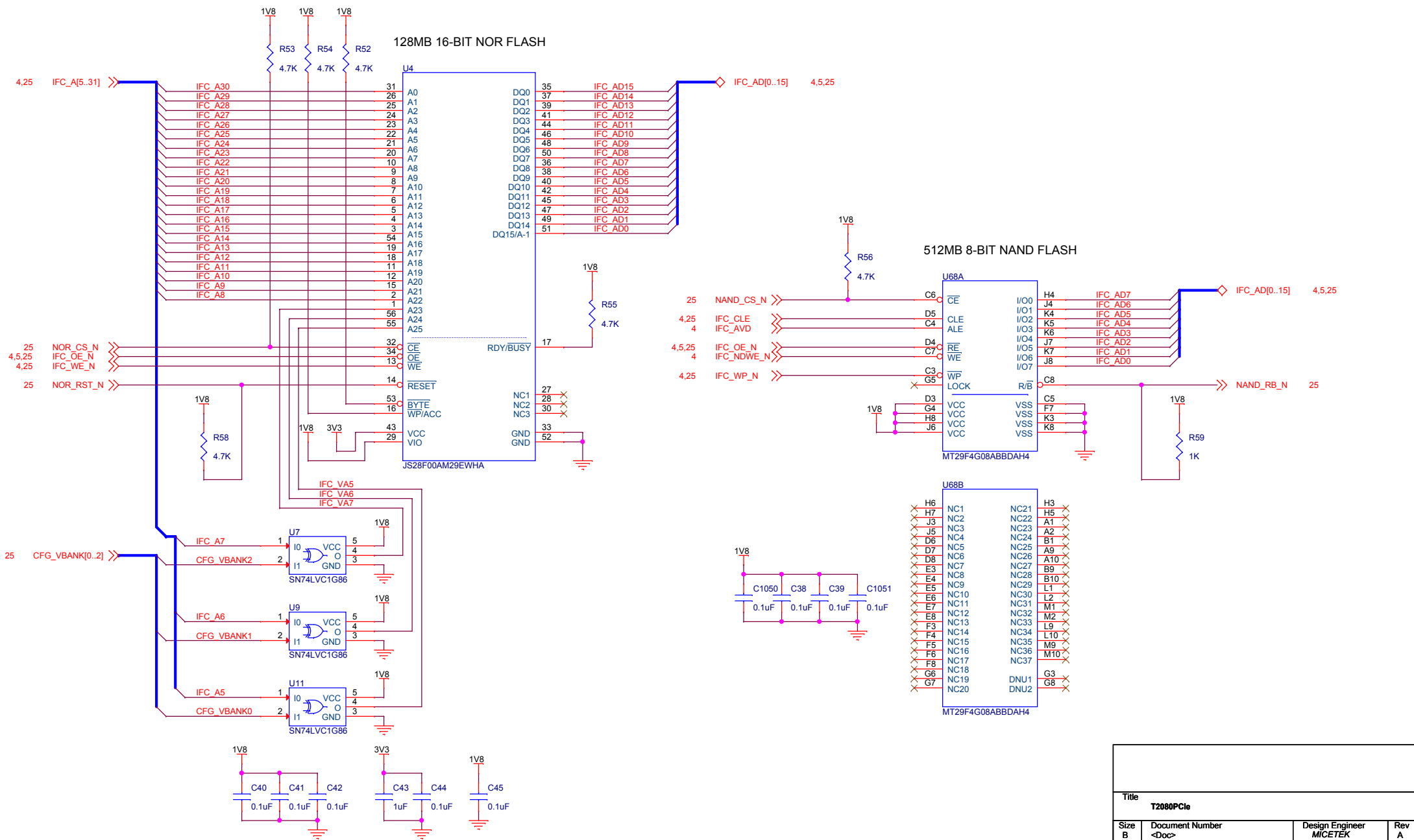
T2080 RESET CONFIGURATION

cfg_row_src[0:8]
 0_0010_0111: NOR FLASH BOOT
 0_0100_0000: SD CARD BOOT
 0_0100_0101: SPI BOOT
 1_0001_1001: NAND FLASH BOOT



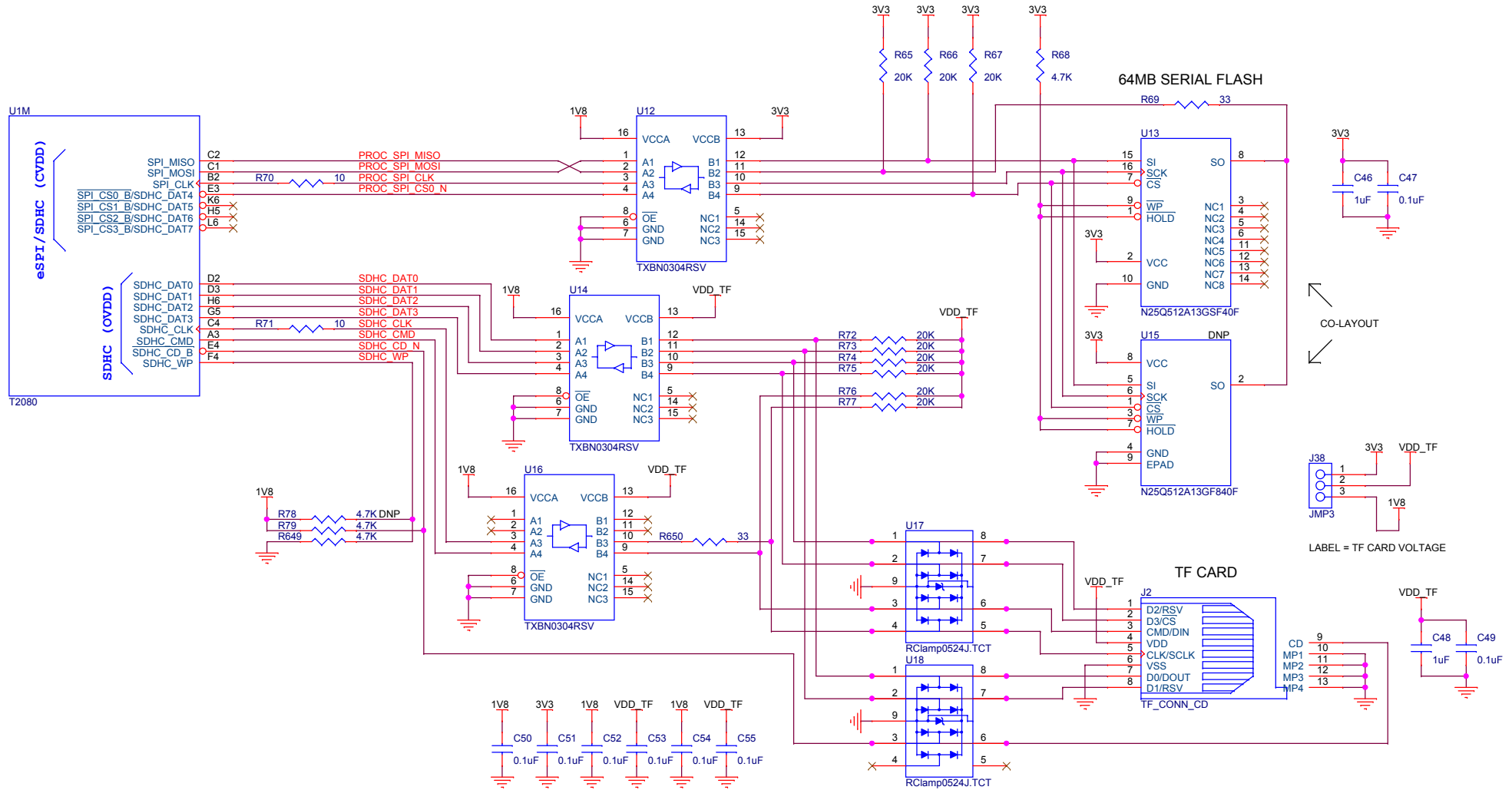
Title			
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T2080 NOR and NAND FLASH INTERFACE



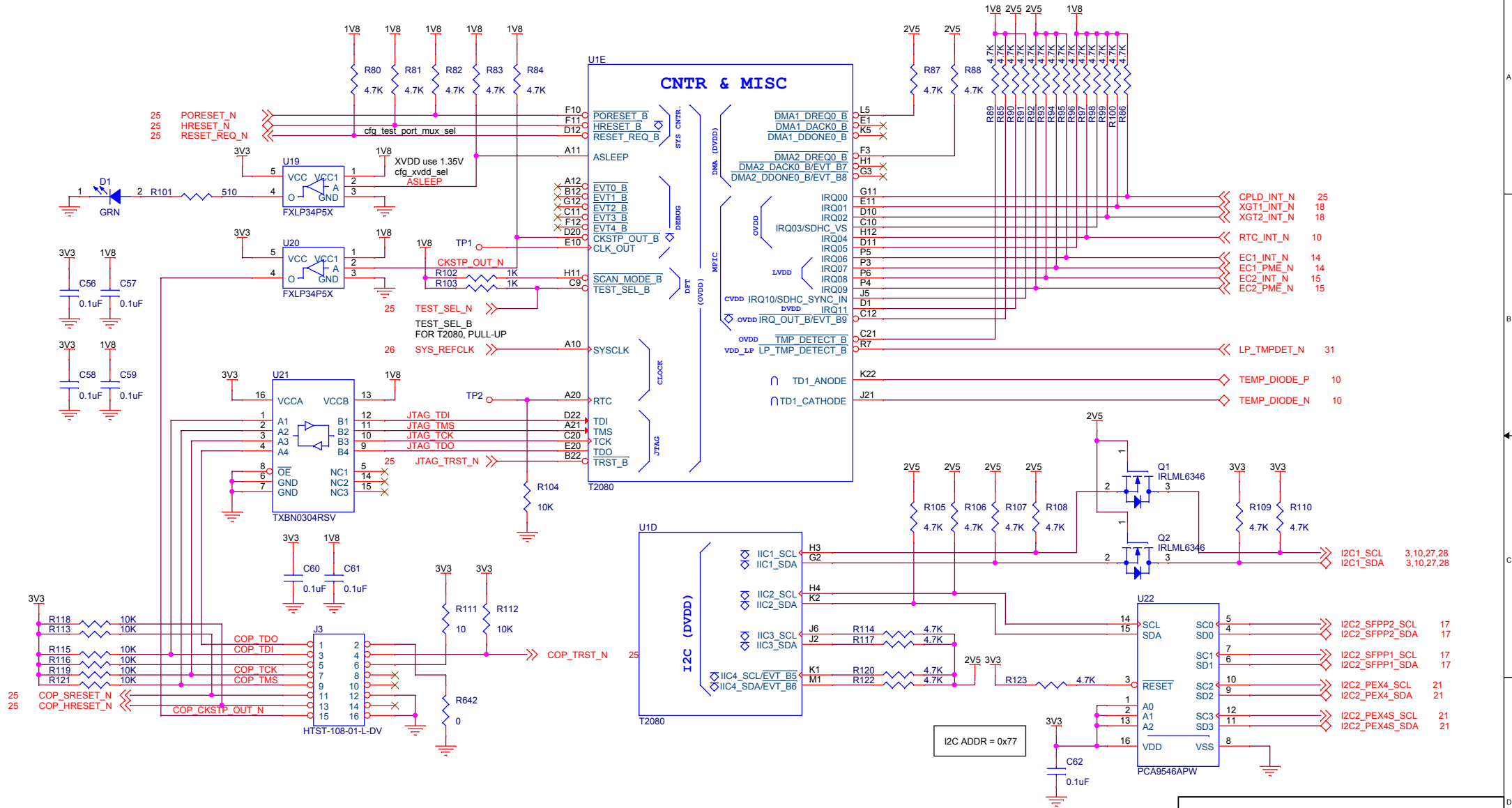
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T2080 SPI FLASH and SDHC INTERFACE



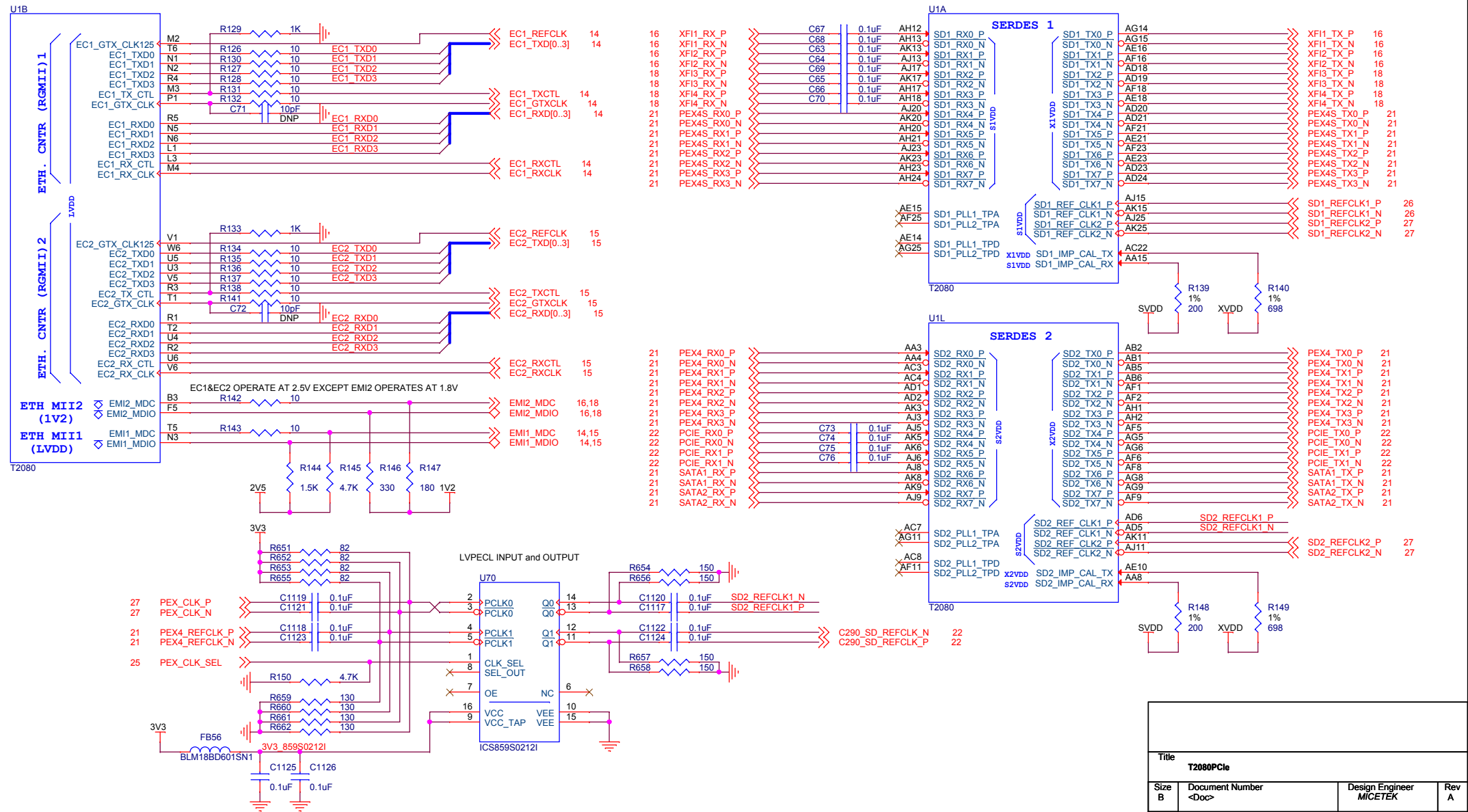
Title			
T2080PCIe			
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T2080 SYSTEM LOGIC INTERFACE

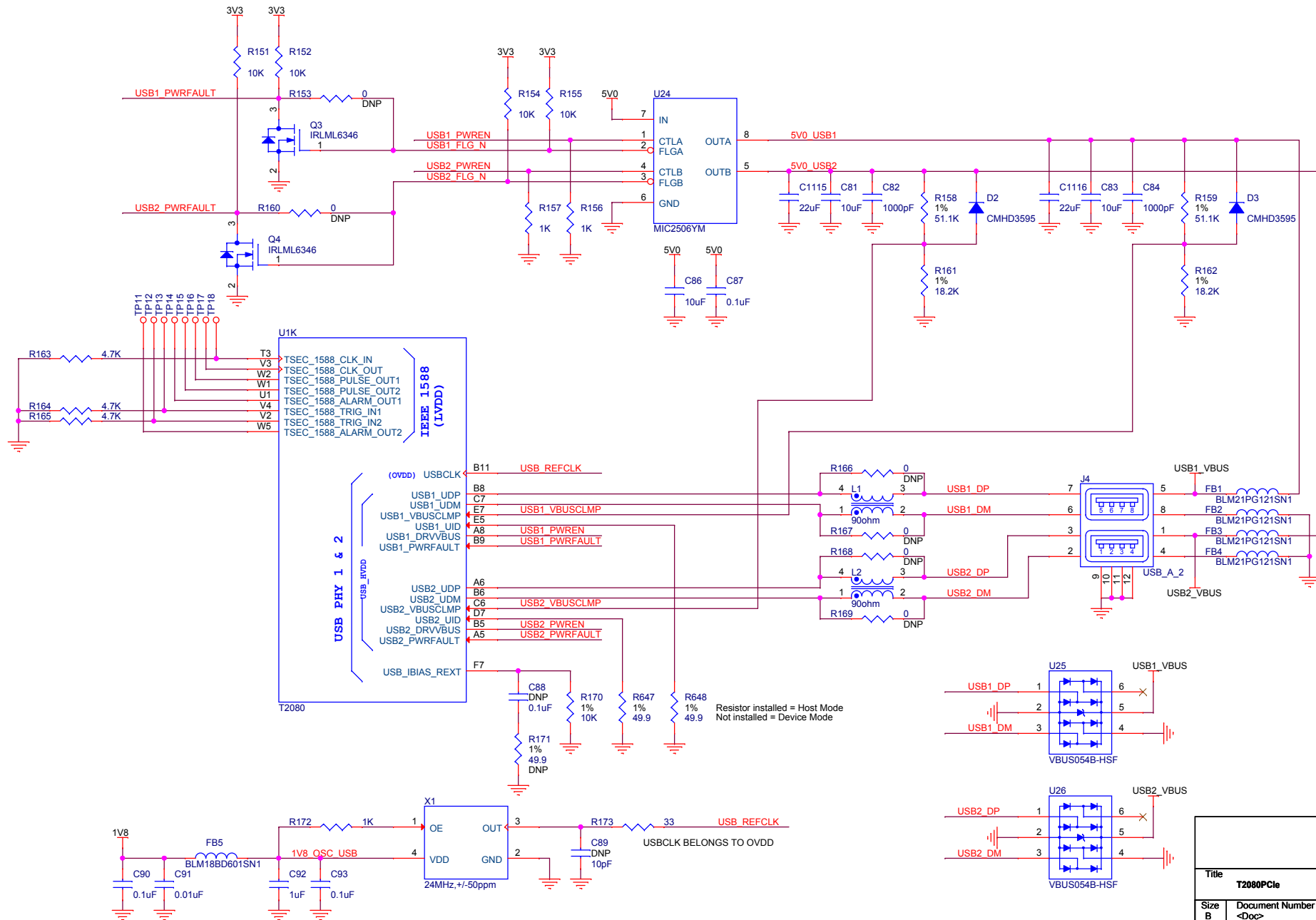


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T2080PCIe			
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T2080 ETHERNET and SERDES INTERFACE

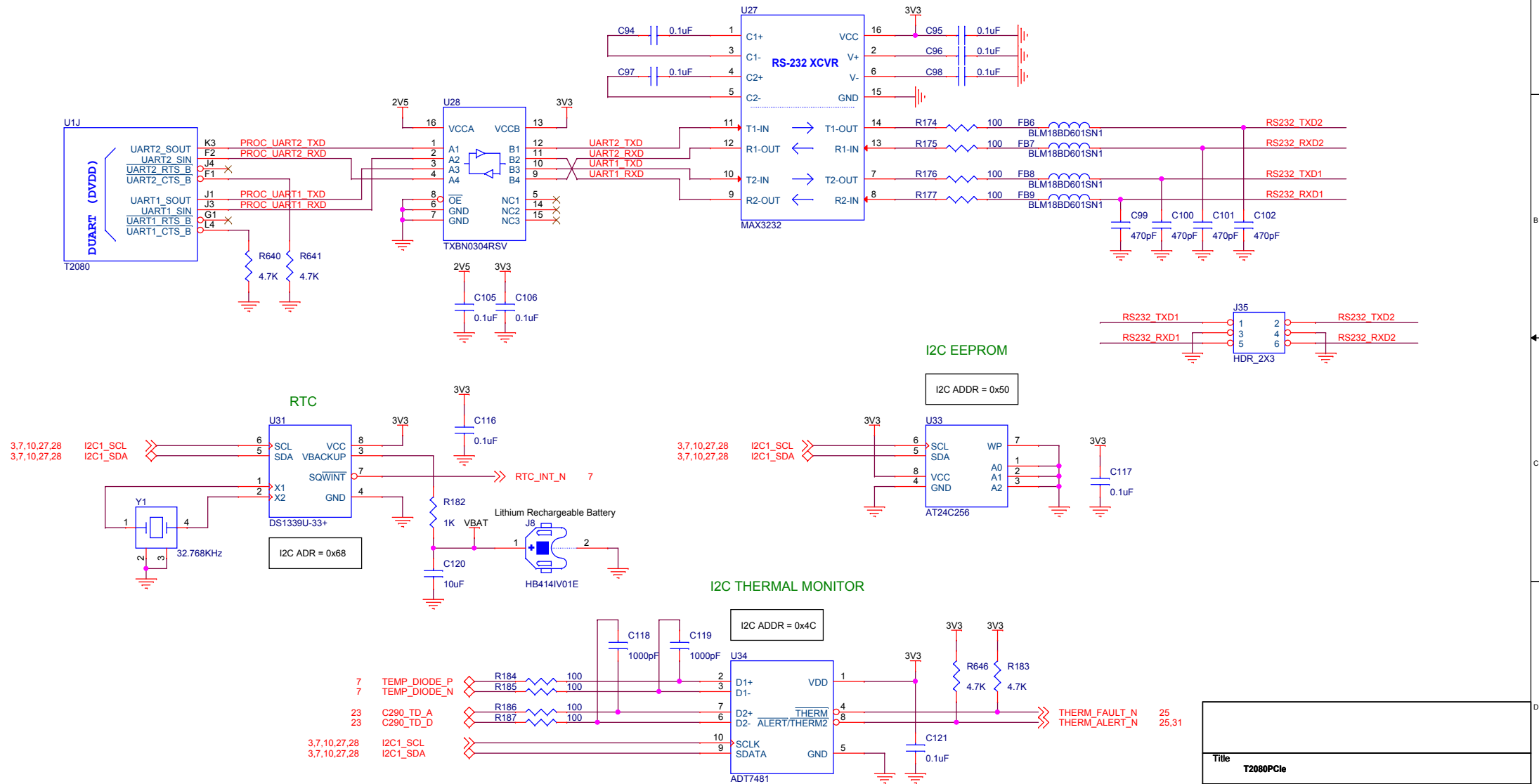


T2080 USB INTERFACE



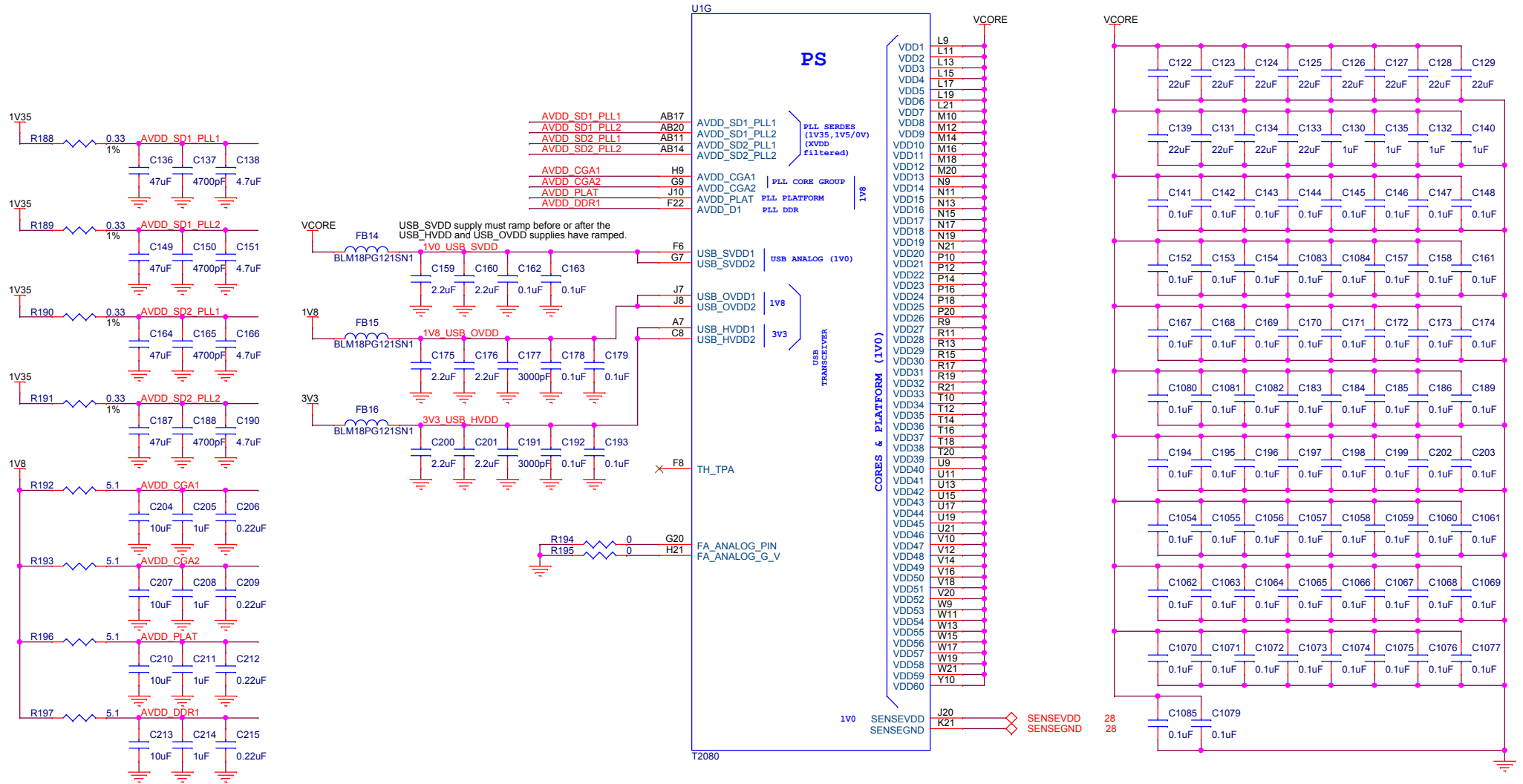
Title			
T2080PCIe			
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T2080 DUART and I2C DEVICE INTERFACE



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T2080 POWER SUPPLY



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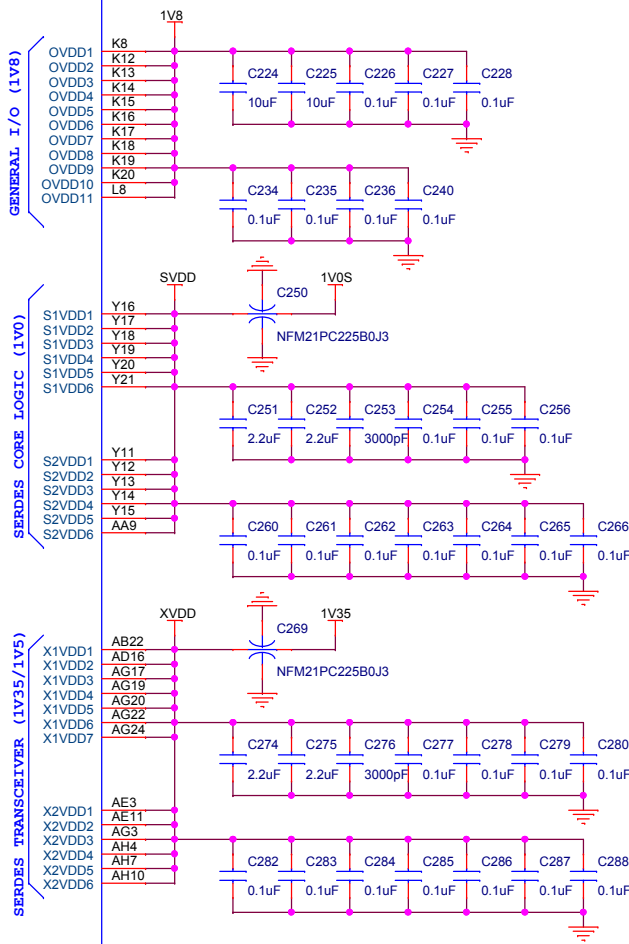
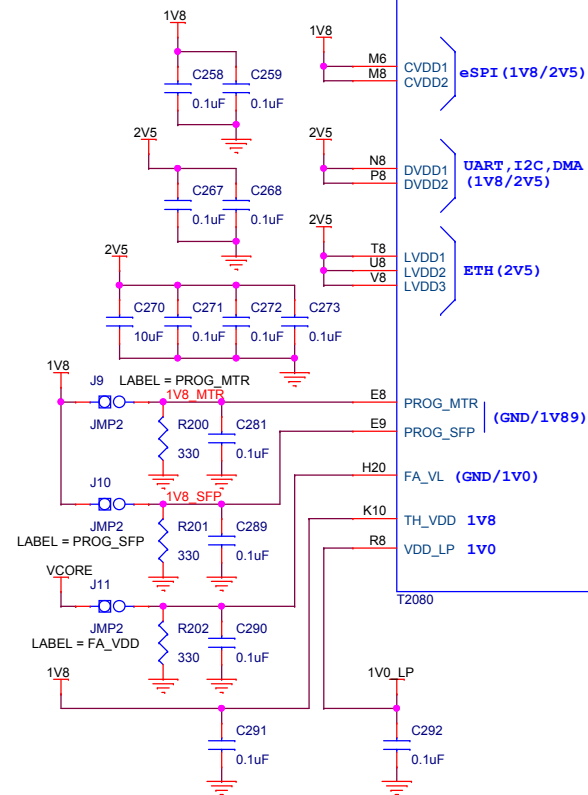
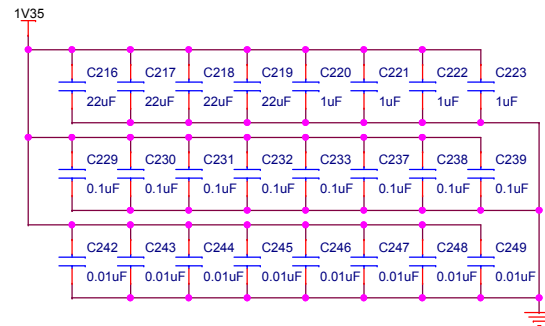
Pin Configuration Diagram for T2080

U1F Package Pins:

- 1V35:** L22, M22, N22, P22, R22, T22, U22, V22, A29, B30, D29, F29, H29, K29, M29, P29, T29, T30, V29, Y29, AB29, AD29, AF29, AJ30, AK29
- 1V8:** M6, M8
- 2V5:** N8, P8, T8, U8, V8
- C273:** 0.1uF
- E8:** PROG_MTR
- E9:** PROG_SFF
- H20:** FA_VL
- K10:** TH_VDD
- R8:** VDD_LP

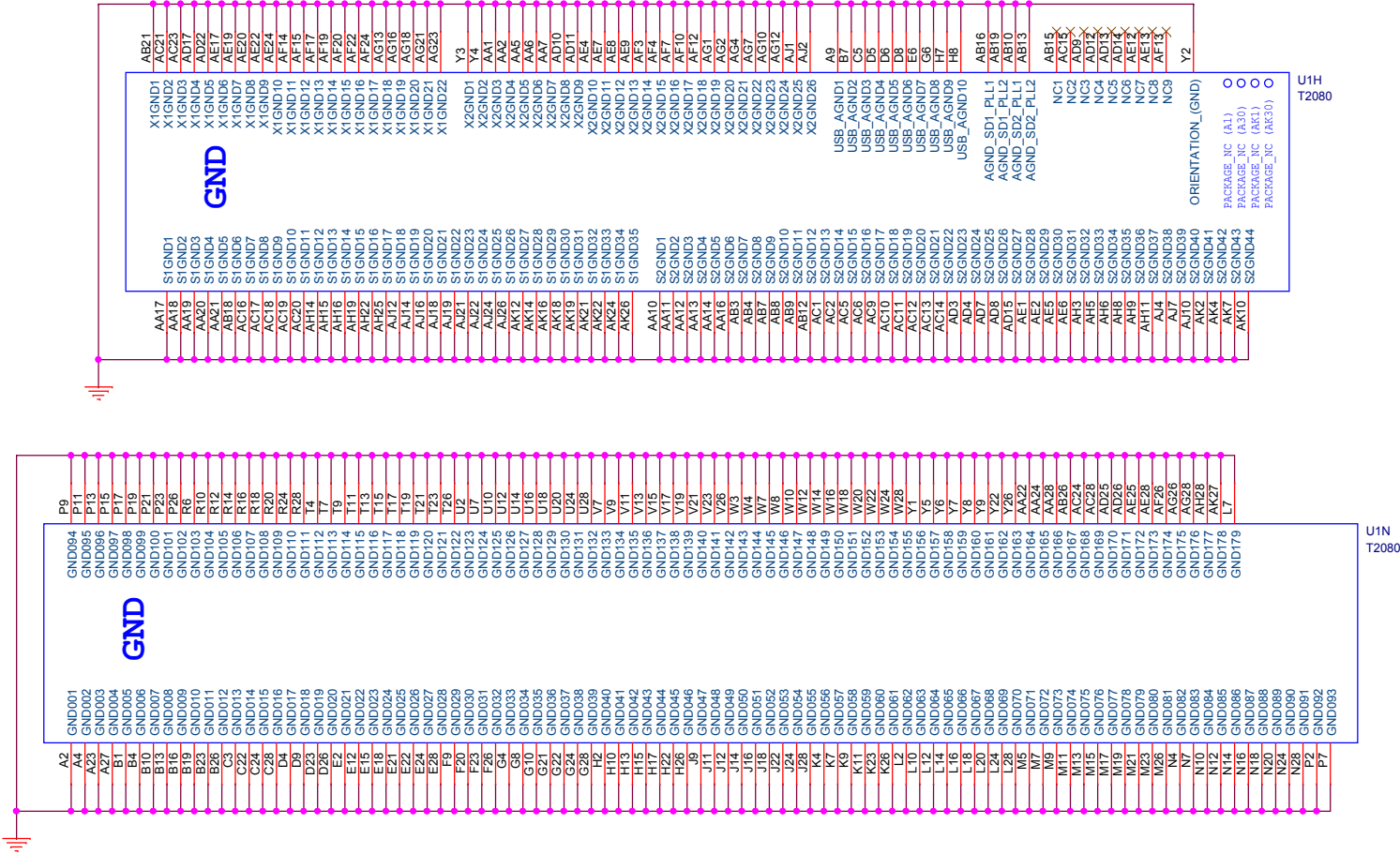
Internal Connections and Labels:

- PS (Power Supply):** G1VDD1, G1VDD2, G1VDD3, G1VDD4, G1VDD5, G1VDD6, G1VDD7, G1VDD8, G1VDD9, G1VDD10, G1VDD11, G1VDD12, G1VDD13, G1VDD14, G1VDD15, G1VDD16, G1VDD17, G1VDD18, G1VDD19, G1VDD20, G1VDD21, G1VDD22, G1VDD23, G1VDD24, G1VDD25
- DDR (1V35/1V5):** G1VDD1, G1VDD2, G1VDD3, G1VDD4, G1VDD5, G1VDD6, G1VDD7, G1VDD8, G1VDD9, G1VDD10, G1VDD11, G1VDD12, G1VDD13, G1VDD14, G1VDD15, G1VDD16, G1VDD17, G1VDD18, G1VDD19, G1VDD20, G1VDD21, G1VDD22, G1VDD23, G1VDD24, G1VDD25
- GENERAL I/O (1V8):** OVDD1, OVDD2, OVDD3, OVDD4, OVDD5, OVDD6, OVDD7, OVDD8, OVDD9, OVDD10, OVDD11
- SERDES CORE LOGIC (1V0):** S1VDD1, S1VDD2, S1VDD3, S1VDD4, S1VDD5, S1VDD6, S2VDD1, S2VDD2, S2VDD3, S2VDD4, S2VDD5, S2VDD6
- UART, I2C, DMA (1V8/2V5):** DVDD1, DVDD2
- ETH (2V5):** LVDD1, LVDD2, LVDD3
- SERDES TRANSCIEVER (1V35/1V5):** X1VDD1, X1VDD2, X1VDD3, X1VDD4, X1VDD5, X1VDD6, X1VDD7, X2VDD1, X2VDD2, X2VDD3, X2VDD4, X2VDD5, X2VDD6
- Other Labels:** (GND/1V89), (GND/1V0)

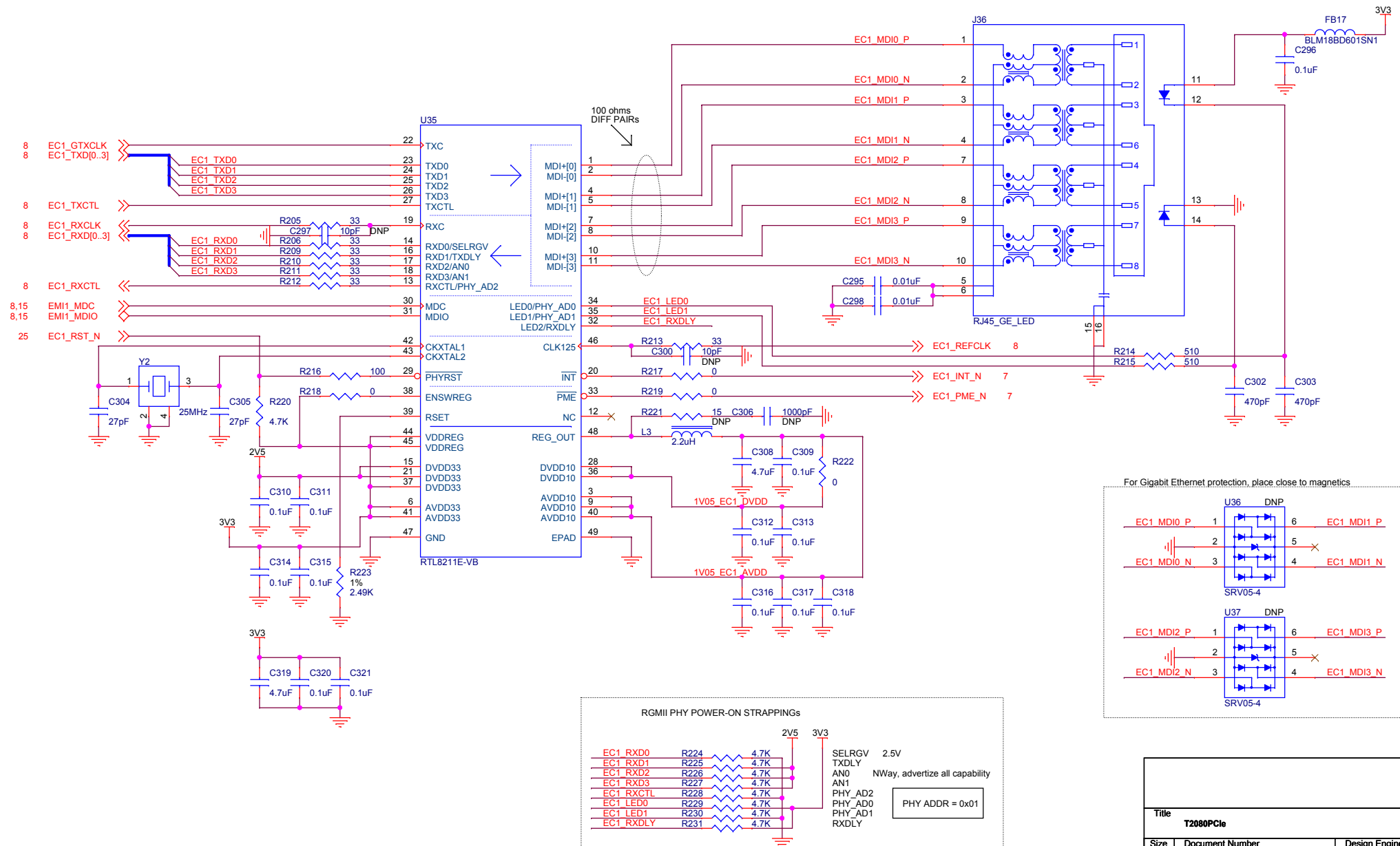


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T2080 GROUND

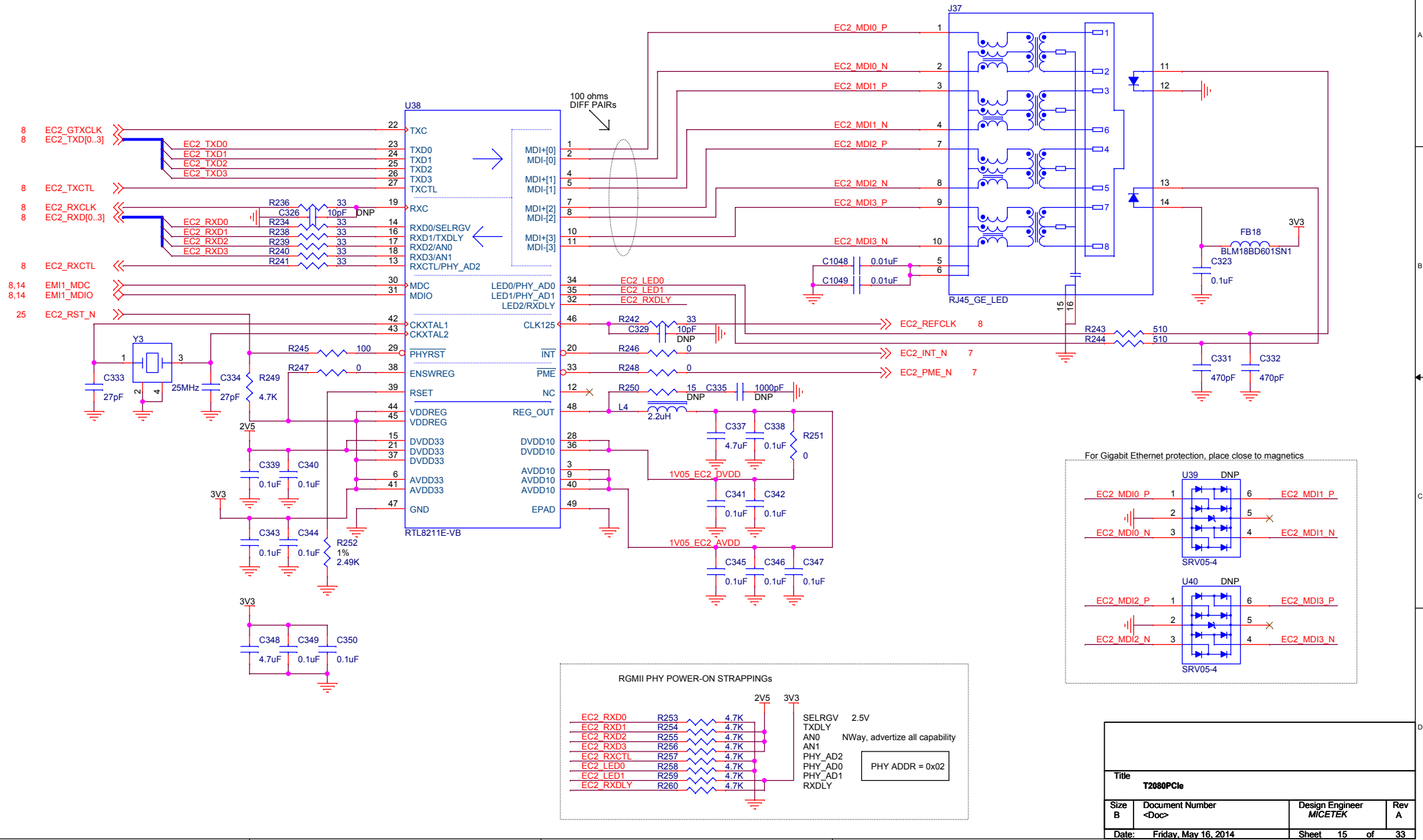


RGMII ETHERNET PORT 1

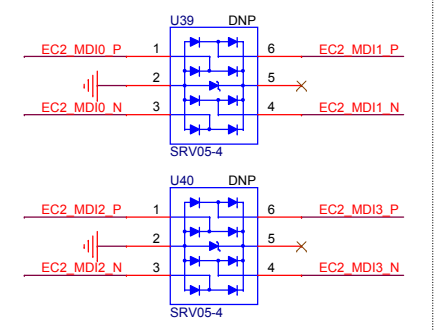


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RGMII ETHERNET PORT 2

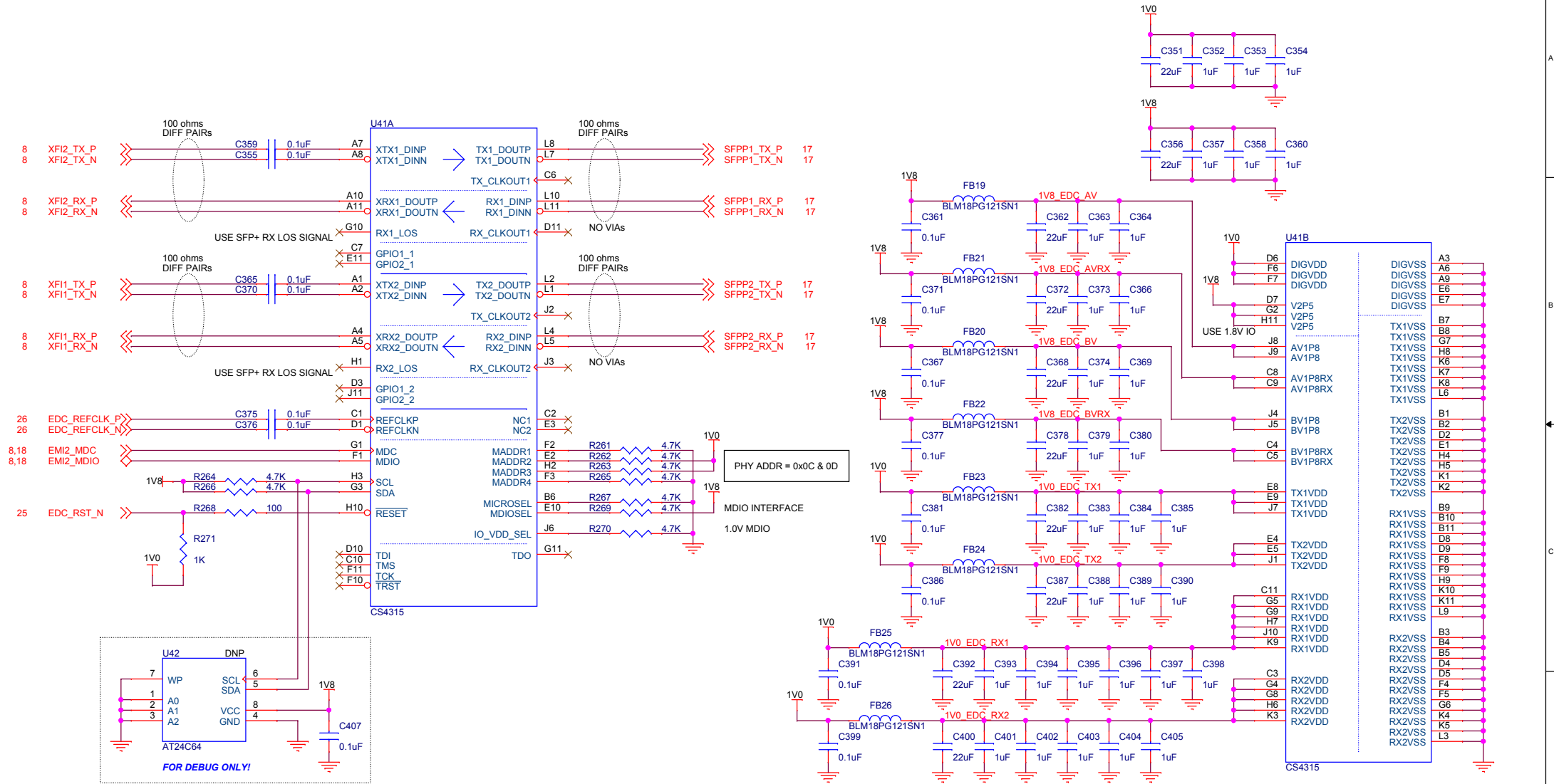


For Gigabit Ethernet protection, place close to magnetics



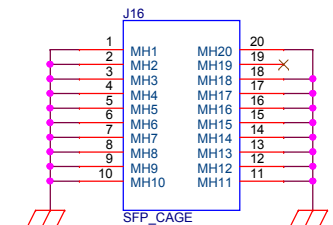
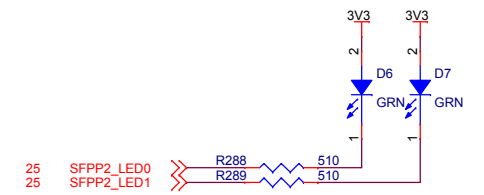
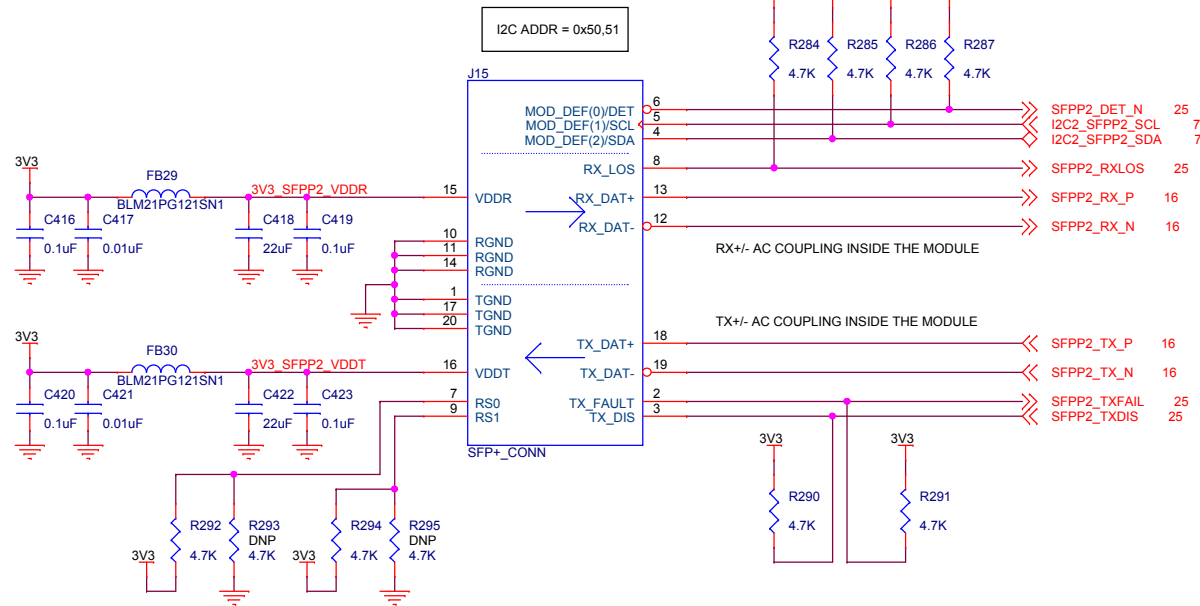
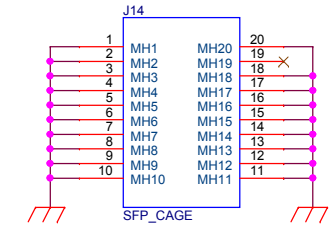
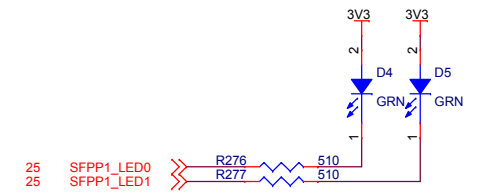
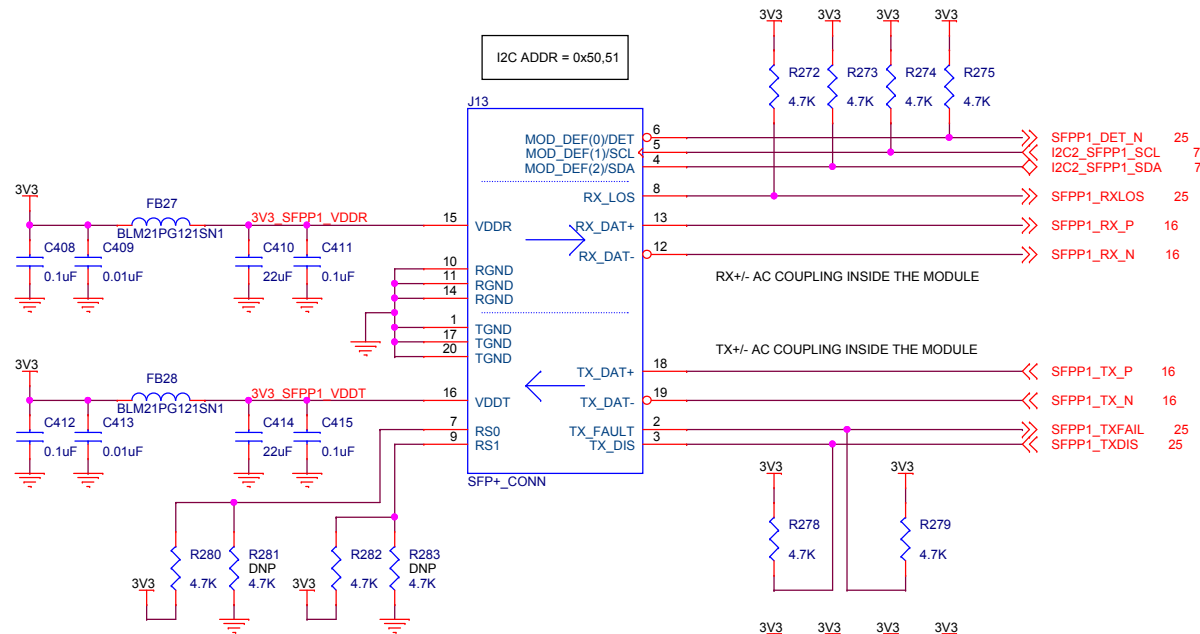
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10G EDC PHY CS4315



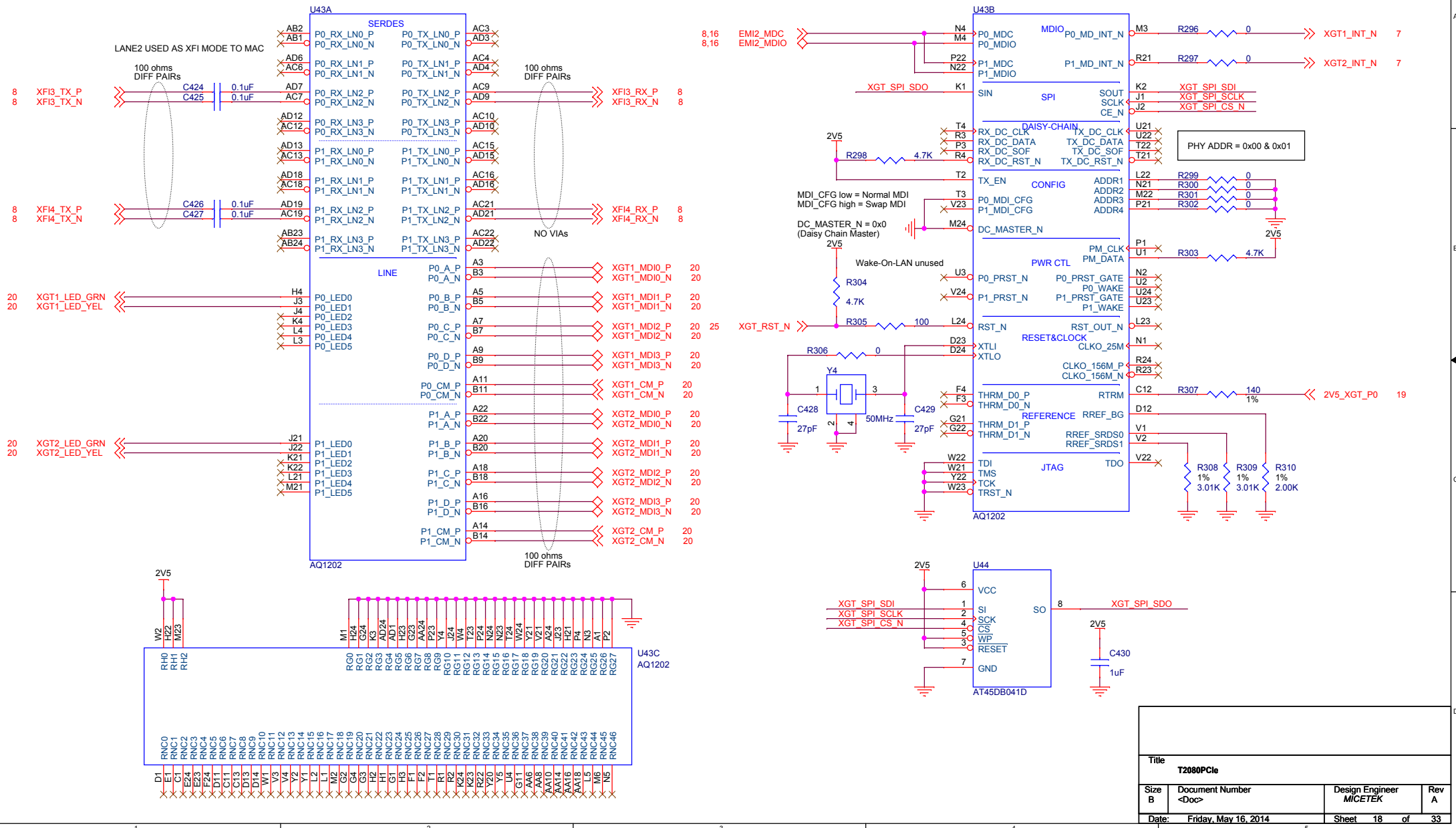
Title			
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SFP+ CONNECTORS



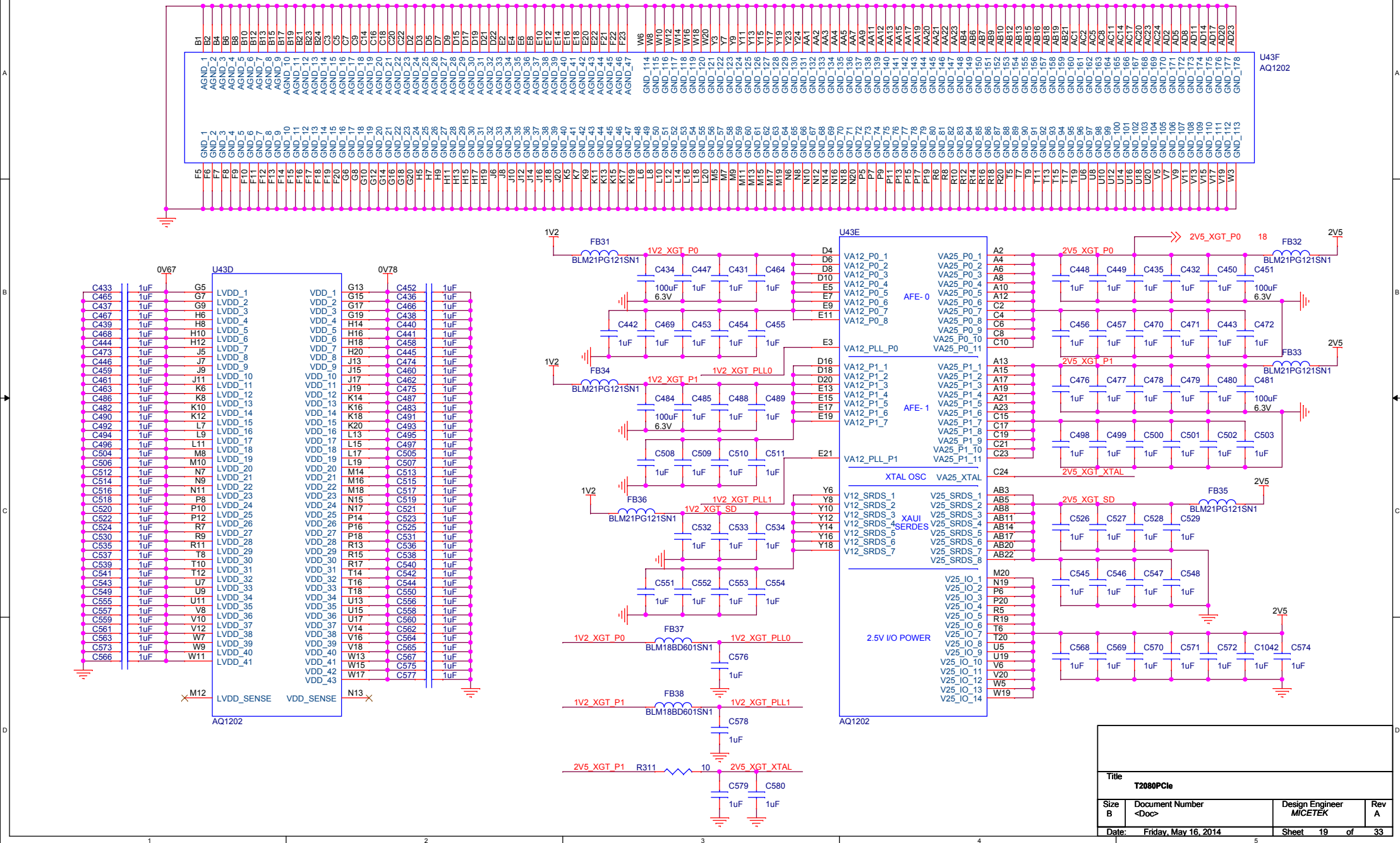
Title			
T2080PCle			
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10G BASE-T PHY AQ1202

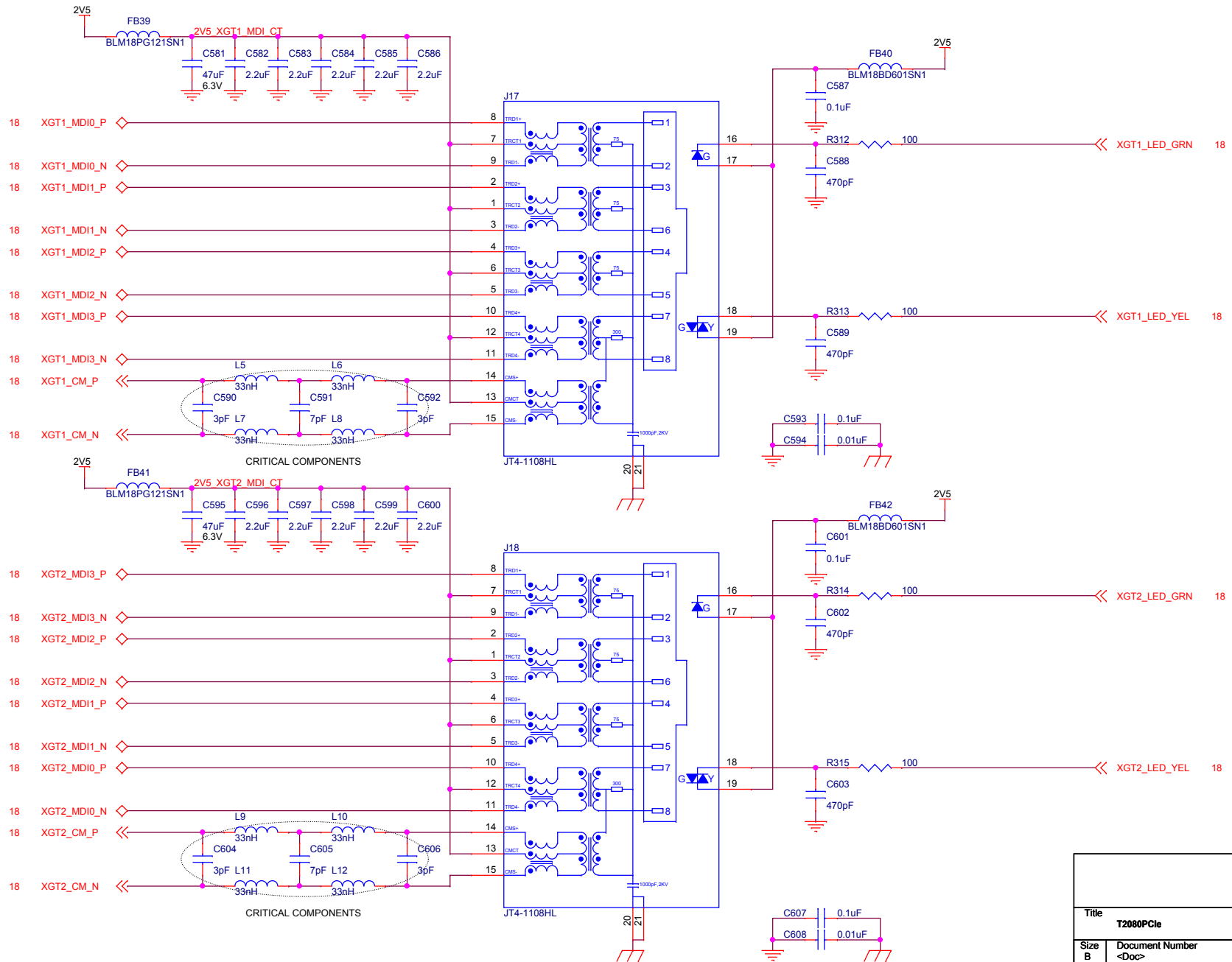


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T2080PCIe			
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10G BASE-T PHY AQ1202 POWER SUPPLY



10G BASE-T RJ46 CONNECTORs



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PCIE X4 FINGER

PCIE X4 SLOT

ON-BOARD SATA CONNECTOR

ON-BOARD SATA CONNECTOR

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PCIE X4 FINGER

PCIE x4 SLOT

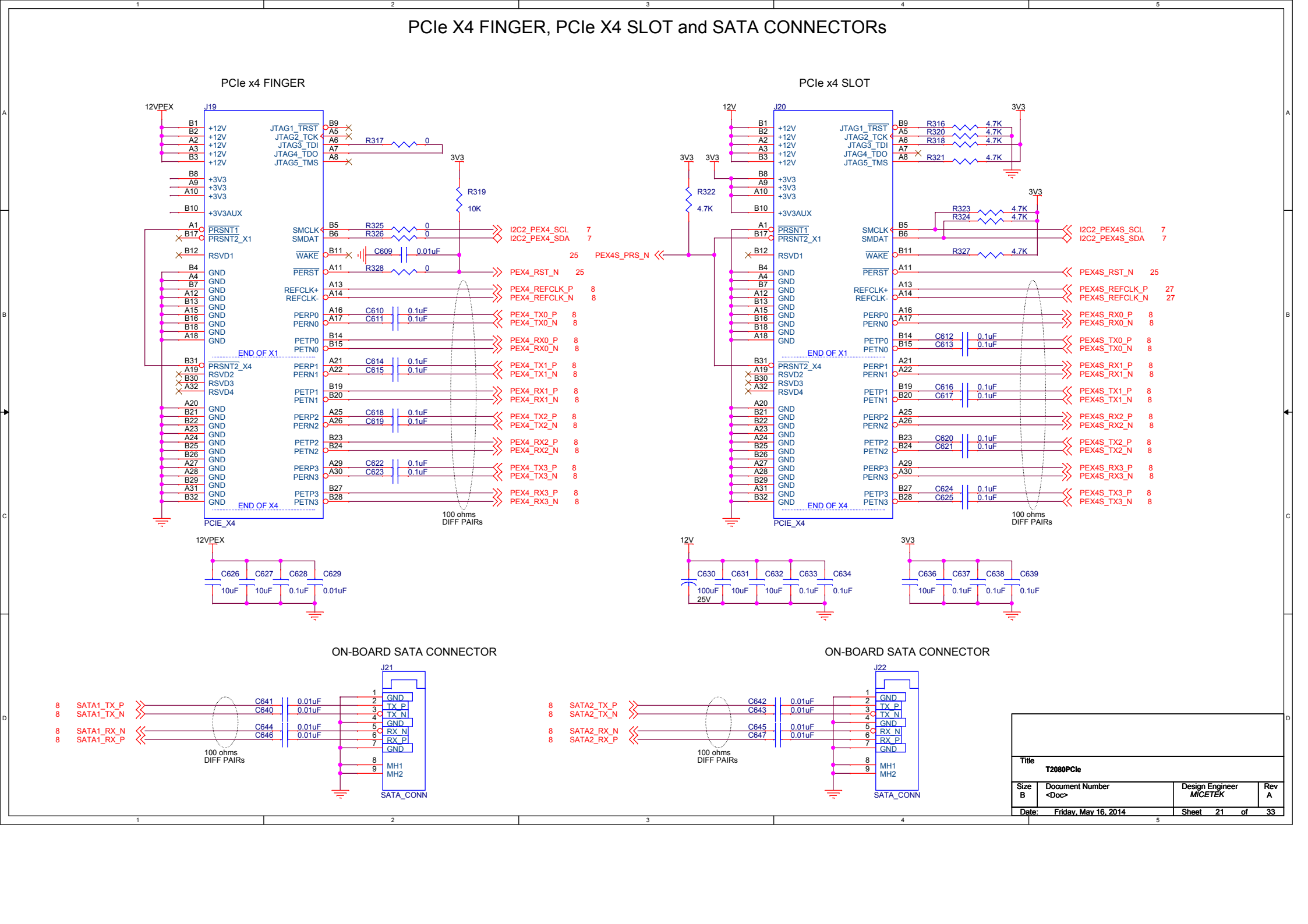
ON-BOARD SATA CONNECTOR

ON-BOARD SATA CONNECTOR

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PCIE X4 FINGER

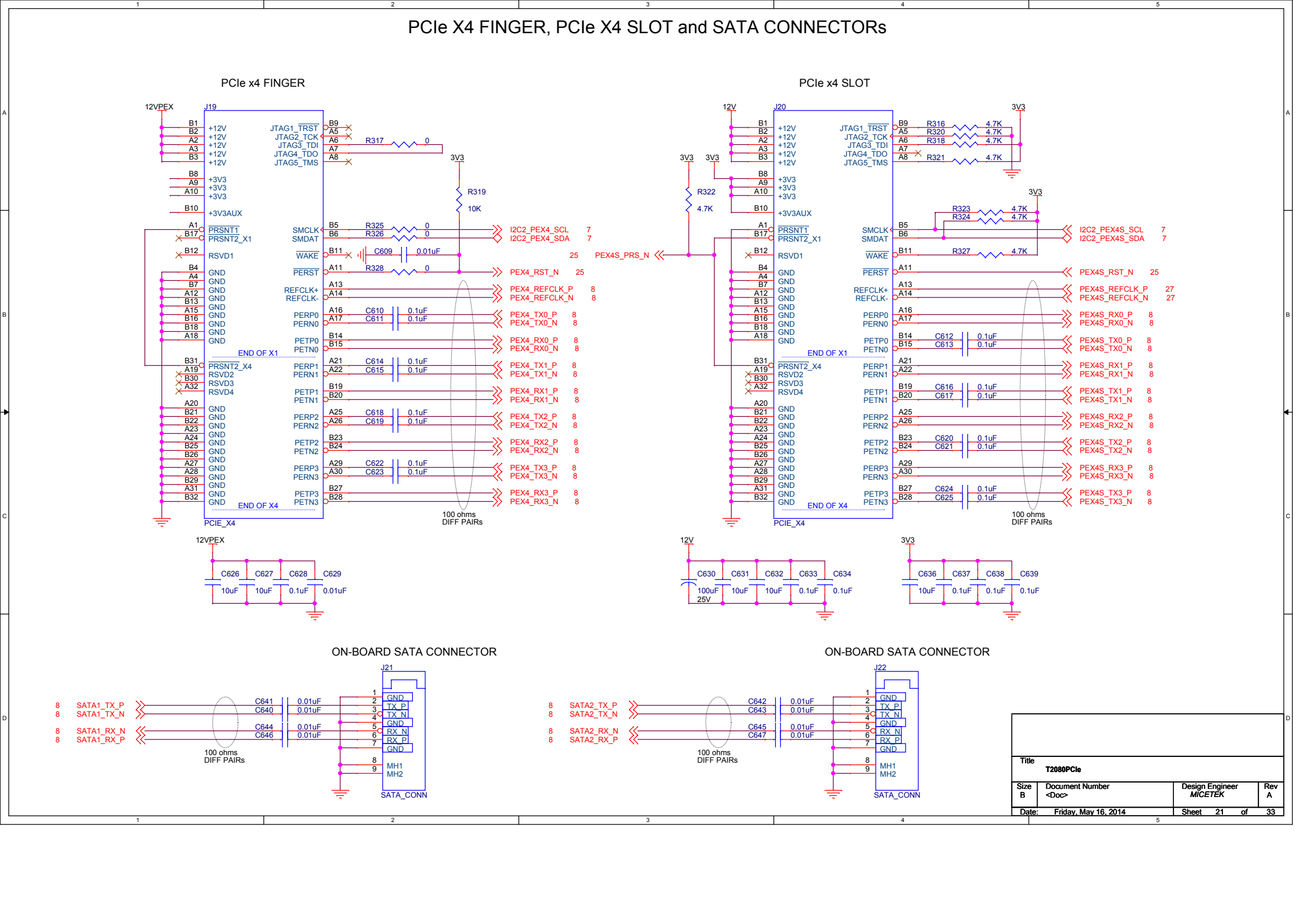
PCIE X4 SLOT

ON-BOARD SATA CONNECTOR

ON-BOARD SATA CONNECTOR

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PCIE X4 FINGER, PCIE X4 SLOT and SATA CONNECTORS

PCIE x4 FINGER

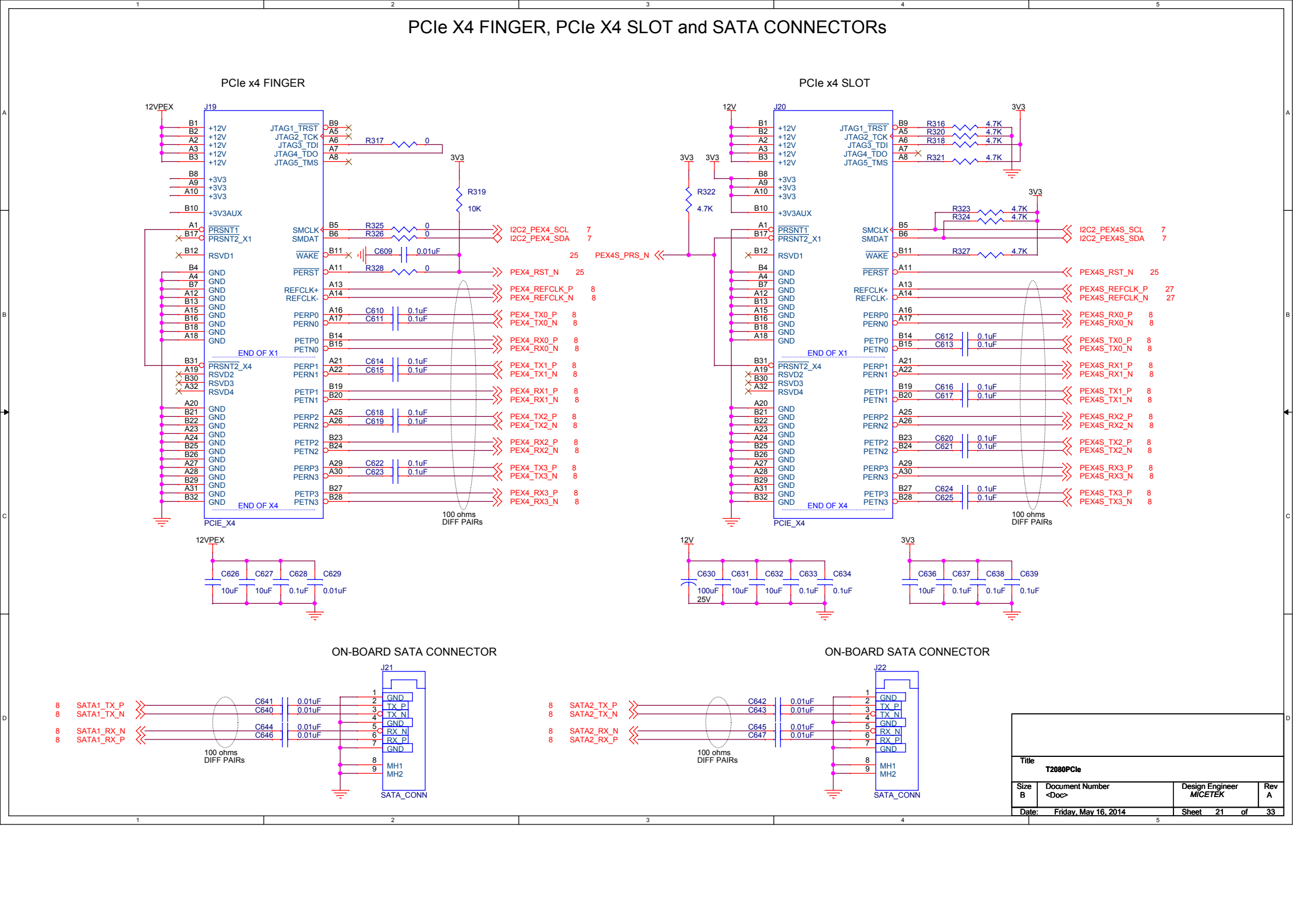
PCIE x4 SLOT

ON-BOARD SATA CONNECTOR

ON-BOARD SATA CONNECTOR

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PCIE X4 FINGER, PCIE X4 SLOT and SATA CONNECTORS

PCIE x4 FINGER

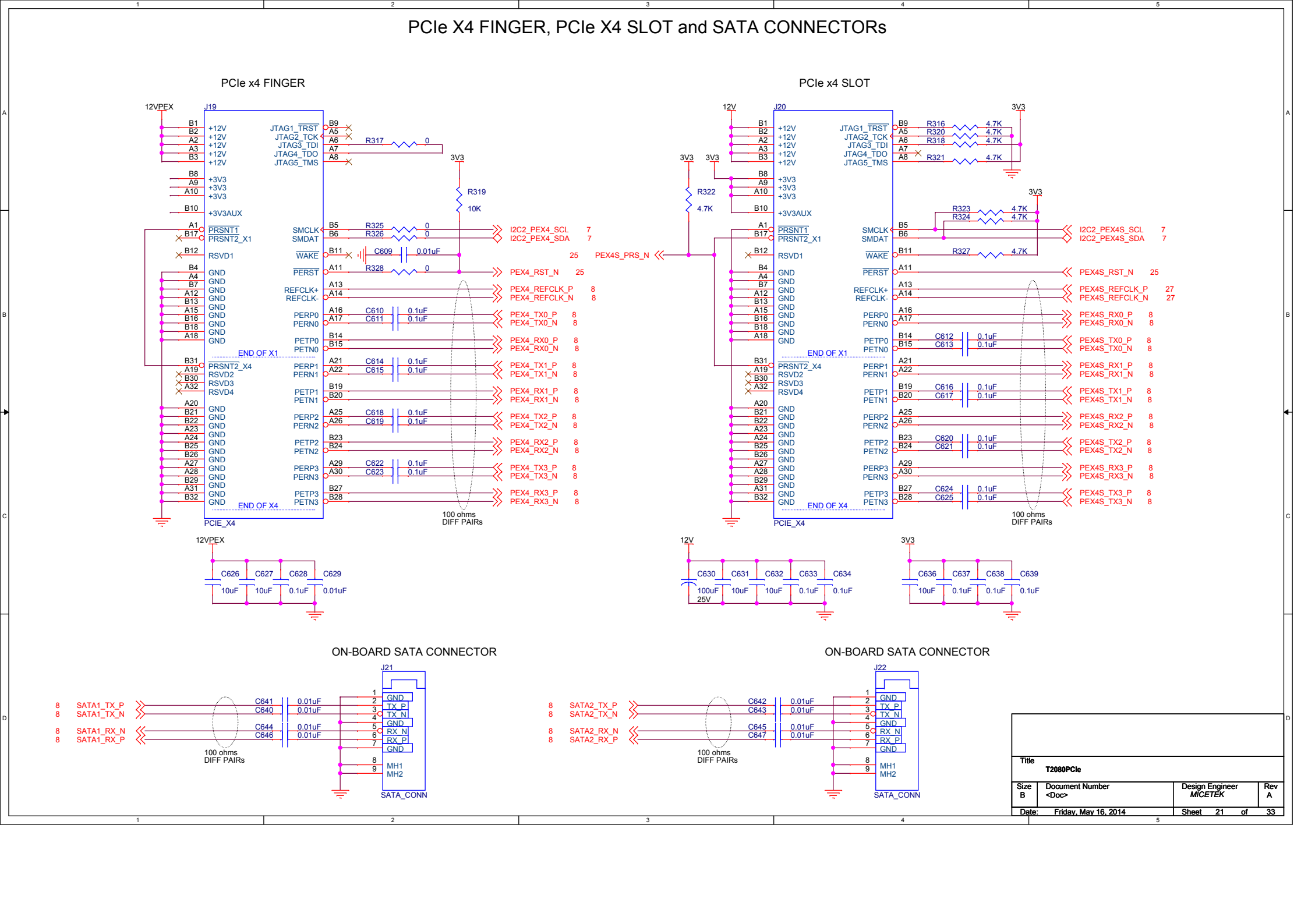
PCIE x4 SLOT

ON-BOARD SATA CONNECTOR

ON-BOARD SATA CONNECTOR

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PCIE X4 FINGER

PCIE X4 SLOT

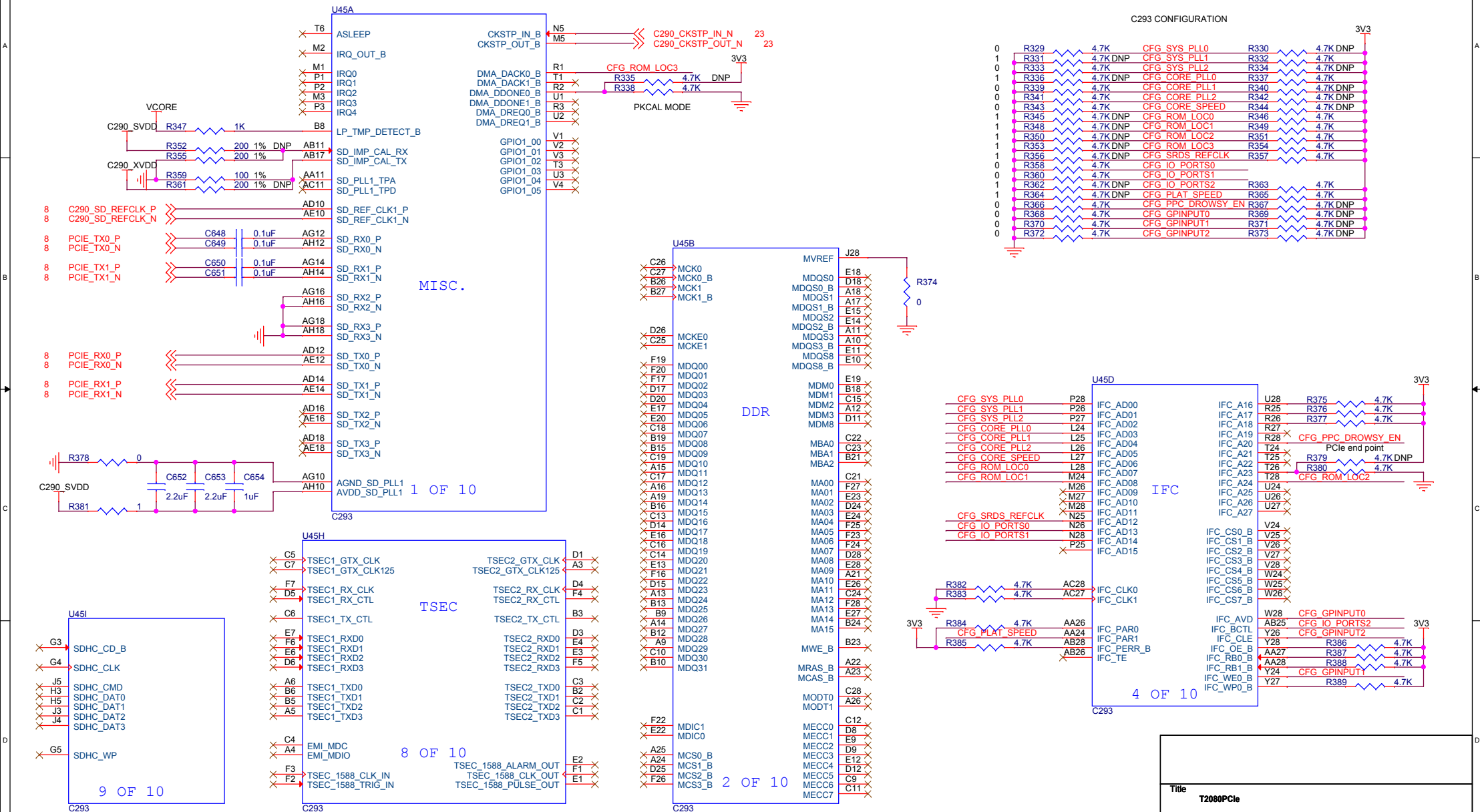
ON-BOARD SATA CONNECTOR

ON-BOARD SATA CONNECTOR

Title: T2080PCIe

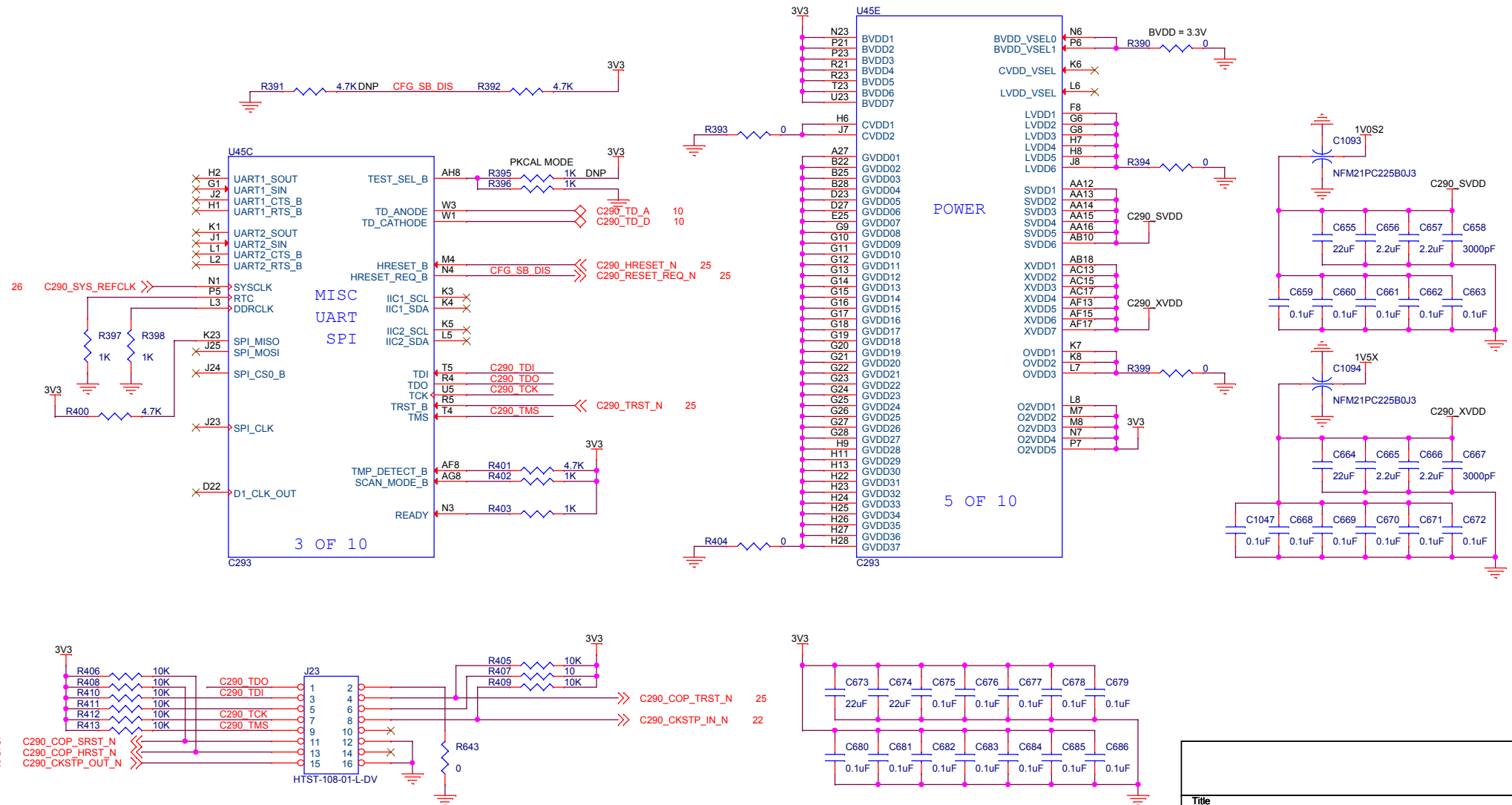
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C293 COPROCESSOR (part 1 of 3)



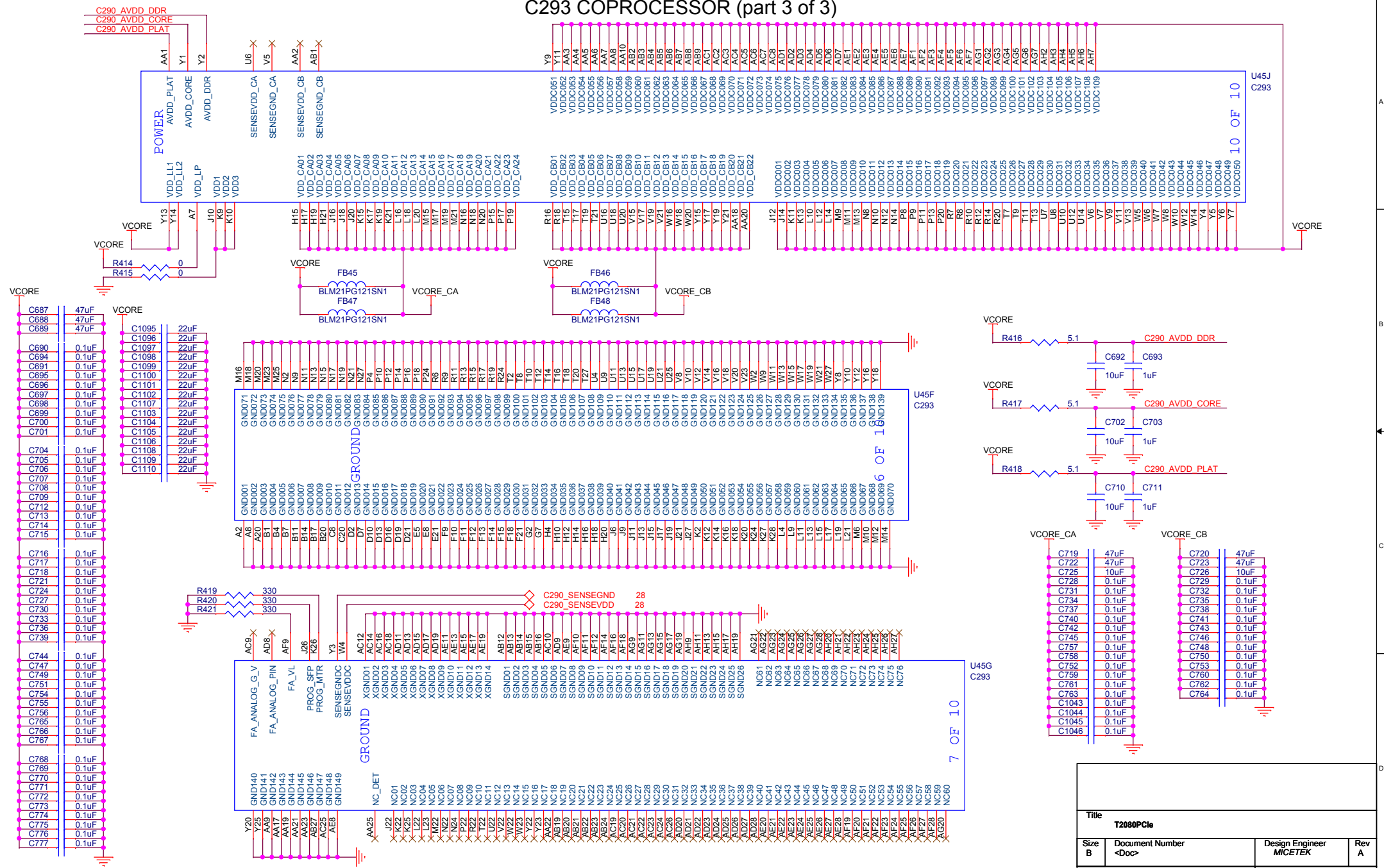
<div style="text-align: right;">D</div>			
Title T2080PClo			
Size B	Document Number <Doc>	Design Engineer <i>MICETEK</i>	Rev A
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C293 COPROCESSOR (part 2 of 3)



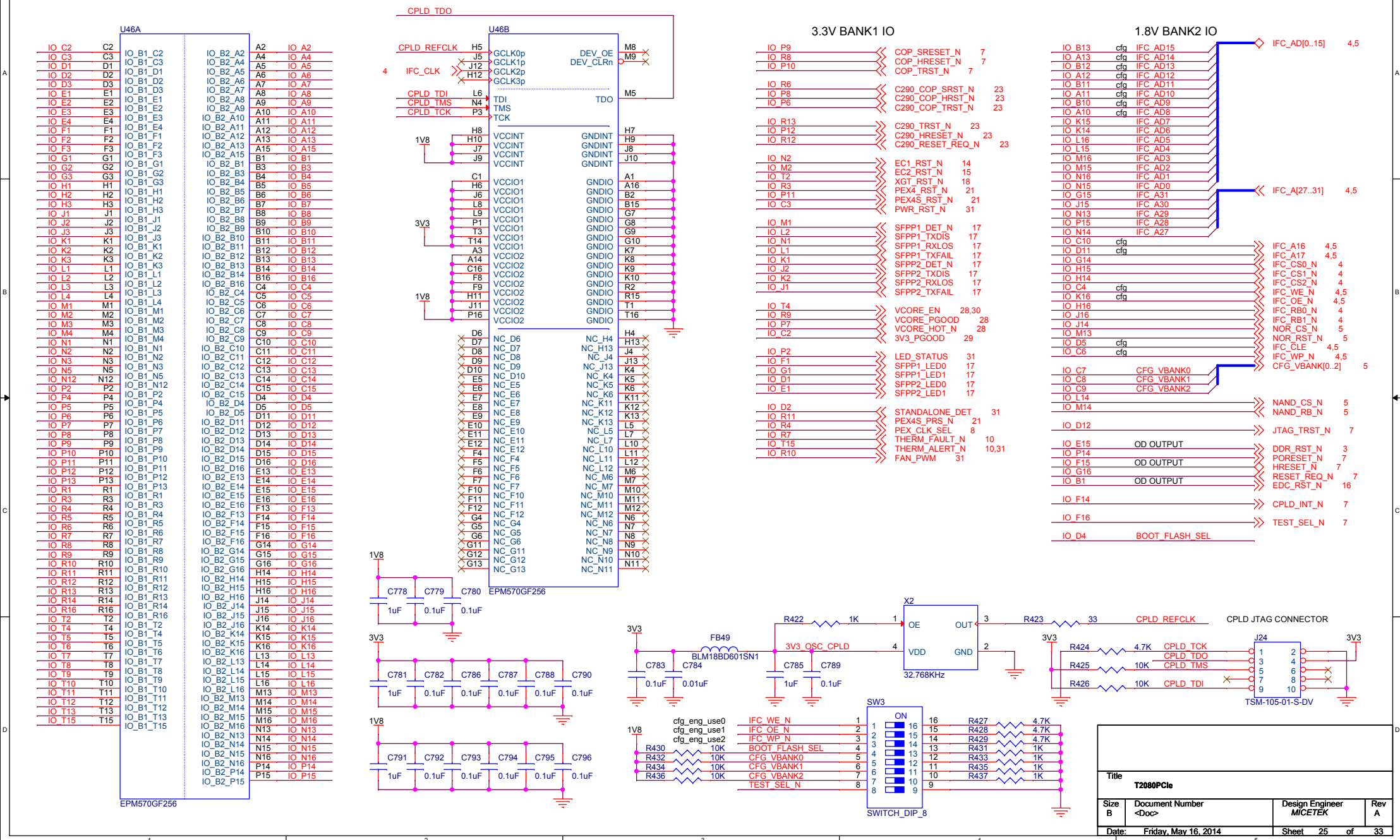
Title				
T2080PC1c				
Size B	Document Number <Doc>	Design Engineer <i>MICETEK</i>	Rev A	
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C293 COPROCESSOR (part 3 of 3)

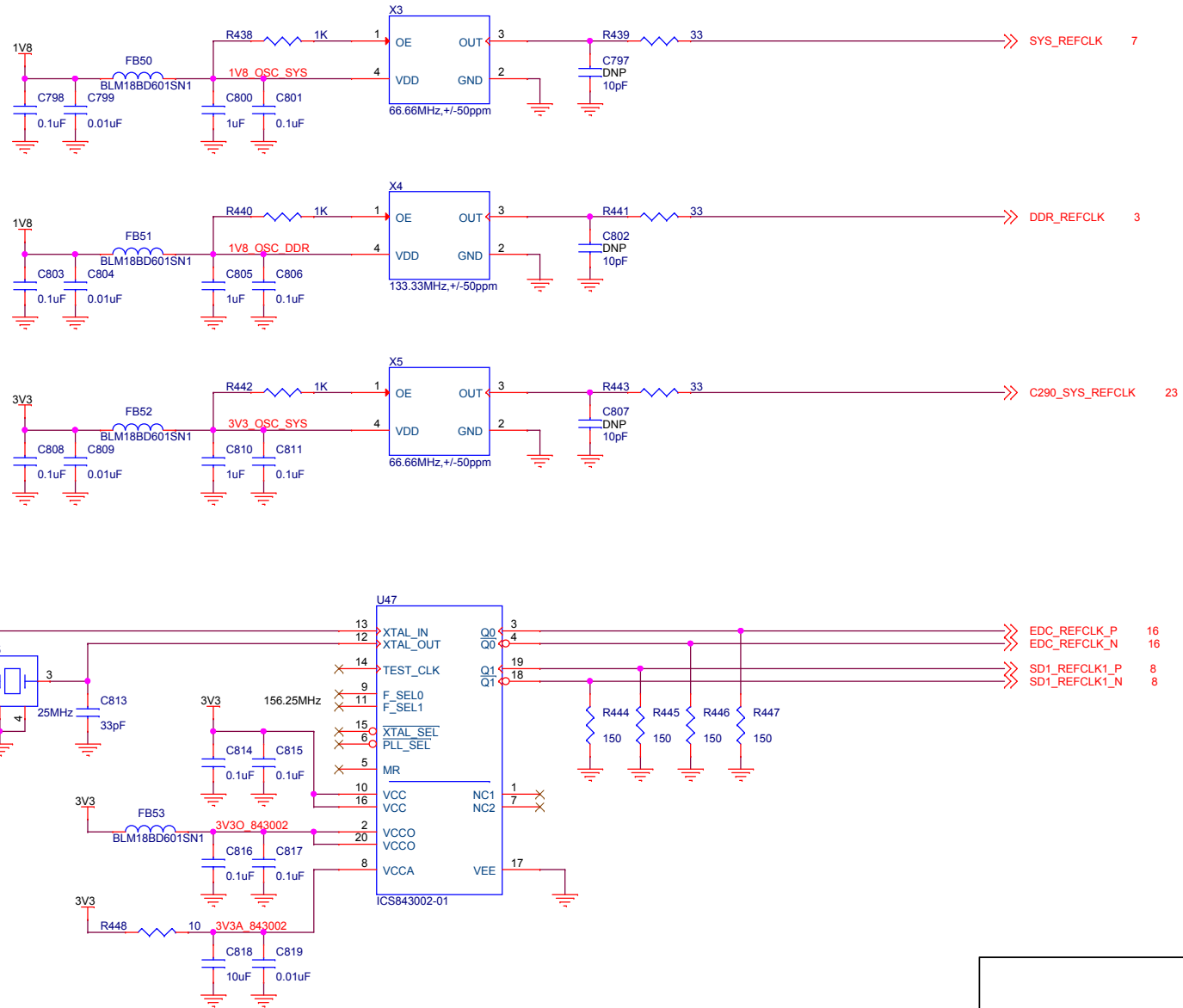


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CPLD

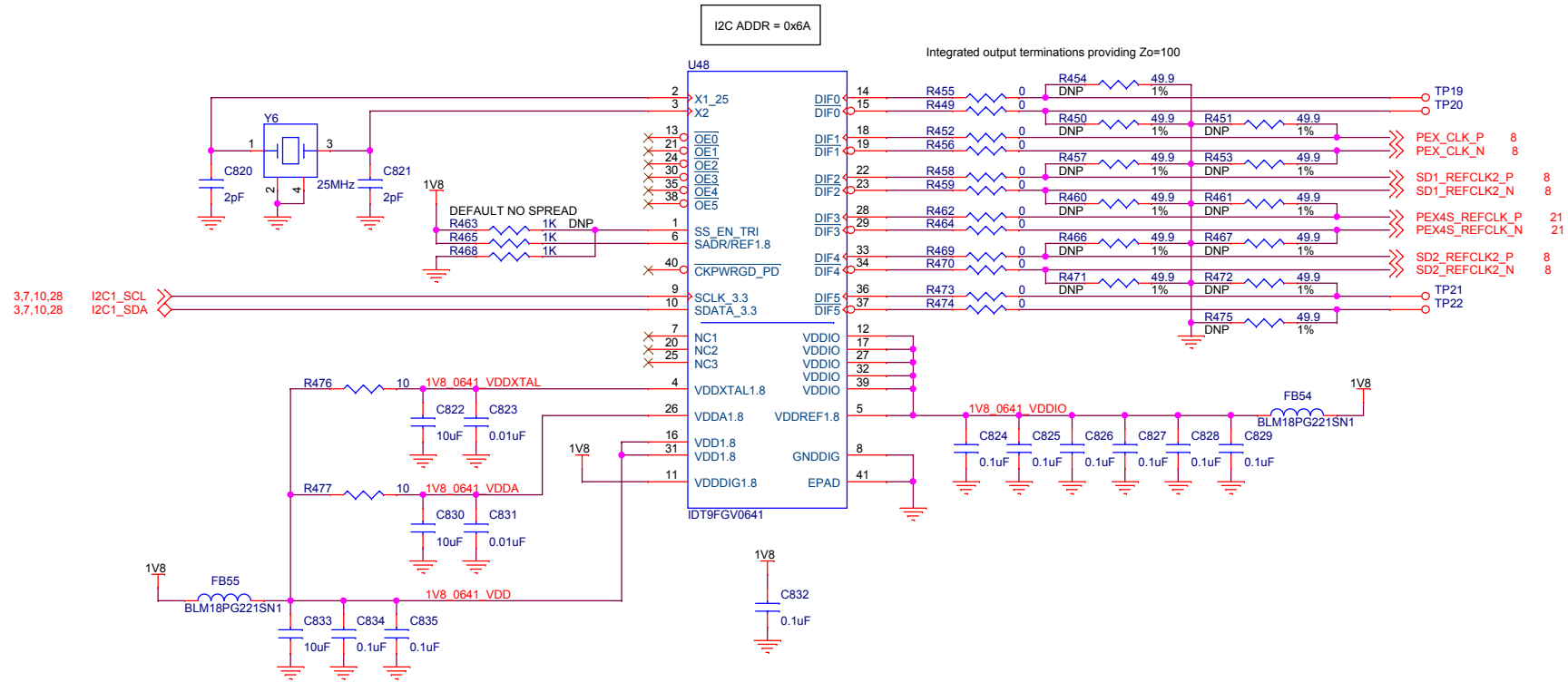


SYSTEM CLOCK GENERATORS



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SYSTEM CLOCK GENERATORS (cont.)

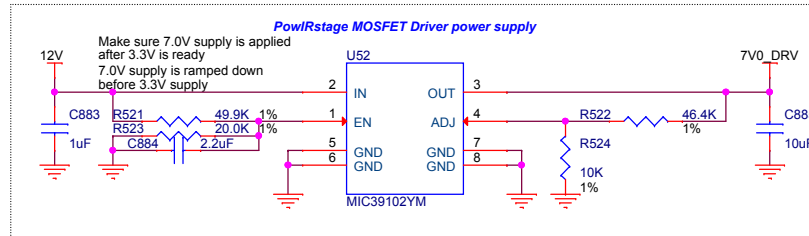
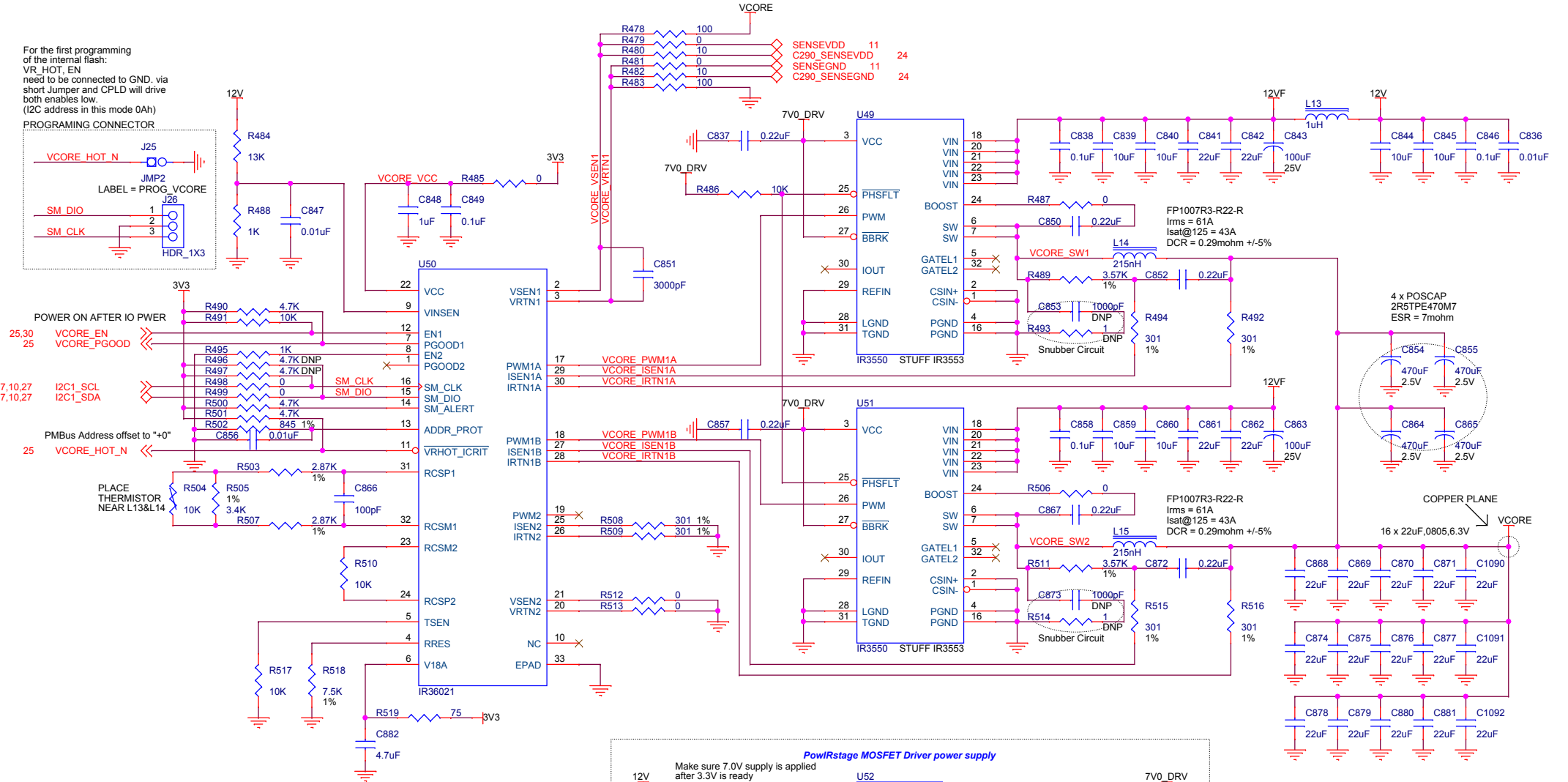
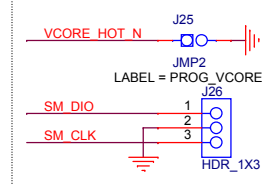


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T2080 CORE POWER CONVERTOR

For the first programming of the internal flash: VR_HOT_EN need to be connected to GND. via short Jumper and CPLD will drive both enables low. (I2C address in this mode 0Ah)

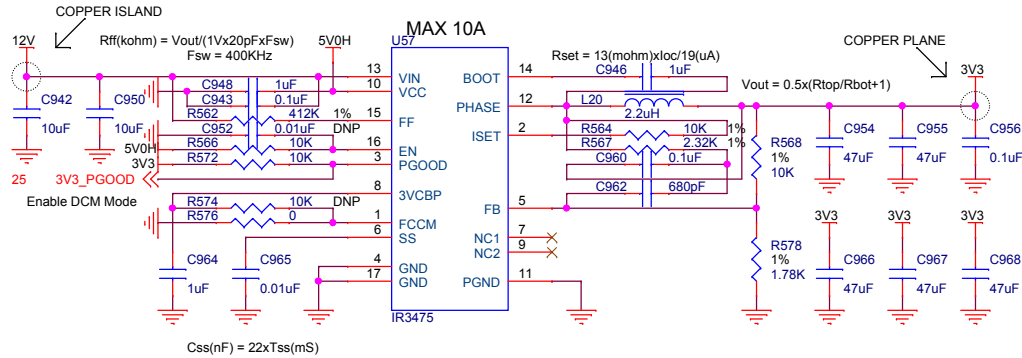
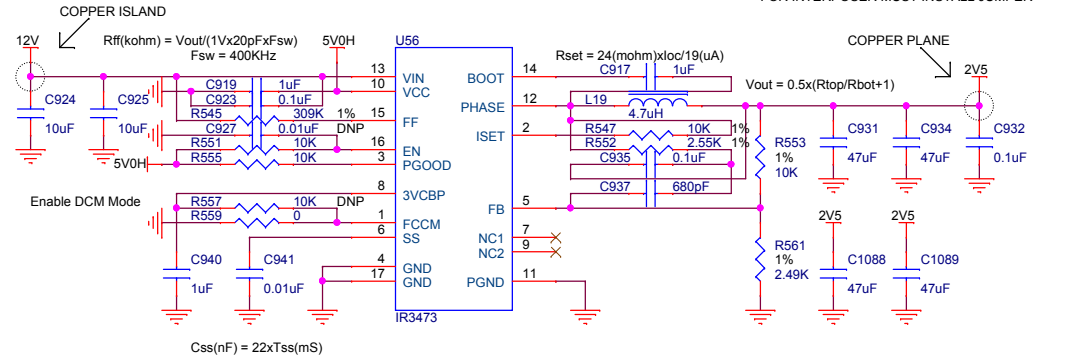
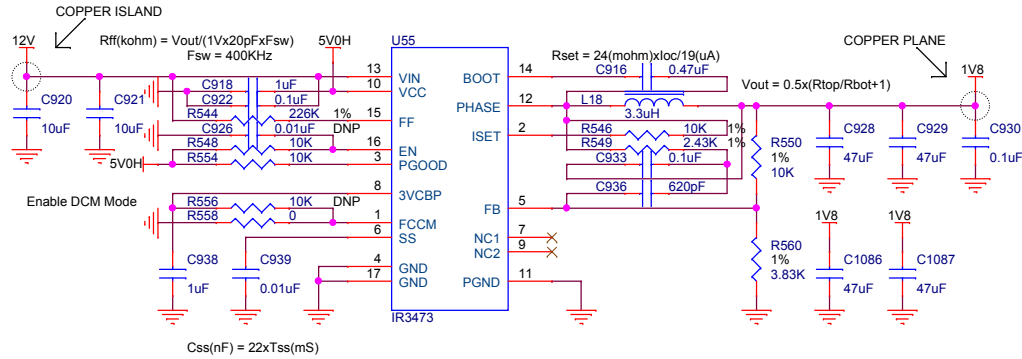
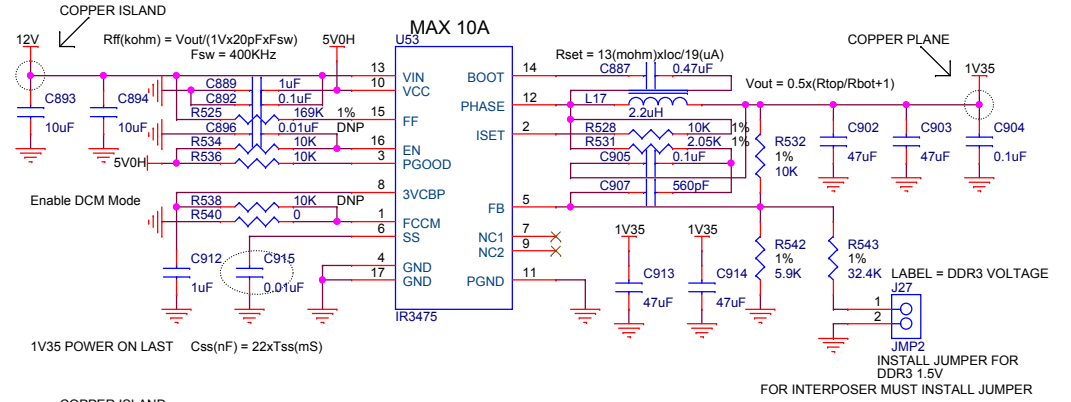
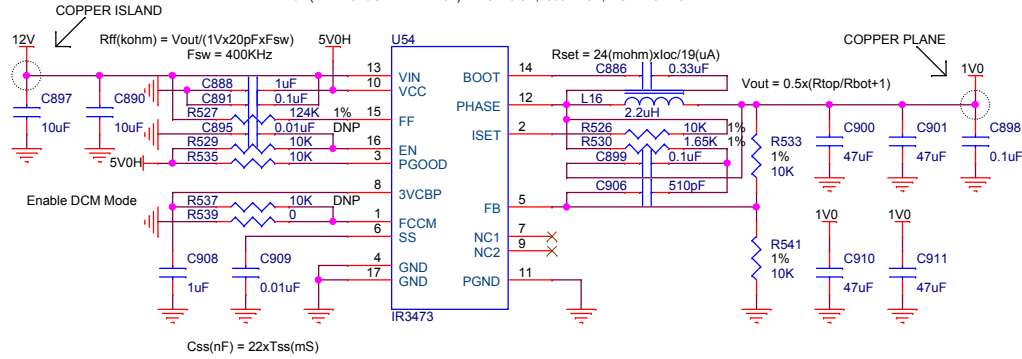
PROGRAMING CONNECTOR



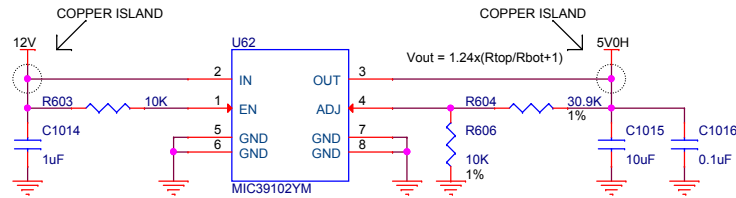
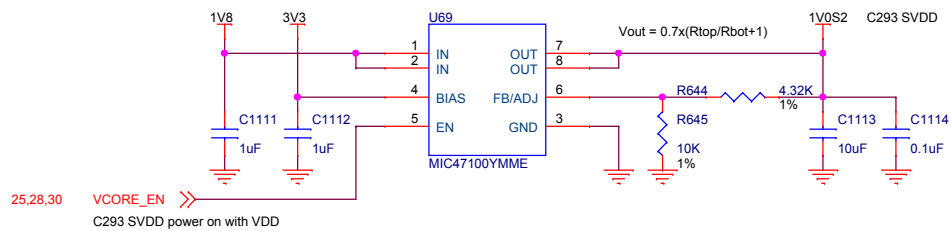
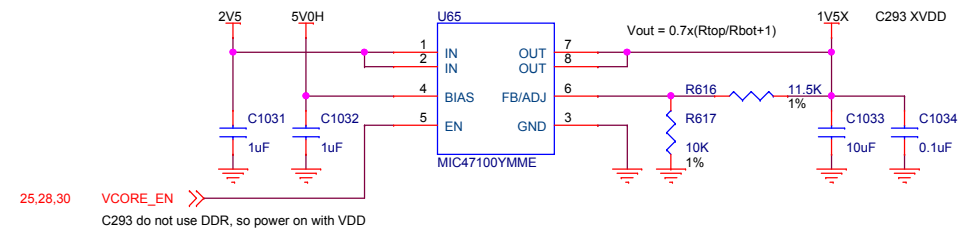
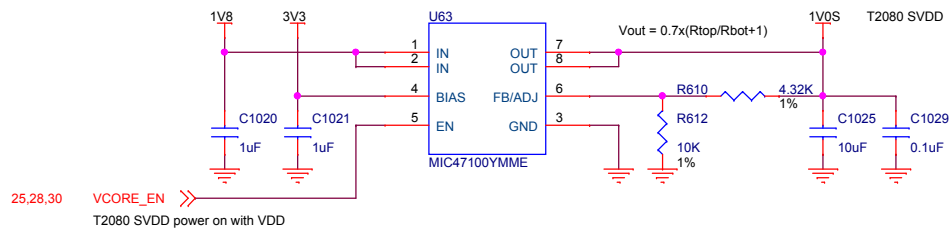
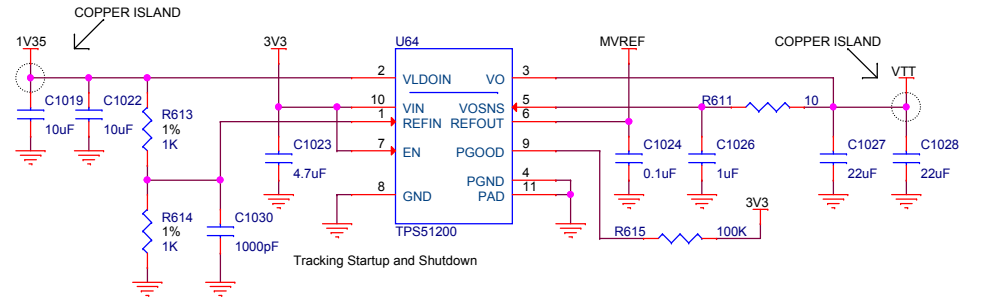
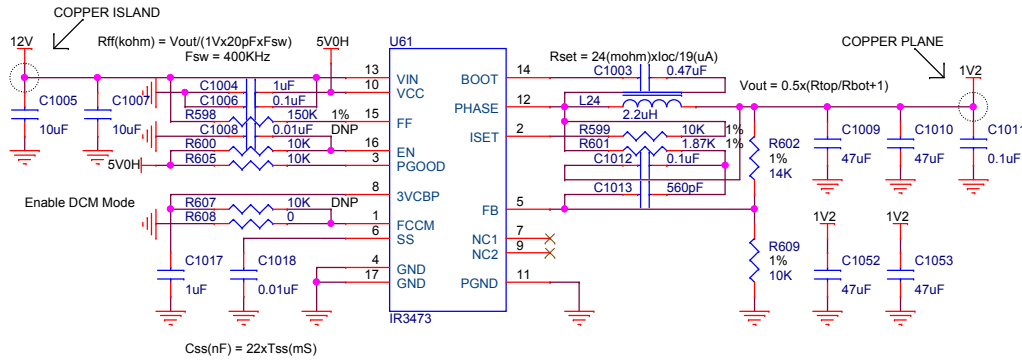
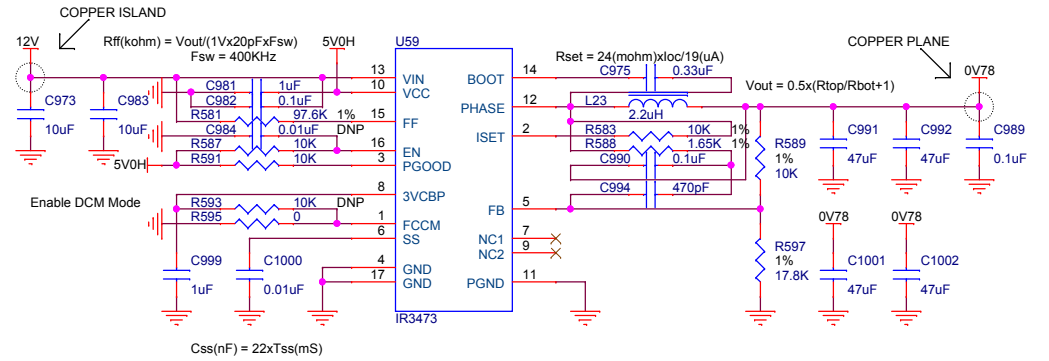
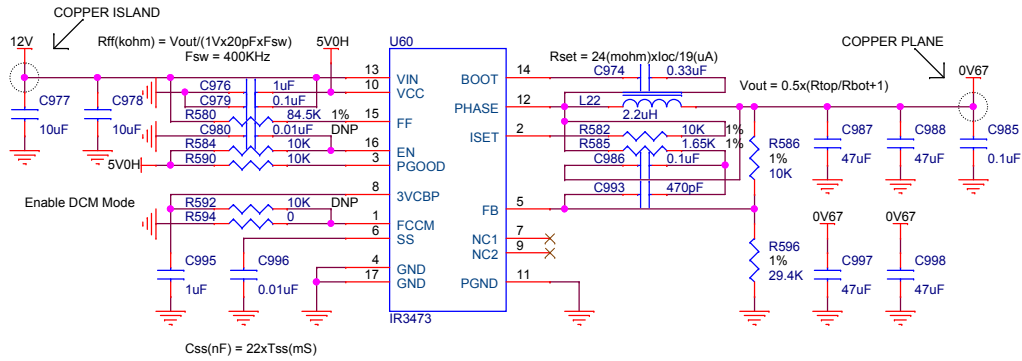
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SYSTEM POWER CONVERTORS

2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
 3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
 4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

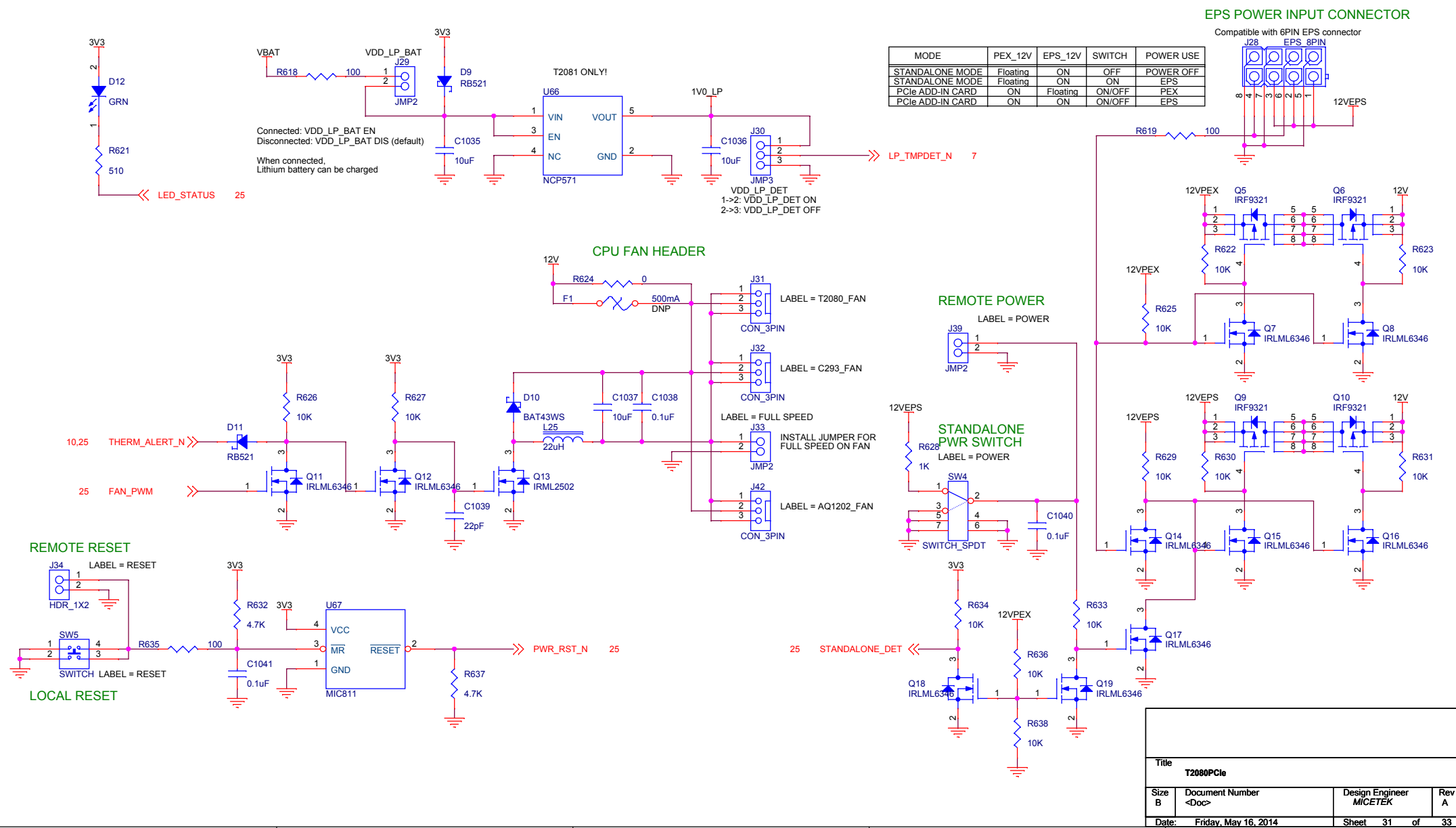


SYSTEM POWER CONVERTORS (cont.)



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SYSTEM POWER INPUT

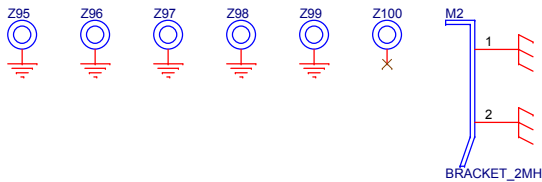


MECHANICALs

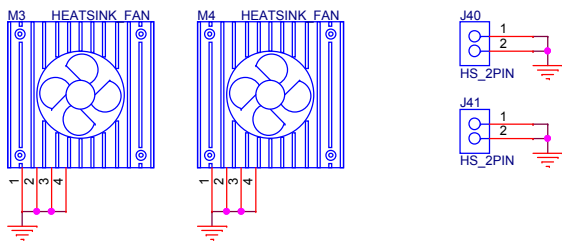
Fiducial Marks



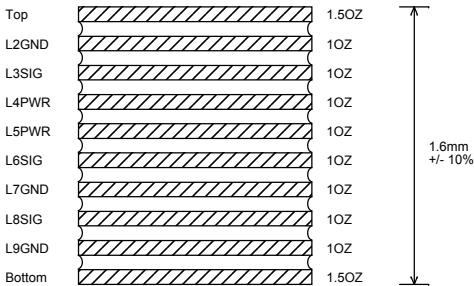
Mouting Holes



Heatsink Fan



Layer Detail



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CHANGE LIST

- 2013/7/19
- 1. Add 20K pull-up to IFC_A[16-19],AVD,OE,WE,WP
 - 2. Add IFC_LATCH_N to IFC voltage level translators
 - 3. Change NAND RB pull-up to 1K
 - 4. Change SD card ESD chip to Rclamp0524J
 - 5. Change NOR MPN to S29GL01GP11TFIV10
 - 6. Add 1.0V LDO for S1VDD, use NFM55PC155F1H4B instead of BLM18 bead for SVDD and XVDD
 - 7. Add 0.22uF to AVDD_CGA, PLAT and D1 voltages
 - 8. Add a 0.1uF debounce cap to power on switch
 - 9. Update IR power regulators refer to IR's comments
 - 10. Change SD card insert and protect signal pull-up to 1.8V and connect to T2080 directly
- 2013/7/24
- 1. Change I2C MUX address to 0x77
 - 2. Add test point for CLK_OUT and RTC, change RTC pull-down to 10K
 - 3. Add test point for 1588 signals
 - 4. Change USB protect chip from SRV05-4 to VBUS054B-HSF
 - 5. Change LED drive resistor from 330ohm to 510ohm
 - 6. Add test points for SD_PLL_TPA and SD_PLL_TPD
 - 7. Add optional filtering for USB_BIAS
 - 10. Connect RGMII PHY tap pins together, change crystal caps from 20pF to 27pF, remove bead, add 0 ohm to ENSWREG, change RST to pull-up
- 2013/8/27
- 1. Update IR3473/IR3475 circuit, following T1040/T1042RDB
 - 2. Change SVDD and XVDD filter cap from NFM55PC155 to NFM21PC225
 - 3. Swap AQ1202 P1 MDI order
 - 4. Change NAND Flash from TSOP48 to BGA, so can delete 1.8V to 3.3V voltage translator
 - 5. Change SD card to TF card for space saving, like T4240PCle board
 - 6. Change battery socket to lithium rechargeable battery for space saving
 - 7. Update C293 part circuit in PKCAL mode
 - 8. Change ADT7461 to ADT7481 for sense T2080 and C293
 - 9. Add FAN header for C293
 - 10. Change EMI2 voltage from 1.8V to 1.2V, change CS4315 IO_VDD_SEL pull-down to select MDIO operates at 1.0V
 - 11. Add 1uH inductor for VCORE 12V filter
 - 12. Change mini PCIe to PCIe x4 slot
- 2013/9/1
- 1. Add P2041 interposer support
 - 2. Change NAND Flash from BGA to TSOP48
 - 3. Change SFP+ RS0/1 signal to CPLD, add pull-up/down resistor
 - 4. Change 100M diff clock chip to IDT9FGV0641
 - 5. Add C293 VDD sense to IR36021
- 2013/9/5
- 1. Change PCIe slot footprint from DIP to SMT
- 2013/9/12
- 1. Add notes at page 1
- 2013/10/15
- 1. Remove interposer support
 - 2. Change UART RJ45 connector to 2x3pin header
 - 3. Change RGMII PHY RJ45 to with magnetic module
- 2013/11/26
- 1. Change IR36021 address offset to +0
- 2013/12/1
- 1. Add 1.0V LDO for C293 SVDD
 - 2. Add 0ohm to COP PIN2

Title			
T1040RDB			
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