

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPPG SHALL MEET IPC-4101B-26, 83 or 98.

T_g - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
T_g - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - SEE TABLE 'B'
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE: .008"/.005"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
 .05080 - .232 MICRON (2.00 - 2.06 MICRONINCH) OF GOLD OVER
 2.540 - 6.350 MICRON (100.00 - 250.00 MICRONINCH) OF NICKEL.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. ADD TEARDROPS TO ALL SIGNAL LAYERS.

15. 2 SOLDER SAMPLES TO BE PROVIDED.

16. BASIC GRID INCREMENT AT 1:1 IS .0001.

17 SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP ~~PG~~

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE $\pm .002$ IN REFERENCE TO THE PRIMARY DATUM.

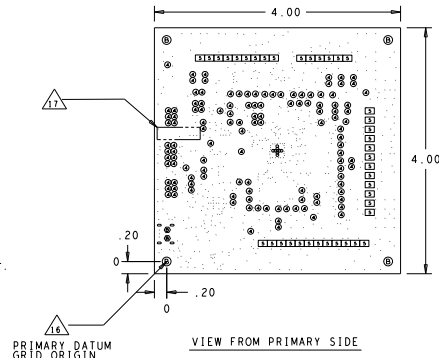
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURING REQUIREMENT. ADDITION OF .25" RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER AND FAB HOUSE. PANELIZATION MUST BE APPROVED BY FREESCALE.

22. THIS BOARD USES VIA-IN-PAD:

A. VIA-IN-PAD TO BE FILLED WITH NON-CONDUCTIVE VIA FILL.
LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.

B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.

23. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS
KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES



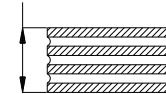
DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

LAYERS	SINGLE ENDED		DIFFERENTIAL		
	TRACE WIDTH (MILS)	IMPEDANCE (OHMS)	TRACE WIDTH (MILS)	TRACE SPACING "AIR GAP" (MILS)	IMPEDANCE (OHMS)
L1_P5	10.0	50	10.0	12.0	90
L3_PWR	8.0	50			
L4_SS	10.0	50	10.0	12.0	90

0.062" THICK +/-10%

DRILL CHART: TOP TO BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	10.0	0.0/-10.0	PLATED	630
•	10.1	0.0/-10.0	PLATED	9
•	40.0	3.0/-3.0	PLATED	121
⊖	52.0	3.0/-3.0	PLATED	39
⊖	130.0	3.0/-3.0	PLATED	4
•	36.0	2.0/-2.0	NON-PLATED	2
•	67.0x31.0	2.0/-2.0	PLATED	4

.062" THK +/- 10%



FINISHED Cu WEIGHT

1/2 • PLATING
1 oz.
1 oz.
1/2 • PLATING

DETAIL A
LAYER STACKUP
SCALE: NONE

PART NO. <div style="text-align: center; font-size: 1.2em;">170-29826</div>		THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR REVERSE ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP	
--- COMPANY PUBLIC X --- COMPANY INTERNAL --- COMPANY CONFIDENTIAL		NXP SEMICONDUCTORS 6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS .01 .XXX .005 * R90 ALL MACHINED SURFACES BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS. DIMENSIONS DO NOT TO SCALE. THINNING ANGLE ORTHOGRAPHIC PROJECTION IS USED.		TITLE: <div style="text-align: center; font-size: 1.2em;">PRINTED WIRING BOARD</div> <div style="text-align: center; font-size: 1.2em;">X-KITPF4210EPEVB</div>	
APPROVALS:		DATE:	
DRAWN: UMANI DESIGNED: PRITHI [Lnt]		05-17-17	
CHECKED: ANGELES DATE: 05-17-17		SIZE:	
LEO PAN		CAD FILE NAME:	
DESIGN ENGINEER: QIAO JUN		DWG. NO.:	
05-17-17		FAB-29826	
SCALE: 1/1		NOT TO SCALE (DRAWING)	
SHEET 1		OF 1	