NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE. WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .012"/.007"

7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.

△8 ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS,
    UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

△16 BASIC GRID INCREMENT AT 1:1 IS .0001.

△17 SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

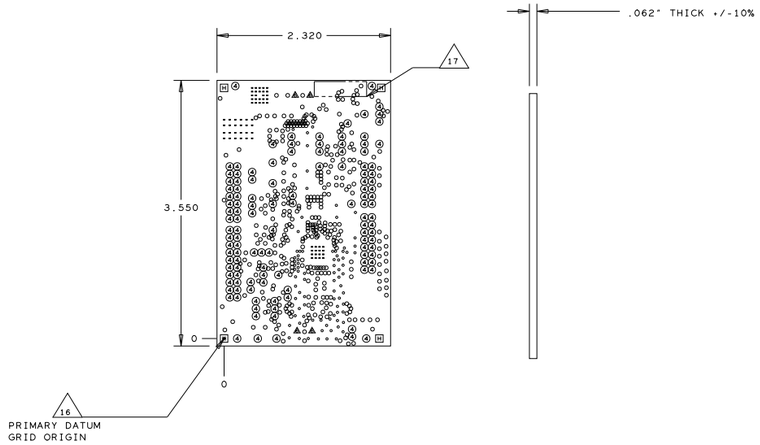
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
    ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.

21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
    THE ADDITION OF RAILS AND .125"NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF
    CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

△22 THIS BOARD USES VIA-IN-PAD:
   A. VIA-IN-PAD TO BE FILLED WITH NON-CONDUCTIVE VIA FILL.
      LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
   B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.

23. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS,
    KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.



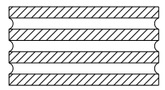
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	04-14-16	J.G.P.

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	NONSTANDARD	QTY
△8 ○	10.0	+0.0/-10.0	PLATED	-	383
△22 VIP	10.1	+0.0/-10.0	PLATED	OTHER	64
○	12.0	+0.0/-12.0	PLATED	-	81
④	40.0	+3.0/-3.0	PLATED	-	122
⚠	63.0	+3.0/-3.0	PLATED	-	4
H	94.0	+2.0/-2.0	NON-PLATED	-	4

FINISHED Cu WEIGHT



LAYER 1	COMPONENT SIDE	1/2 oz.
LAYER 2	GROUND PLANE	1 oz.
LAYER 3	POWER PLANE	1 oz.
LAYER 4	SOLDER SIDE	1/2 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

___ PUBI (PUBLIC INFORMATION)
X IUO (NXP INTERNAL USE ONLY)
___ CP (NXP CONFIDENTIAL PROPRIETARY)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30'
.XXX .005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS, REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN neuronPro-RCC02C	04-14-16
CHECKED JORGE G. POLANCO	04-14-16
DESIGN ENGINEER PRAMIT NANDY	04-14-16

PART NO. 170-28929

NXP SEMICONDUCTORS

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE:
PRINTED WIRING BOARD
FRDM-HB200

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-28929	FAB-28929	A

SCALE DO NOT SCALE DRAWING SHEET OF