NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98

   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL "A"

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL "B"
   5a. THE TRACES FROM J1.1 TO L1.2 AND J2.1 TO L2.2 ARE MEET TO 50 OHMS IMPENDANCE. REST OF THE SIGNALS ARE NON IMPEDANCE.

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.006"

7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. ADD TEARDROPS TO ALL SIGNAL LAYERS.

15. SOLDER SAMPLES TO BE PROVIDED.

16. BASIC GRID INCREMENT AT 1:1 IS .0001.

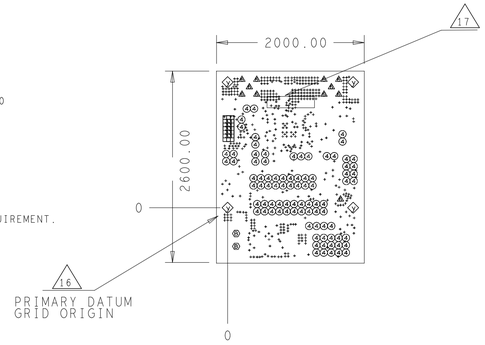
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.

21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURING REQUIREMENT. ADDITION OF .25" RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER AND FAB HOUSE. PANELIZATION MUST BE APPROVED BY FREESCALE.



VIEW FROM PRIMARY SIDE

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	X	ORIGINAL RELEASE	10-15-12	A.Q.
	X1	GPIO REASSIGMENT (PTA4 &PTD5)	10-23-12	A.Q.
	X2	RE-PLACE/ REROUTE J18 & J5/RF MATCHING	10-26-12	A.Q.
	A	PRODUCTION RELEASE	11-07-12	A.Q.
	B	PINOUT UPDATE & MATCHING COMPONENTS	05-28-13	A.Q.
	C	DIO0-PTC3 & DIO1-PTC4 CONNECTED	07-22-13	A.Q.
	D	USB2SERINTERFACE UPDATE, ADD C45&C46	10-22-13	A.Q.

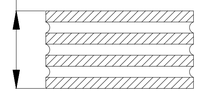
DETAIL B
IMPEDANCE REQUIREMENTS

Layers	Single Ended	
	Trace Width (MILS)	Impedance (Ohms)
L1_PS	18.00	50

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	8.0	+0.0/-8.0	PLATED	493
D	31.0	+2.0/-2.0	PLATED	10
◎	40.0	+3.0/-3.0	PLATED	86
▲	63.0	+3.0/-3.0	PLATED	11
◎	36.0	+2.0/-2.0	NON-PLATED	2
◈	125.0	+4.0/-4.0	NON-PLATED	4

.034" THK +/- 10%



		FINISHED Cu WEIGHT
LAYER 1	COMPONENT SIDE	1/2 oz.
LAYER 2	L2_GND	1 oz.
LAYER 3	L3_PWR	1 oz.
LAYER 4	SOLDER SIDE	1/2 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

--- PUBI (PUBLIC INFORMATION)
X FIUO (FREESCALE INTERNAL USE ONLY)
--- FCP (FREESCALE CONFIDENTIAL PROPRIETARY)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX .01 .0-30'
.XXX .005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS, REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN ANTONIO QUIROZ	10-22-13
CHECKED PABLO MUNOZ	10-22-13
DESIGN ENGINEER ANTONIO QUIROZ	10-22-13

PART NO. 170-27792

FREESCALE SEMICONDUCTOR
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
MRB-KW019032

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-27792	FAB-27792	D

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1