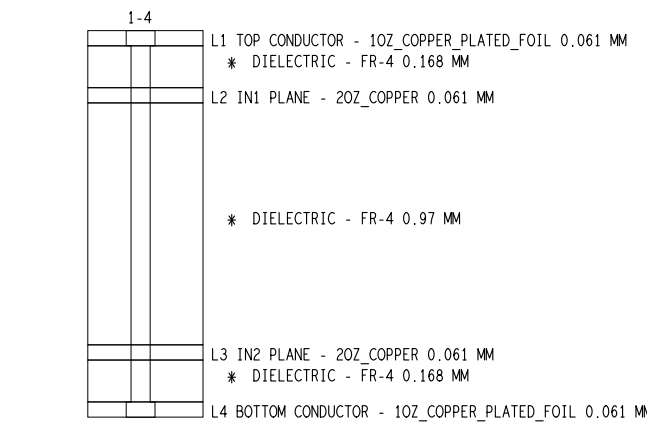
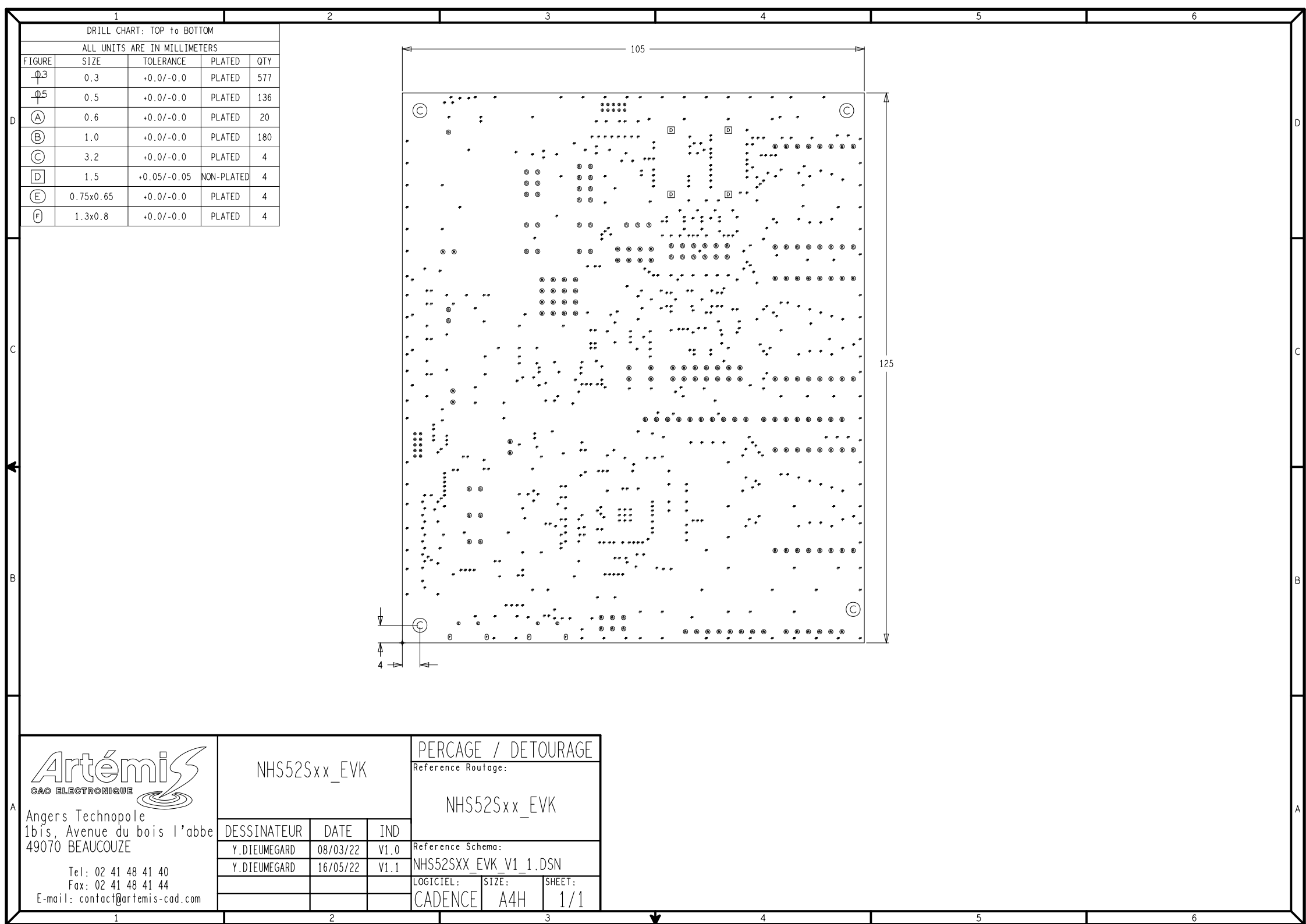


NOTES (UNLESS OTHERWISE SPECIFIED):

ZONE	REV	REVISIONS				
		DESCRIPTION	DATE	APPROVED		
				DE	PE	CAD
	A	ORIGINAL RELEASE	XX - XX - XX	X . X .	X . X .	X . X .

3. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
 - T_g - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
 - T_d - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - NO REQUIREMENT.
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE 0.2mm/0.2mm
7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).
8. FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.
9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
RED COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
TYPE: LPI OR EQUIVALENT.
 - A. LOCATION = $\pm .002$ " OF PLATED PADS.
 - B. DIAMETER OR SIZE = $\pm .002$ OF ORIGINAL DATA
10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS.
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. TWO SOLDER SAMPLES TO BE PROVIDED.
16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)
18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE $\pm .002$ IN REFERENCE TO THE PRIMARY DATUM
UNLESS OTHERWISE SPECIFIED.
20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF
CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
21. THIEVING REQUIREMENT:
COPPER THIEVING ADDITION IS NOT ALLOWED.



DESIGN CROSS SECTION CHART
TOTAL THICKNESS 1.55 MM
ALL VALUES ARE FINISHED VALUES.
BOARD THICKNESS TOLERANCE +/- 10%

DETAIL A
LAYER: STACK
SCALE: NONE

PART NO. <div>170-95578</div>		NXP SEMICONDUCTORS	
--- COMPANY PUBLIC <input checked="" type="checkbox"/> COMPANY INTERNAL --- COMPANY CONFIDENTIAL		THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.	
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DIMENSIONS ARE: .XX .01 .XXX .005 ✓ RMS ALL MACHINED SURFACES BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS. UNDERLINE DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.		APPROVALS DRAWN XXXXX CHECKED XXXXX DESIGN ENGINEER XXXXX	
ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES LISTED IN THE COMMISSION DELEGATED DIRECTIVE (EU) 2015/863, ANNEX I TO DIRECTIVE 2011/65/EU, ANNEX II TO DIRECTIVE 2011/65/EU, OR ANNEX I TO DIRECTIVE 2011/65/EU, AS REQUIRED UPON REQUEST.		TITLE: PRINTED WIRING BOARD MCXW23-EVK-BB	
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