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Revisions			
Rev	Description	Date	Approved
X1	Preliminary SCH design	08-JUL-2020	Amish D.
A	Agile Release	06-AUG-2020	Amish D.
A1	Replaced D3 & Y2	20-AUG-2021	Amish D.


LPC55S06-EVK

Niobe4-Nano

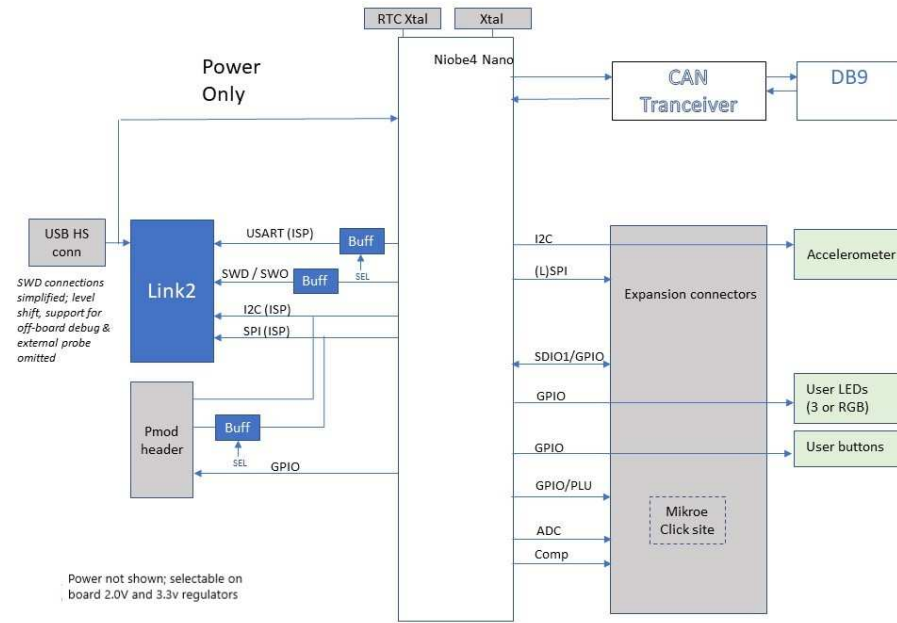
This Color is for Silk

This Color is for User Notes

This Color is for CAD Notes

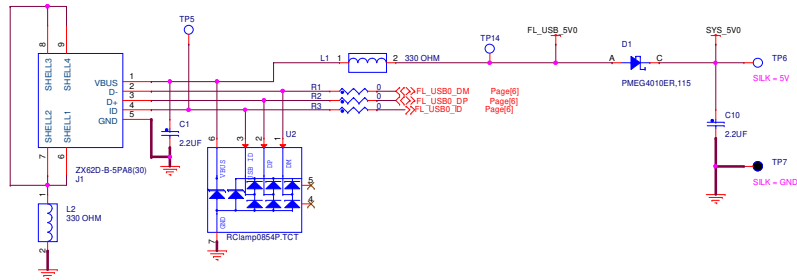
		Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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Designer: Fernanda Isles	Drawing Title: LPC55S06-EVK		
Drawn by: Fernanda Isles	Page Title: Title, TOC & Rev		
Approved: Amish D.	Size: C	Document Number: SCH-47516 PDF: SPF-47516	Rev: A1
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System Block Diagram

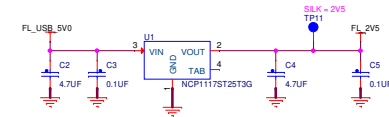


Classification: Company Internal/Proprietary			
Drawing Title: LPC55S06-EVK			
Page Title: Block Diagram			
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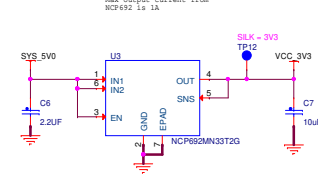
SLK - Link2
Link2
MICRO B



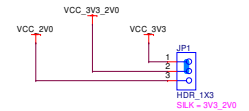
2V5 Regulator



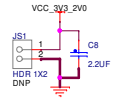
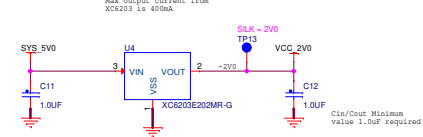
3V3 Regulator



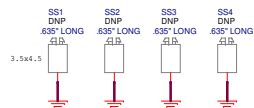
Selector 2V0 || 3V3



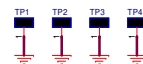
2V0 Regulator



Mounting Holes

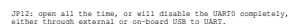


GND TestPads

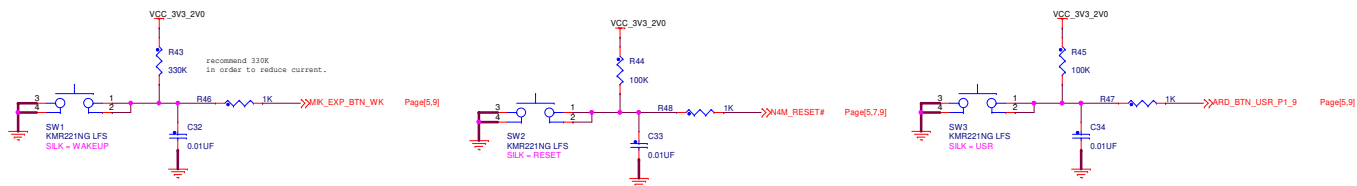


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The diagram illustrates a CAN FD transceiver circuit. It features two 74VHC1450W,125 transceivers (U25 and U26) and a TJA1044GT CAN FD controller (U9). The circuit is powered by VCC_3V3_2V0 and SYS_5V0 rails, with decoupling capacitors (C442, C444, C23) and termination resistors (R159, R29). The CAN bus is connected to a DB9 connector (J19) with a 330 Ohm termination resistor (L7). The diagram is labeled "Page[9]" and "CAN_TXD".



I2C Address 0x1E



Page Title: Peripheral

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VCC_3V3

SY5_5V0

CAD Note: PCB Edge Side

microBUS

CON SKT 8

Page[5,9] ARD_MIK_ADC0_8_N Page[5,9] ARD_MIK_F1_5 Page[5,9]

Page[4,5,7,8] NEM_RESET Page[4,5,8] ARD_MIK_F0_0_TX Page[4,5,8]

Page[5,8,9] ARD_MIK_HSSI_SSEL1 Page[5,8,9] ARD_MIK_F0_1_USART_RXD Page[5,8,9]

Page[5,9] ARD_MIK_HSSI_SCK Page[5,9] ARD_MIK_F0_1_USART_TXD Page[5,9]

Page[5,9] ARD_MIK_HSSI_MISO Page[5,9] ARD_MIK_F0_2_SCL Page[5,9]

Page[5,9] ARD_MIK_HSSI_MOSI Page[5,9] ARD_MIK_F0_2_SDA Page[5,9]

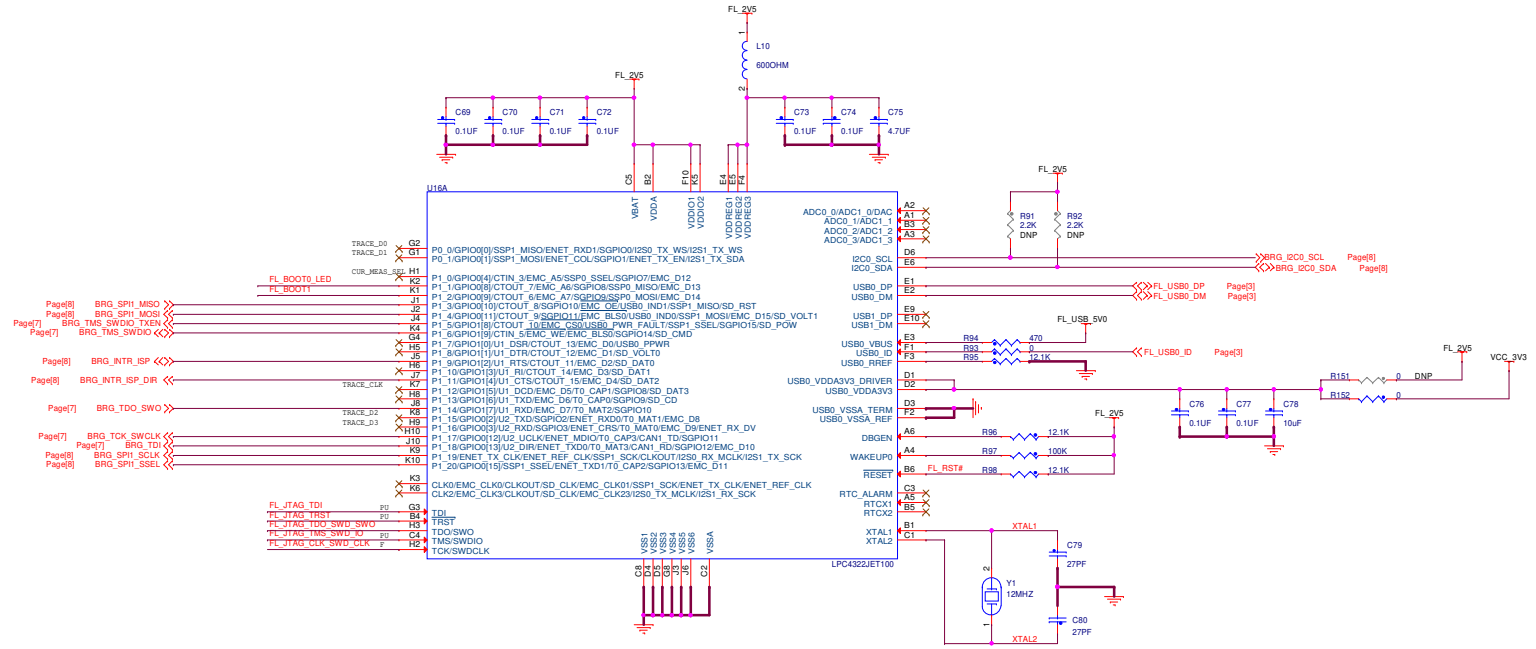
C55 10uF

C56 10uF

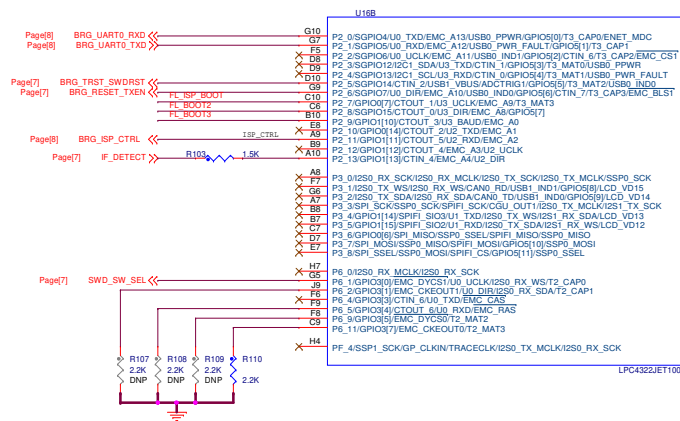
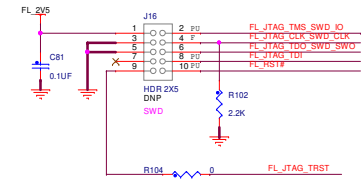
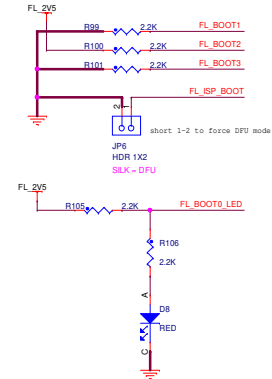
-
- The schematic diagram illustrates the I2C interface circuit. It features three I2C devices connected to a common bus:
- Page[4] (ACC_FC09_IC0_SCL):** Connected to the bus via resistor R77.
 - Page[5] (ARD_MK_FC09_IC0_SCL):** Connected to the bus via resistor R80.
 - Page[6] (ACC_FC09_IC0_SDA):** Connected to the bus via resistor R84.
 - Page[5] (ARD_MK_FC09_IC0_SDA):** Connected to the bus via resistor R88.
- The I2C bus is terminated at both ends with 2.2K resistors (R75 and R74) connected to VCC_3V3_ZV0. The bus also connects to Page[5] (ARD_MK_FC09_IC0_SDA) and Page[9] (ACC_FC09_IC0_SDA).



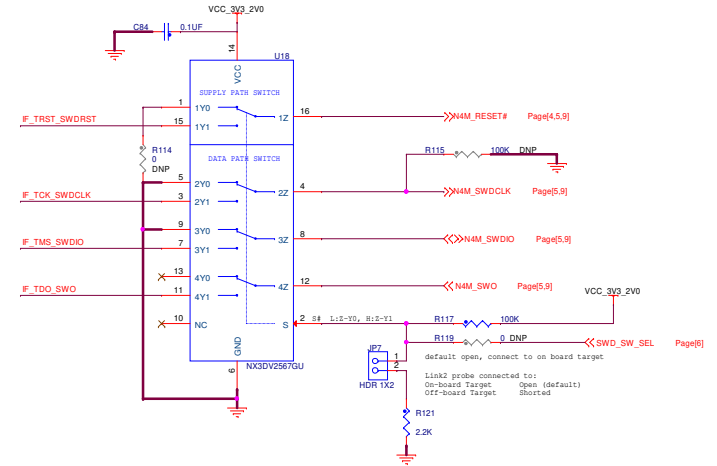
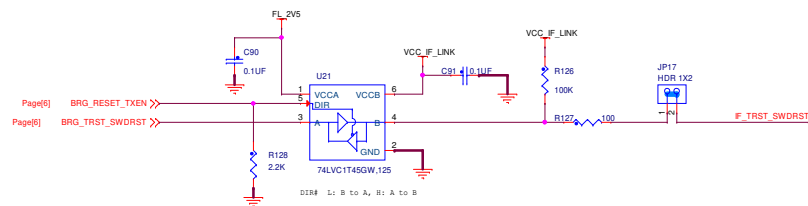
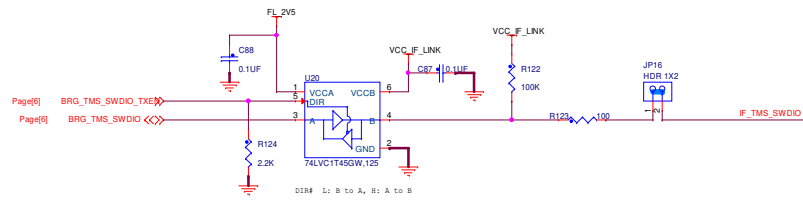
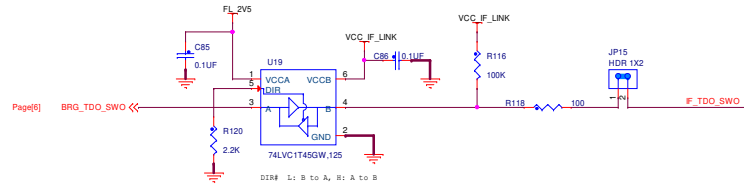
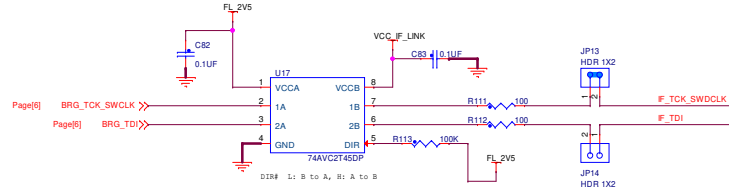
LINK2 MCU



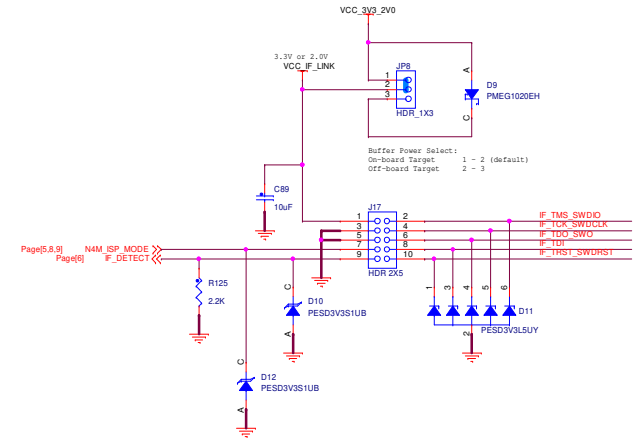
Link2
LPC4322 Boot Mode
DFU USB0 = B3:0 = 0101



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SWD CONN



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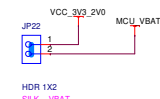
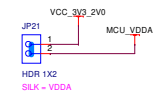
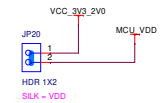


LPC55S06-EVK

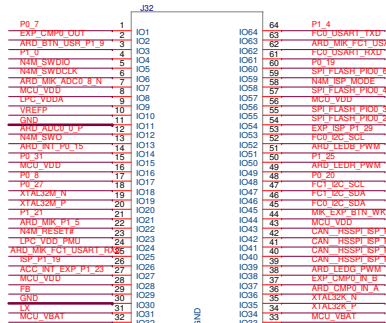
Link2 ISP

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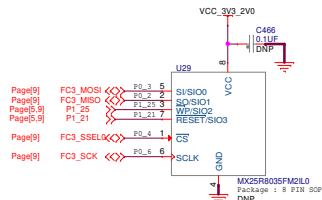
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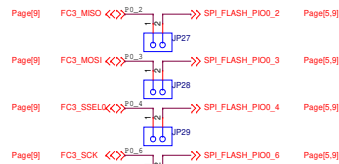
SKT 64 QFP SMT 0.5MM 680H AU



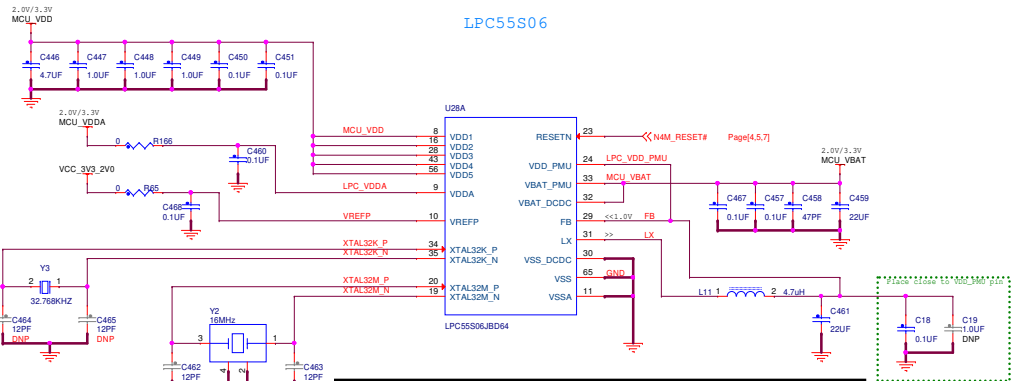
SPI NOR FLASH



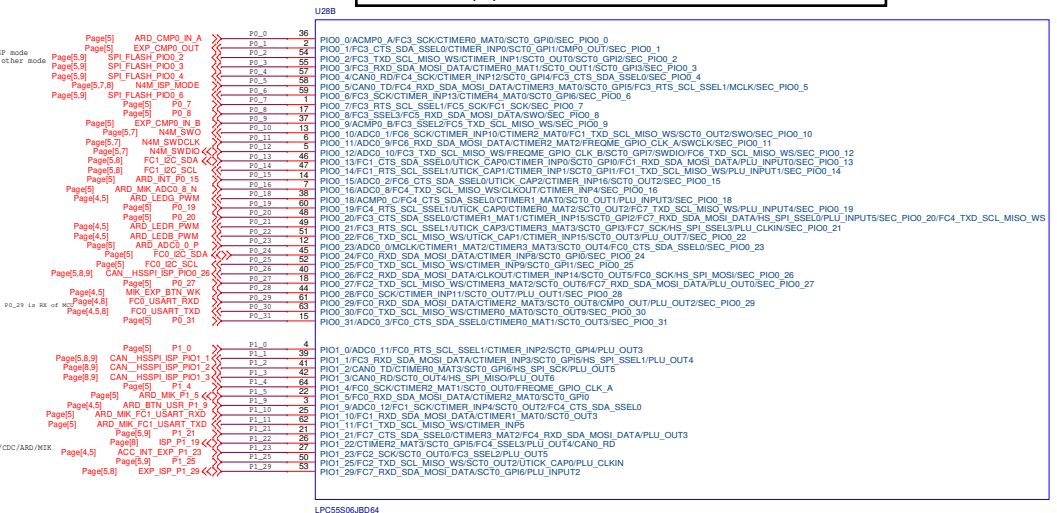
SPI NOR FLASH Mode / SPI Mode



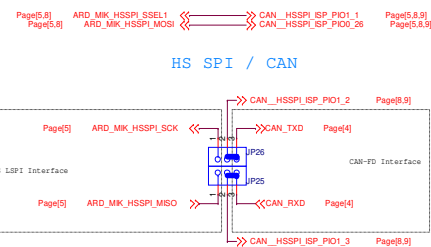
LPC55S06



NOTE:
To meet the Power-up ramp conditions in the Datasheet and Errata (VBAT_DCDC.1), please refer to AN13033 Hardware Design Guidelines for LPC55(S)xx Microcontrollers.



LPC55S06JBD64



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Jumper Table

REF DES	JUMPER(DEFAULT)	PAGE NAME
JP1	1-2	03 - System Power
JP24,JP23	1-2	04 - Peripheral
J3,JP12	OPEN	04 - Peripheral
J11	OPEN	05 - Other Interface
JP6	OPEN	06 - Link2 MCU
JP16,JP17,JP15,JP8,JP13	1-2	07 - Link2 SWD
JP14,JP7,J17	OPEN	07 - Link2 SWD
JS4,JS5	1-2	08 - Link2 ISP
J18,JS3,JP9	OPEN	08 - Link2 ISP
JP20,JP21,JP22	1-2	09 - LPC55S06
JP25,JP26	2-3	09 - LPC55S06
JP28,JP29,JP30,JP27	OPEN	09 - LPC55S06

DNP Table

REF DES	ASSY OPT	PAGE NAME
JS1,SS4,SS3,SS2,SS1	DNP	03 - System Power
R34,R35,R32,R33	DNP	04 - Peripheral
JP4	DNP	05 - Other Interface
R107,R108,R109,R91,R92,J16, R151	DNP	06 - Link2 MCU
R115,R119,R114	DNP	07 - Link2 SWD
R136	DNP	08 - Link2 ISP
C464,C462,C465,C19,C463,U29, C466,J32	DNP	09 - LPC55S06

