


LA1224-RDB-BLS

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Drawn by: Rituraj Anand	Page Title: Cover Page		
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Revisions			
Rev	Description	Date	Approved
A	Release A085	6-June-2022	

Design Note:

1. This design is derived from X-LA1224-RDB-B [51937 RevB].
-U65 part replaced with PLA1238S7S88AB.

2. 51937 RevB PCB has been used for this design.

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Revision Control

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Block Diagram

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Lyr	Image	Vendor
✓cp	0.000 mils	
✓cs	0.000 mils	
✓cm	0.700 mils	
✓1sp	2.325 mils Dk: 3.34 MEG6 1078 (68.0%) 3.428 mils Dk: 3.34 MEG6 1078 (68.0%)	Oak Mitsui
✓2pp	1.200 mils Dk: 3.58 MEG6 (2-1078) HVLP 94% 4.000 mils Dk: 3.58 MEG6 (2-1078) HVLP 14%	Panasonic
✓3sp	0.600 mils Dk: 3.25 MEG6 1035 (70.0%) 4.132 mils Dk: 3.25 MEG6 1035 (70.0%)	Panasonic
✓4pp	1.200 mils Dk: 4.50 R-175SV (1-2116) RTF 94% 4.000 mils Dk: 4.50 R-175SV (1-2116) RTF 6%	Panasonic
✓5sp	0.600 mils Dk: 4.00 R-1650V 1080 (64.0%) 5.184 mils Dk: 4.00 R-1650V 1080 (64.0%)	Panasonic
✓6pp	1.200 mils Dk: 4.50 R-175SV (1-2116) RTF 94% 4.000 mils Dk: 4.50 R-175SV (1-2116) RTF 10%	Panasonic
✓7sp	0.600 mils Dk: 3.80 R-1650V 106 (74.0%) 4.734 mils Dk: 3.80 R-1650V 106 (74.0%)	Panasonic
✓8pp	2.600 mils Dk: 3.90 R-175SV (1-106) RTF 94% 2.000 mils Dk: 3.90 R-175SV (1-106) RTF 90%	Panasonic
✓9pp	2.600 mils Dk: 3.80 R-1650V 106 (74.0%) 4.858 mils Dk: 3.80 R-1650V 106 (74.0%)	Panasonic
✓10pp	2.600 mils Dk: 3.90 R-175SV (1-106) RTF 88% 2.000 mils Dk: 3.90 R-175SV (1-106) RTF 94%	Panasonic
✓11pp	2.600 mils Dk: 4.00 R-1650V 1080 (67.0%) 4.740 mils Dk: 4.00 R-1650V 106 (74.0%)	Panasonic
✓12sp	0.600 mils Dk: 4.50 R-175SV (1-2116) RTF 11% 4.000 mils Dk: 4.50 R-175SV (1-2116) RTF 7%	Panasonic
✓13pp	1.200 mils Dk: 3.58 MEG6 (2-1078) HVLP 94% 5.178 mils Dk: 4.00 R-1650V 1080 (64.0%)	Panasonic
✓14sp	0.600 mils Dk: 3.25 MEG6 1035 (70.0%) 4.150 mils Dk: 3.25 MEG6 1035 (70.0%)	Panasonic
✓15pp	0.600 mils Dk: 3.58 MEG6 (2-1078) HVLP 17% 1.200 mils Dk: 3.58 MEG6 (2-1078) HVLP 94%	Panasonic
✓16sp	0.600 mils Dk: 3.25 MEG6 1035 (70.0%) 3.428 mils Dk: 3.34 MEG6 1078 (68.0%)	Panasonic
✓17pp	2.325 mils Dk: 3.34 MEG6 1078 (68.0%) 0.700 mils	Oak Mitsui
✓18sp	0.000 mils	
✓sm	0.000 mils	
✓ss	0.000 mils	
✓sp	0.000 mils	

Impedance Table										
Layer	Required Impedance (Ohms)	Calculated Impedance (Ohms)	Tolerance (Ohms)	Impedance Type	Reference Layers	Design L/W (mils)	Design Space (mils)	Finished L/W (mils)	Finished Space (mils)	Coplanar Space (mils)
1sp	50.0	47.8	±5.0	se coated microstrip	None / 2pp	6.50	---	6.50	---	---
1sp	100.0	95.5	±10.0	diff coated microstrip	None / 2pp	6.00	16.00	6.00	16.00	---
1sp	90.0	85.9	±9.0	diff coated microstrip	None / 2pp	7.55	18.00	7.55	18.00	---
3sp	50.0	49.5	±5.0	se stripline	2pp / 4pp	4.75	---	4.75	---	---
3sp	100.0	99.1	±10.0	diff stripline	2pp / 4pp	4.65	11.40	4.65	11.40	---
3sp	90.0	89.2	±9.0	diff stripline	2pp / 4pp	5.64	10.50	5.64	10.50	---
5sp	50.0	50.4	±5.0	se stripline	4pp / 6pp	3.60	---	3.60	---	---
5sp	100.0	100.1	±10.0	diff stripline	4pp / 6pp	3.60	12.30	3.60	12.30	---
5sp	90.0	90.8	±9.0	diff stripline	4pp / 6pp	4.40	11.50	4.40	11.50	---
7sp	50.0	49.7	±5.0	se stripline	6pp / 8pp	3.60	---	3.60	---	---
7sp	100.0	99.4	±10.0	diff stripline	6pp / 8pp	3.55	12.30	3.55	12.30	---
12sp	50.0	49.7	±5.0	se stripline	11pp / 13pp	3.60	---	3.60	---	---
12sp	100.0	99.5	±10.0	diff stripline	11pp / 13pp	3.55	12.30	3.55	12.30	---
14sp	50.0	50.4	±5.0	se stripline	13pp / 15pp	3.60	---	3.60	---	---
14sp	100.0	100.1	±10.0	diff stripline	13pp / 15pp	3.60	12.30	3.60	12.30	---
16sp	50.0	49.5	±5.0	se stripline	15pp / 17pp	4.75	---	4.75	---	---
16sp	100.0	99.2	±10.0	diff stripline	15pp / 17pp	4.65	11.40	4.65	11.40	---
16sp	90.0	89.3	±9.0	diff stripline	15pp / 17pp	5.64	10.50	5.64	10.50	---
18sp	50.0	47.8	±5.0	se coated microstrip	17pp / None	6.50	---	6.50	---	---
18sp	100.0	95.5	±10.0	diff coated microstrip	17pp / None	6.00	16.00	6.00	16.00	---
18sp	90.0	85.9	±9.0	diff coated microstrip	17pp / None	7.55	18.00	7.55	18.00	---

Drill Table											
Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Stacked Via	Min Drill Size (mils)	Drill Depth (mils)	Pad Size (mils)	Hole Qty	Do Not Hit Layer	Related Process
1	18	Mechanical	PTH	---	---	0.00	92.1	0.00	0	---	Final Assembly - 1/18
1	18	Mechanical	Via	Non-Conductive Epoxy	---	9.80	92.1	19.00	9158	---	Final Assembly - 1/18
1	2	Laser	Micro Via	Copper Fill	No	6.00	4.0	12.00	190	---	Final Assembly - 1/18
18	17	Laser	Micro Via	Copper Fill	No	6.00	4.0	12.00	56	---	Final Assembly - 1/18
1	13	Backdrill	NPTH	---	---	19.00	63.8	0.00	24	14	Final Assembly - 1/18
18	6	Backdrill	NPTH	---	---	19.00	63.8	0.00	56	5	Final Assembly - 1/18
18	8	Backdrill	NPTH	---	---	19.00	52.8	0.00	10	7	Final Assembly - 1/18



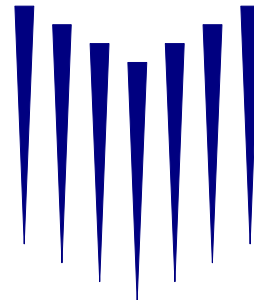
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LX2 SECTION



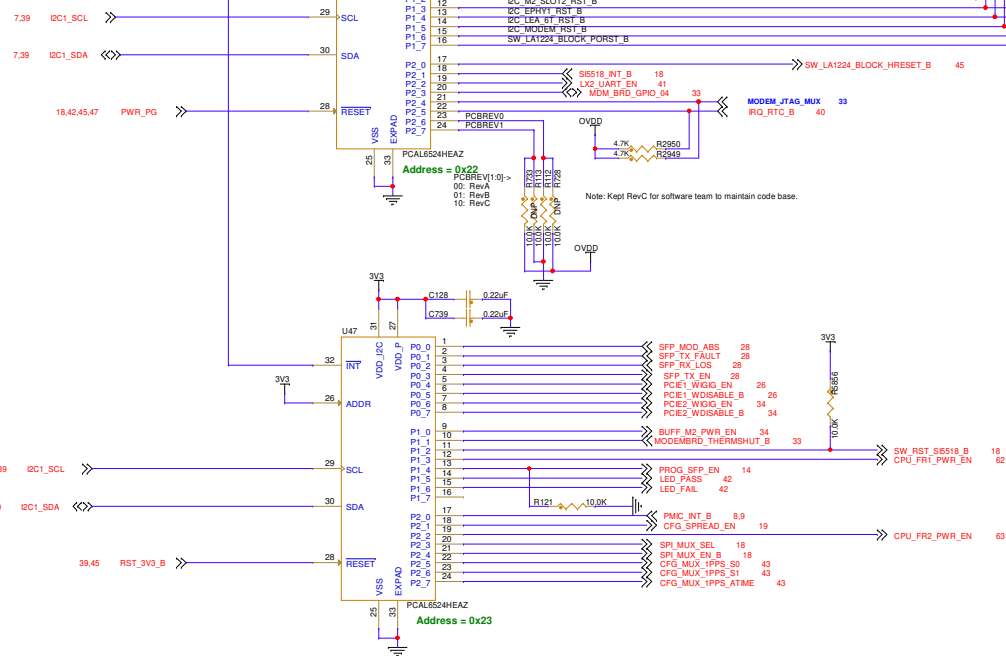
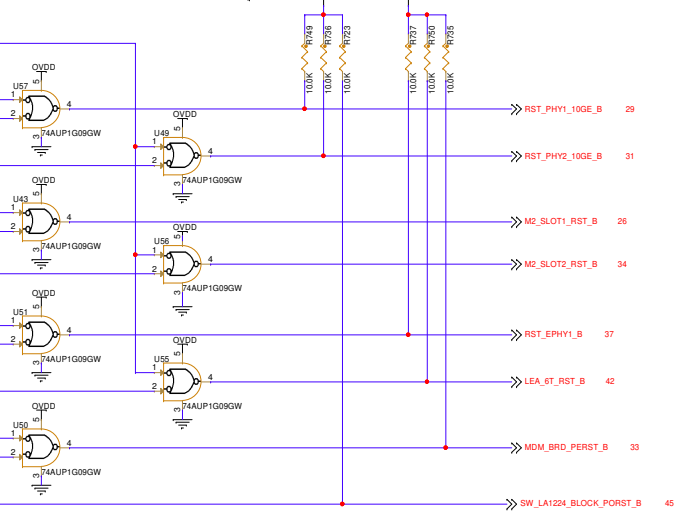
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SW_DP-4SM

SW1[DEFAULT] = SW_DP[8]:1111_0011

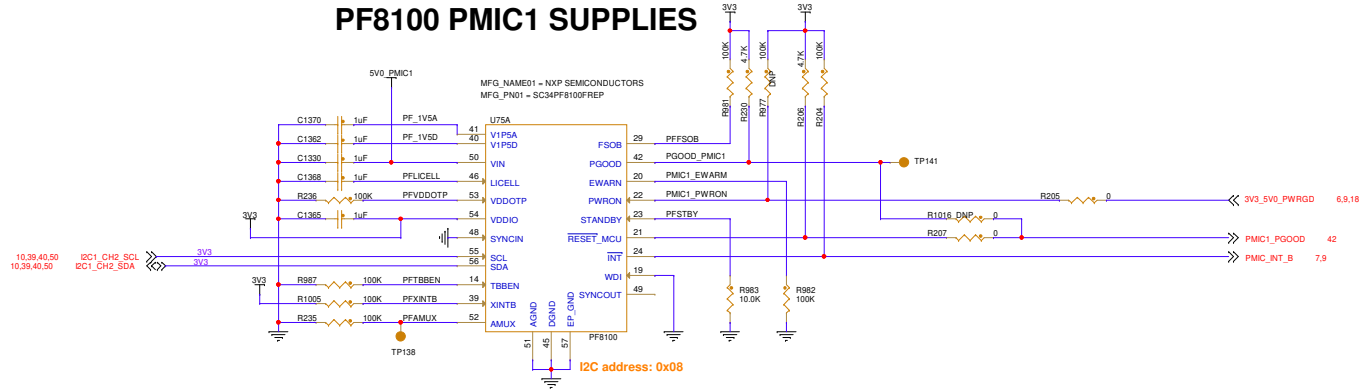
CFG_XSPI_MAP0 20
SD1_CLKF_SEL 19
CFG_MEM_WP 40

```
CFG_XSPI_MAP0
-----
          XSPI_A_CS0  XSPI_A_CS1  DESCRIPTION
>> 0      : DEVW0    DIVW1        Normal
      1      : DEVW1    DIVW0        Swapped
```



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PF8100 PMIC1 SUPPLIES



LX2 POWER SEQUENCING

```
TIER 0
**USB_HVDD
#####
TIER 1
** VDD, OVDD, USB_SVDD,VPP
#####
TIER 3
SD_OVDD,SD_SVDD,AVDD_SdN_PLLn
#####
TIER 4
GVDD, VTT, DDR_VREF,EVDD
#####
```

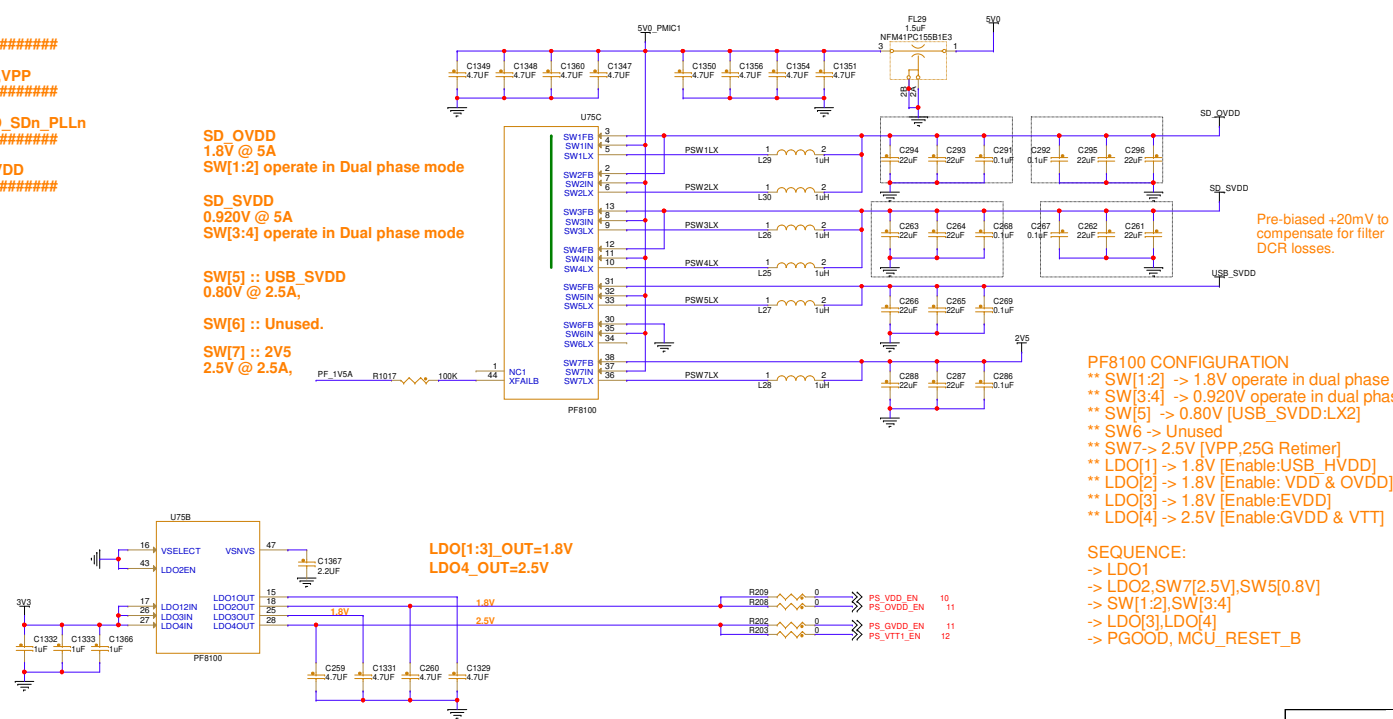
SD_OVDD
1.8V @ 5A
SW[1:2] operate in Dual phase mode

SD_SVDD
0.920V @ 5A
SW[3:4] operate in Dual phase mode

SW[5] :: USB_SVDD
0.80V @ 2.5A,

SW[6] :: Unused.

SW[7] :: 2V5
2.5V @ 2.5A,



PF8100 CONFIGURATION

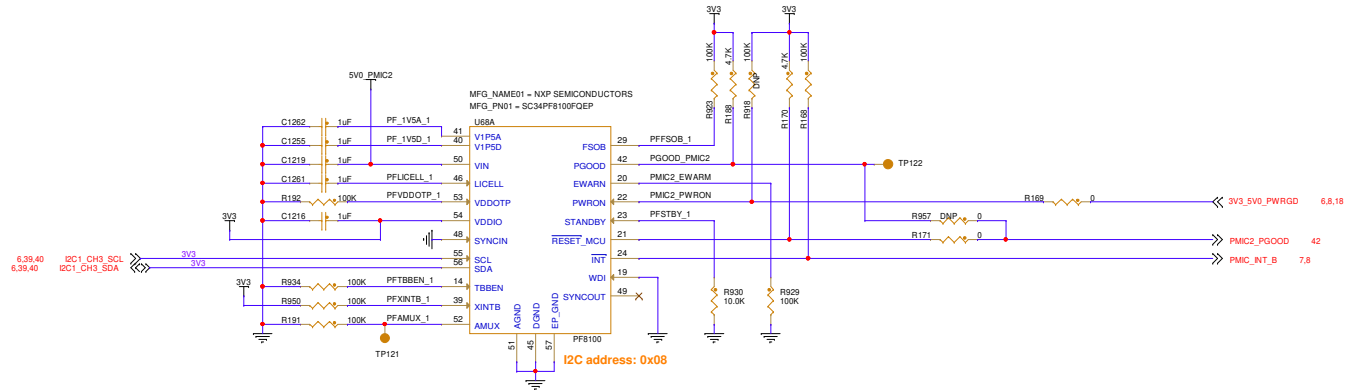
- ```
** SW1[2] -> 1.8V operate in dual phase mode [SD_OVDD:LX2]
** SW1[4] -> 0.920V operate in dual phase mode [SD_SVDD:LX2]
** SW5 -> 0.80V [USB_SVDD:LX2]
** SW6 -> Unused
** SW7 -> 2.5V [VPP_25G Retimer]
** LDO[1] -> 1.8V [Enable:USB_HVDD]
** LDO[2] -> 1.8V [Enable: VDD & OVDD]
** LDO[3] -> 1.8V [Enable:EVDD]
** LDO[4] -> 2.5V [Enable:GVDD & VTT]
```

SEQUENCE:

- > LDO1
- > LDO2, SW7[2.5V], SW5[0.8V]
- > SW[1:2], SW[3:4]
- > LDO[3], LDO[4]
- > PGOOD, MCU\_RESET\_B



# PF8100 PMIC2 SUPPLIES

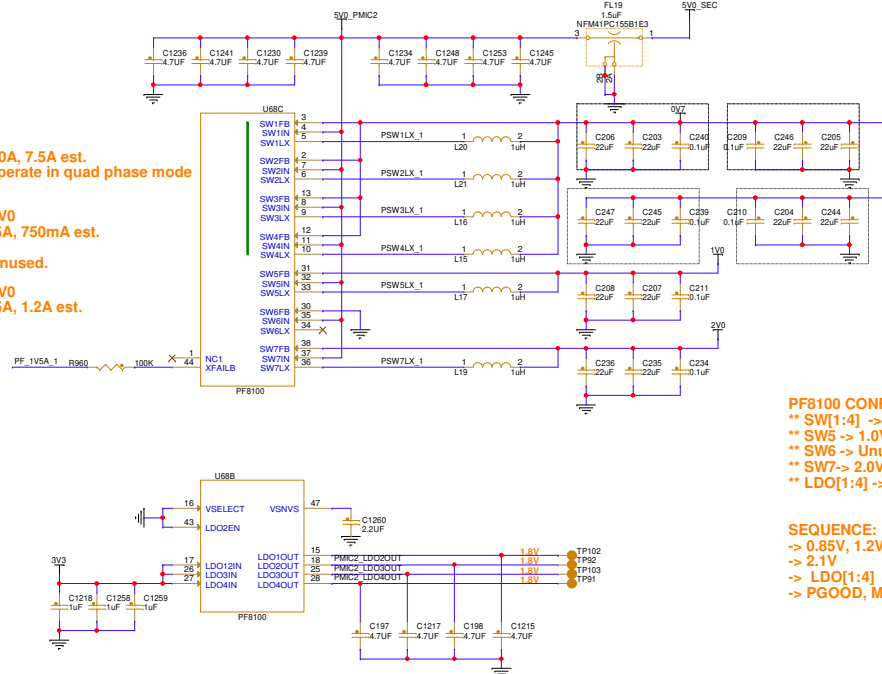


0V7  
0.70V @ 10A, 7.5A est.  
SW[1:4] operate in quad phase mode

SW[5] :: 1V0  
1.0V @ 2.5A, 750mA est.

SW[6] :: Unused.

SW[7] :: 2V0  
2.0V @ 2.5A, 1.2A est.



**PF8100 CONFIGURATION**  
 \*\* SW[1:4] -> 0.70V operate in quad phase mode [ AQR113 PHY]  
 \*\* SW5 -> 1.0V [AQR113 PHY]  
 \*\* SW6 -> Unused  
 \*\* SW7-> 2.0V [AQR113 PHY]  
 \*\* LDO[1:4] -> 1.8V [DONT CARE]

**SEQUENCE:**  
 -> 0.85V, 1.2V,  
 -> 2.1V  
 -> LDO[1:4]  
 -> PGOOD, MCU\_RESET\_B



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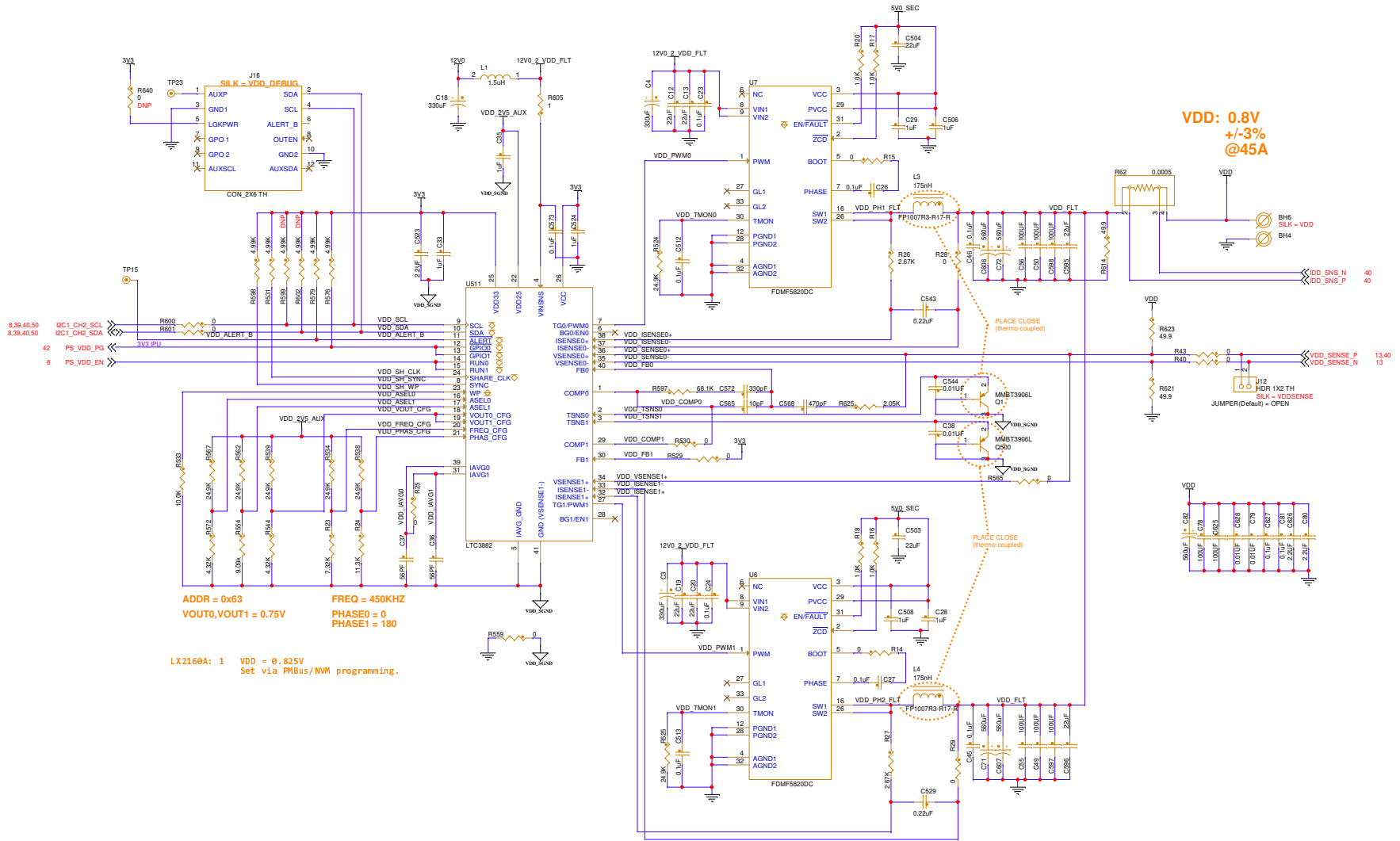
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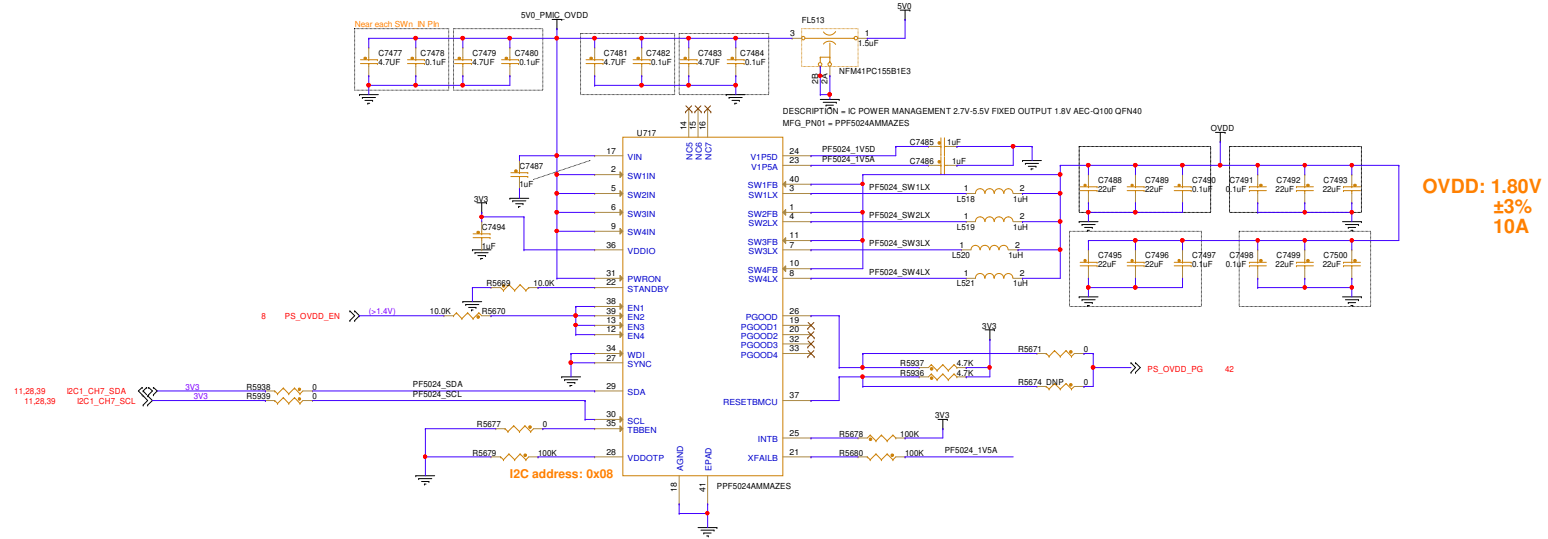
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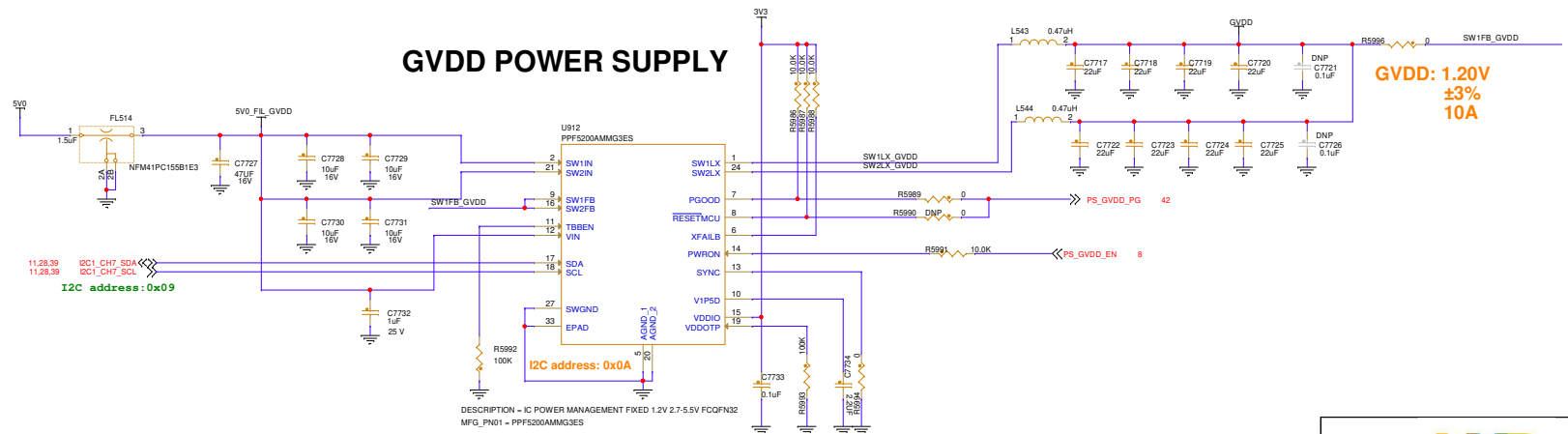
## VDD POWER SUPPLY



## OVDD POWER SUPPLY



## GVDD POWER SUPPLY



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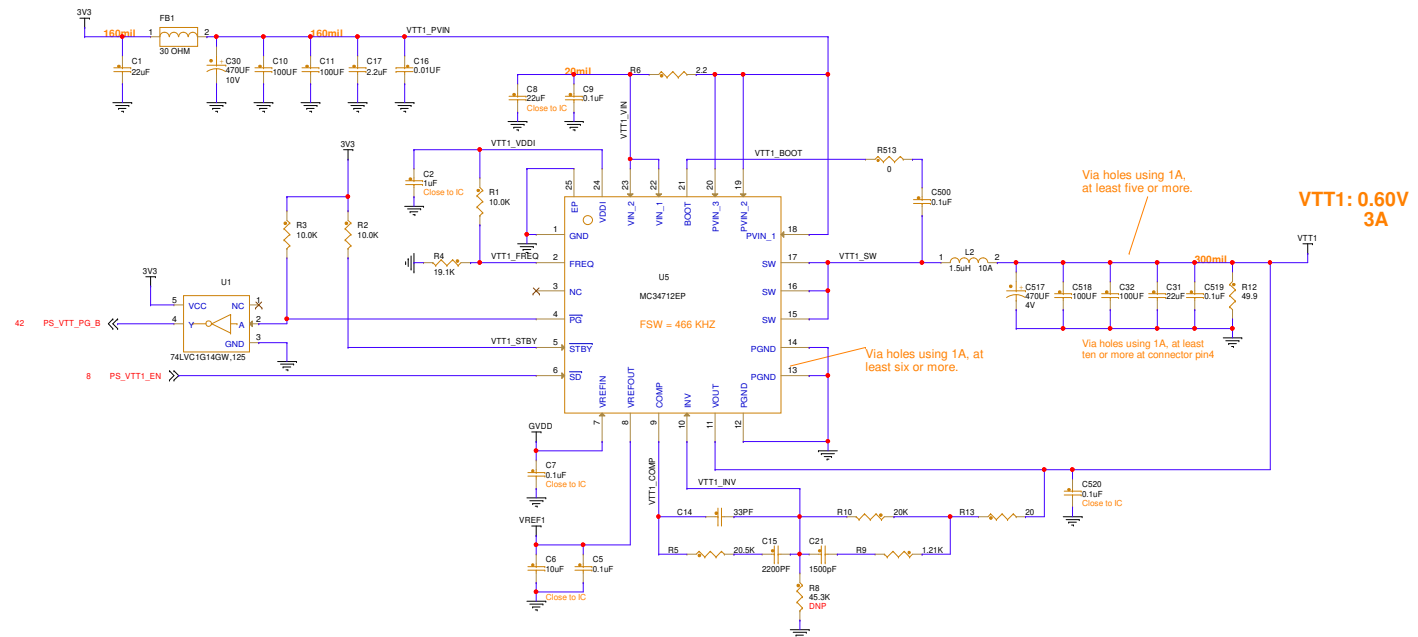
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Page Title: OVDD & GVDD SUPPLIES

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## VTT POWER SUPPLIES



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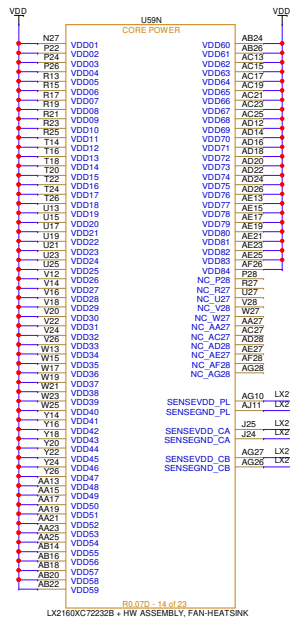
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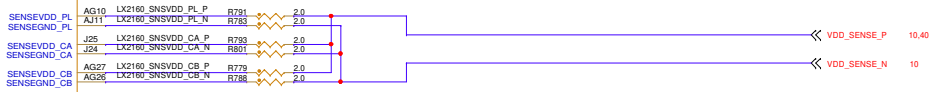
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# LX2160 VDD/CORE POWER



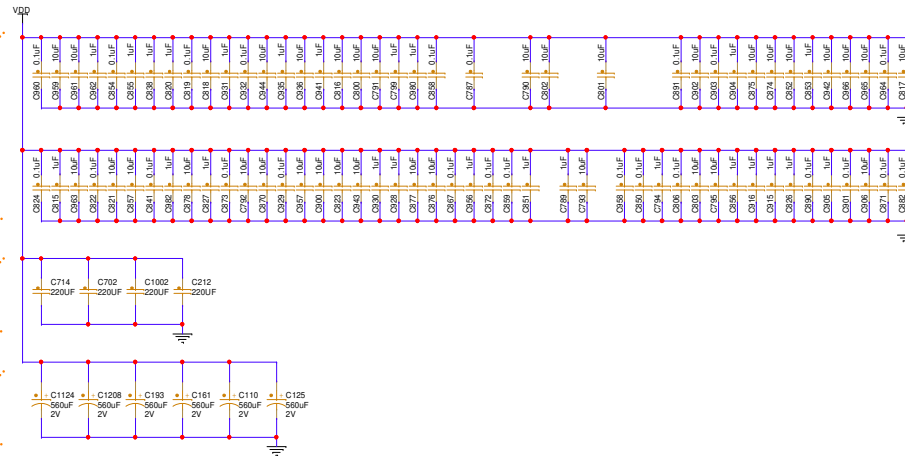
RO 07D - 14 of 23  
LX2160XC7232B + HW ASSEMBLY, FAN-HEATSINK



Place one cap directly on each VDD pin (95 total)

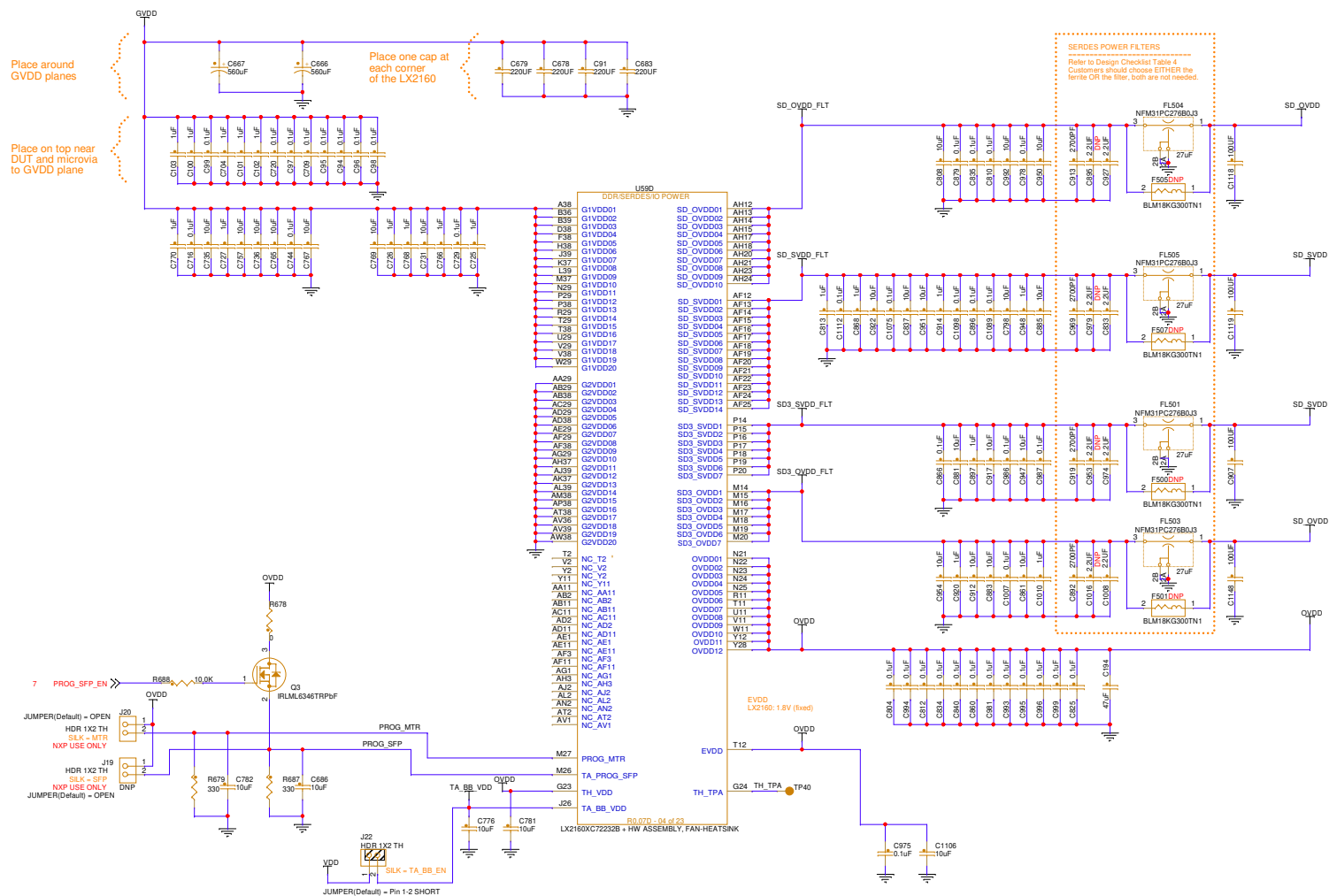
Place one cap at each corner of the LX2160

Place around VDD planes

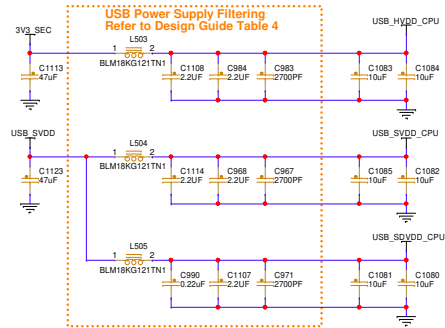
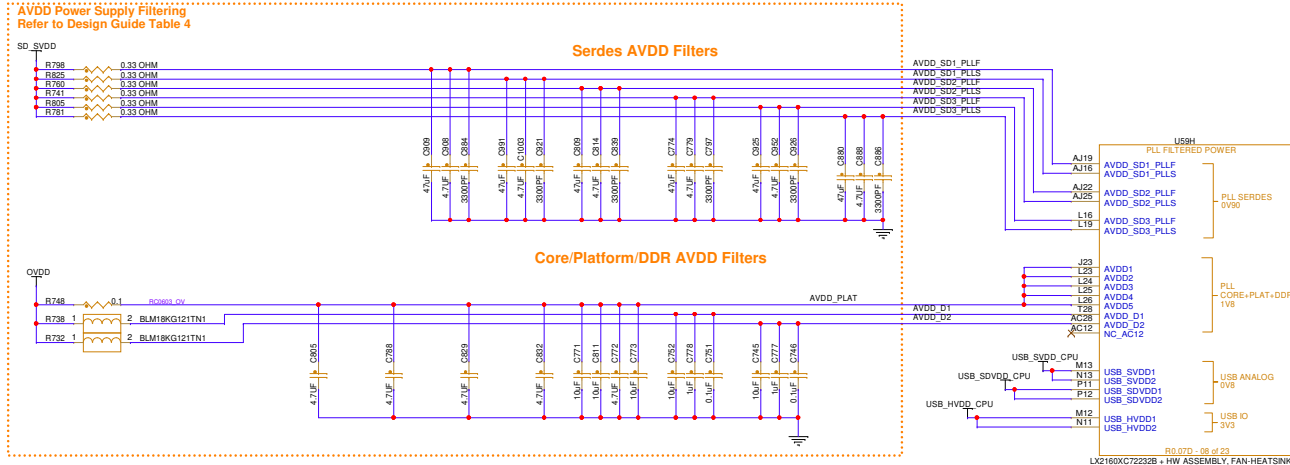


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## LX2160 GVDD, OVDD, SD\_VDD POWER CONNECTIONS



## PLL FILTERED POWER



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Drawing Title:

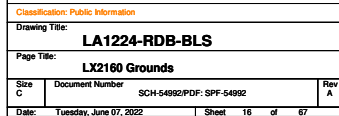
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Page Title: LX2160 PLL Power

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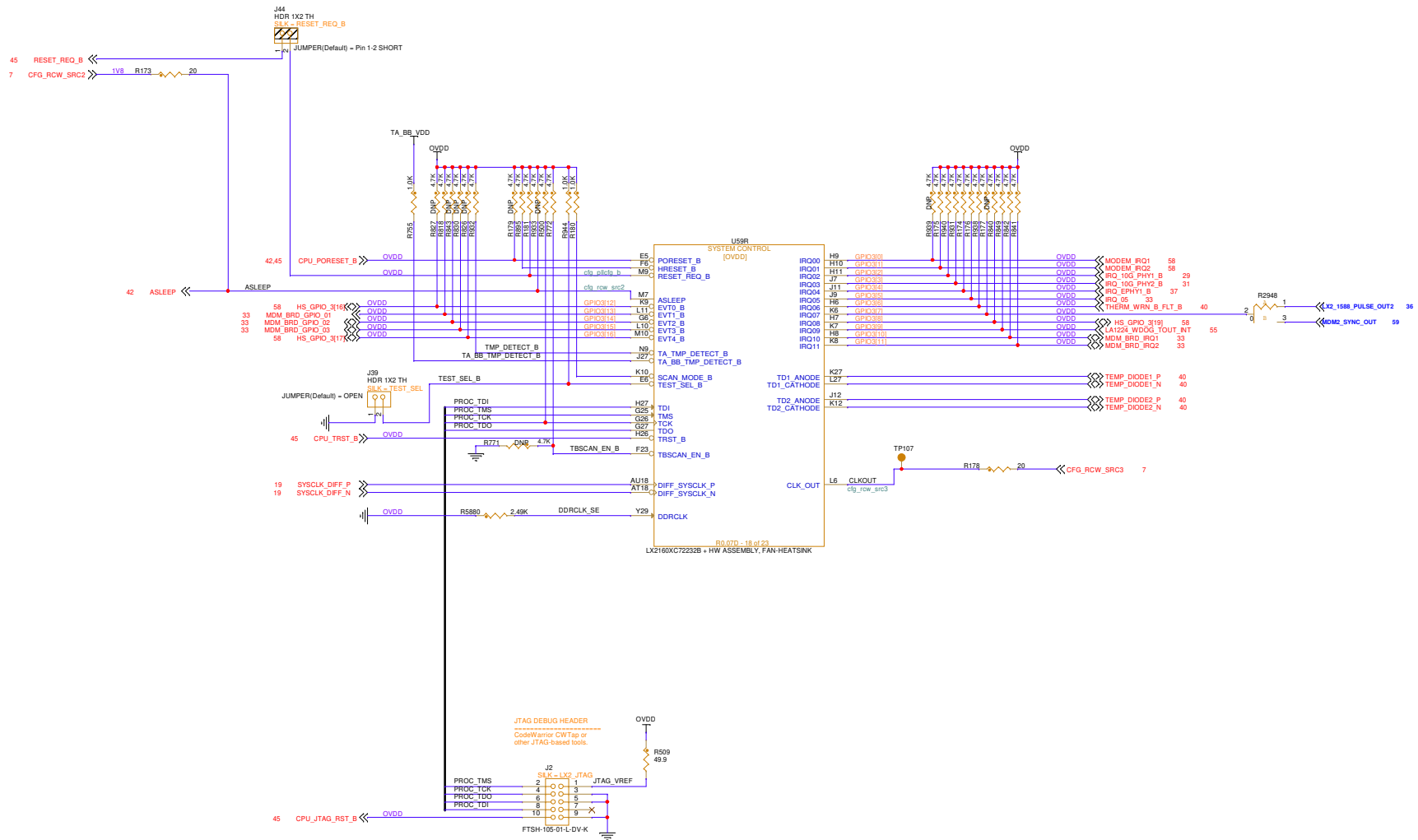
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## LX2160 System Control / JTAG



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## LX2160 System Ctl. & JTAG

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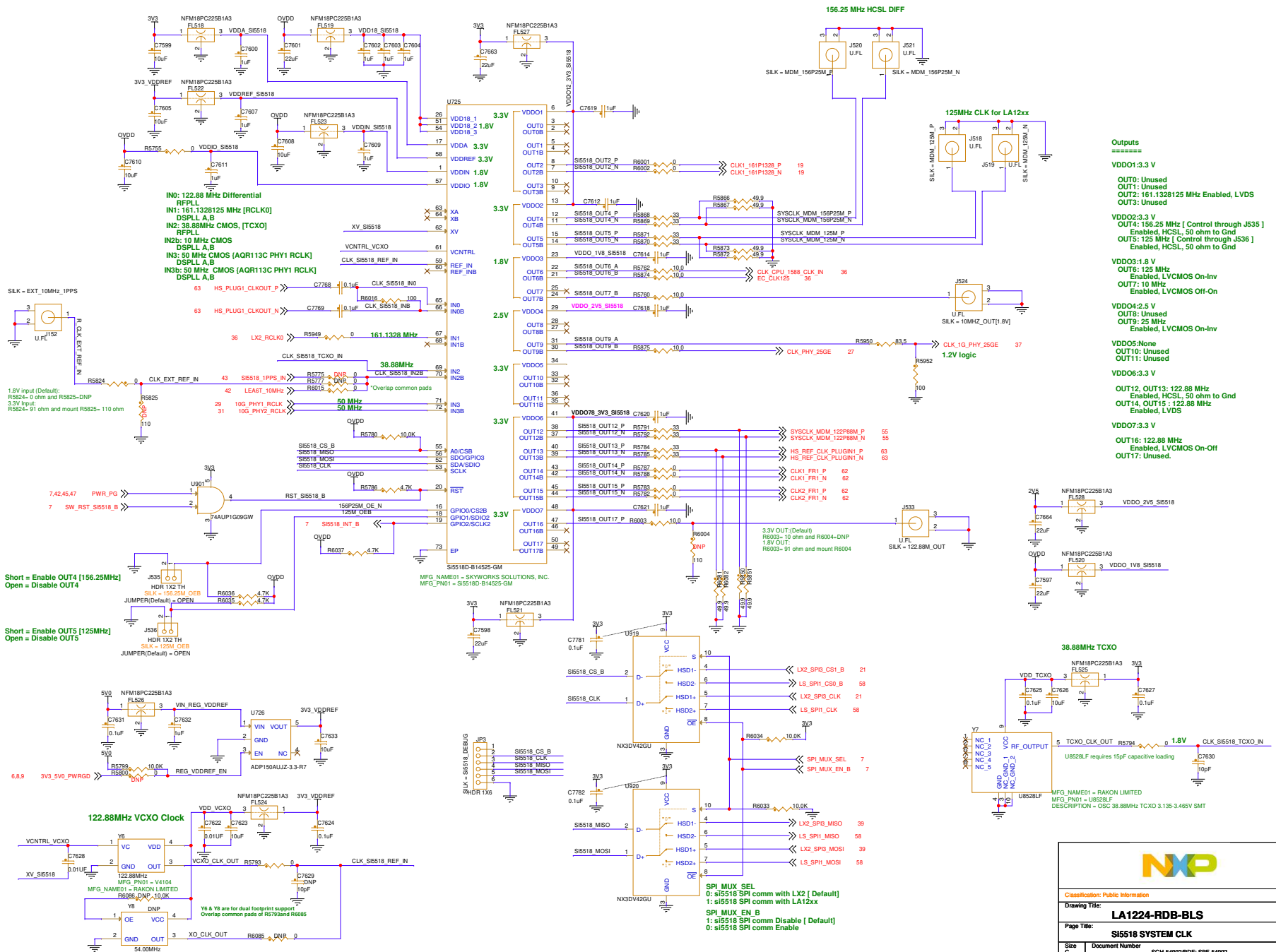
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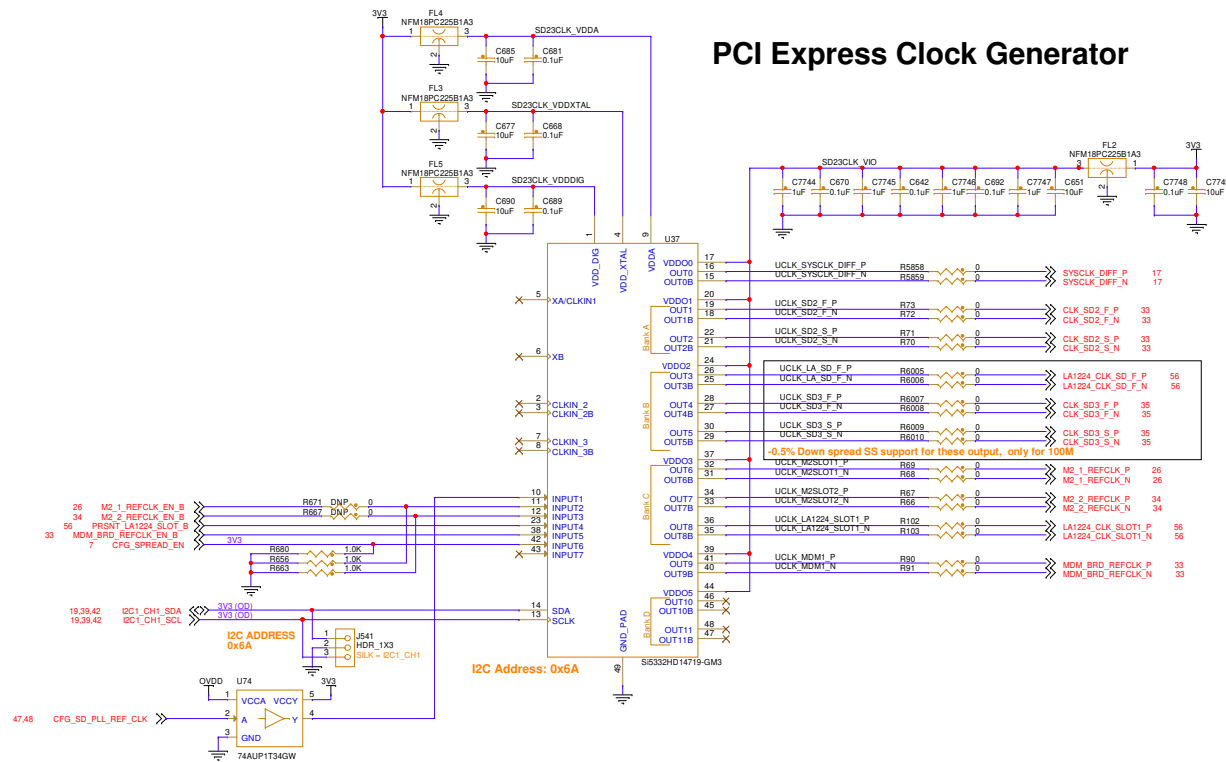
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## Si5518 SYSTEM CLK



|                                                                                                                     |                        |                          |          |
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|                                |                        |                          |          |
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| <b>Page Title:</b><br><div style="text-align: center; font-size: 1.2em; font-weight: bold;">SIS518 SYSTEM CLK</div> |                        |                          |          |
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## PCI Express Clock Generator



Design

Base I2C Address: 0x6A

Universal Hardware Input Pins:

INPUT1 (P10): Frequency Select (Input: LOW = A / HIGH = B)  
 INPUT2 (P11): Output Enable (Input: active LOW)  
 INPUT3 (P12): Output Enable (Input: active LOW)  
 INPUT4 (P23): Output Enable (Input: active LOW)  
 INPUT5 (P38): Output Enable (Input: active LOW)  
 INPUT6 (P42): Spread Spectrum [-0.5% Down spread] (Input: active HIGH)  
 INPUT7 (P43): None

Inputs:

XAXB: 50 MHz Embedded Crystal Mode

CLKIN2: Unused

CLKIN3: Unused

Outputs:

# OUT[0:2]: 100 MHz HCSL 3.3 V 50 Ohms - Internal

# OUT3, OUT4, OUT5:

Profile A: (INPUT1 (P10) = LOW)

125 MHz

Profile B: (INPUT1 (P10) = HIGH)

100 MHz

Format: HCSL 3.3 V 50 Ohms - Internal

#OUT6: 100 MHz HCSL 3.3 V 50 Ohms - Internal,

OEB INPUT2 (P11)

#OUT7: 100 MHz HCSL 3.3 V 50 Ohms - Internal,

OEB INPUT3 (P12)

#OUT8: 100 MHz HCSL 3.3 V 50 Ohms - Internal,

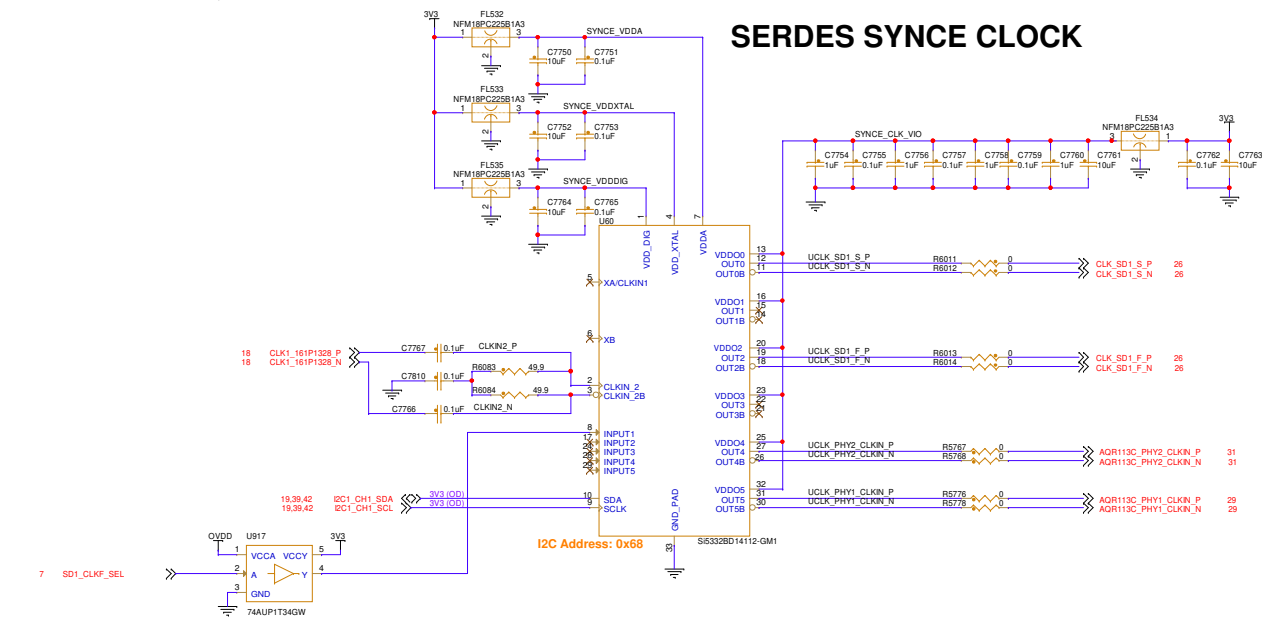
OEB INPUT4 (P23)

#OUT9: 100 MHz HCSL 3.3 V 50 Ohms - Internal,

OEB INPUT5 (P38)

# OUT[10:11]: Unused

## SERDES SYNC CLOCK



Design

Base I2C Address: 0x68

Universal Hardware Input Pins:

INPUT1 (P8): Frequency Select (Input: LOW = A / HIGH = B)  
 INPUT2 (P5): None

Inputs:

XAXB: Unused

CLKIN2: 161.1328125 MHz Differential (LVDS 3.3V)

Outputs:

# OUT0: 161.1328125 MHz HCSL 3.3 V 50 Ohms - Internal,

# OUT1: Unused

# OUT2:

Profile A: (INPUT1 (P8) = LOW)

100 MHz

Format: HCSL 3.3 V 50 Ohms - Internal

# OUT3: Unused

# OUT4: 50 MHz LVDS Fast 3.3 V

# OUT5: 50 MHz LVDS Fast 3.3 V



Classification: Public Information

Drawing Title:

LA1224-RDB-BLS

Page Title:

SYSTEM CLOCK2

Size

Document Number

SC454922PDF: SPF-54992

Rev

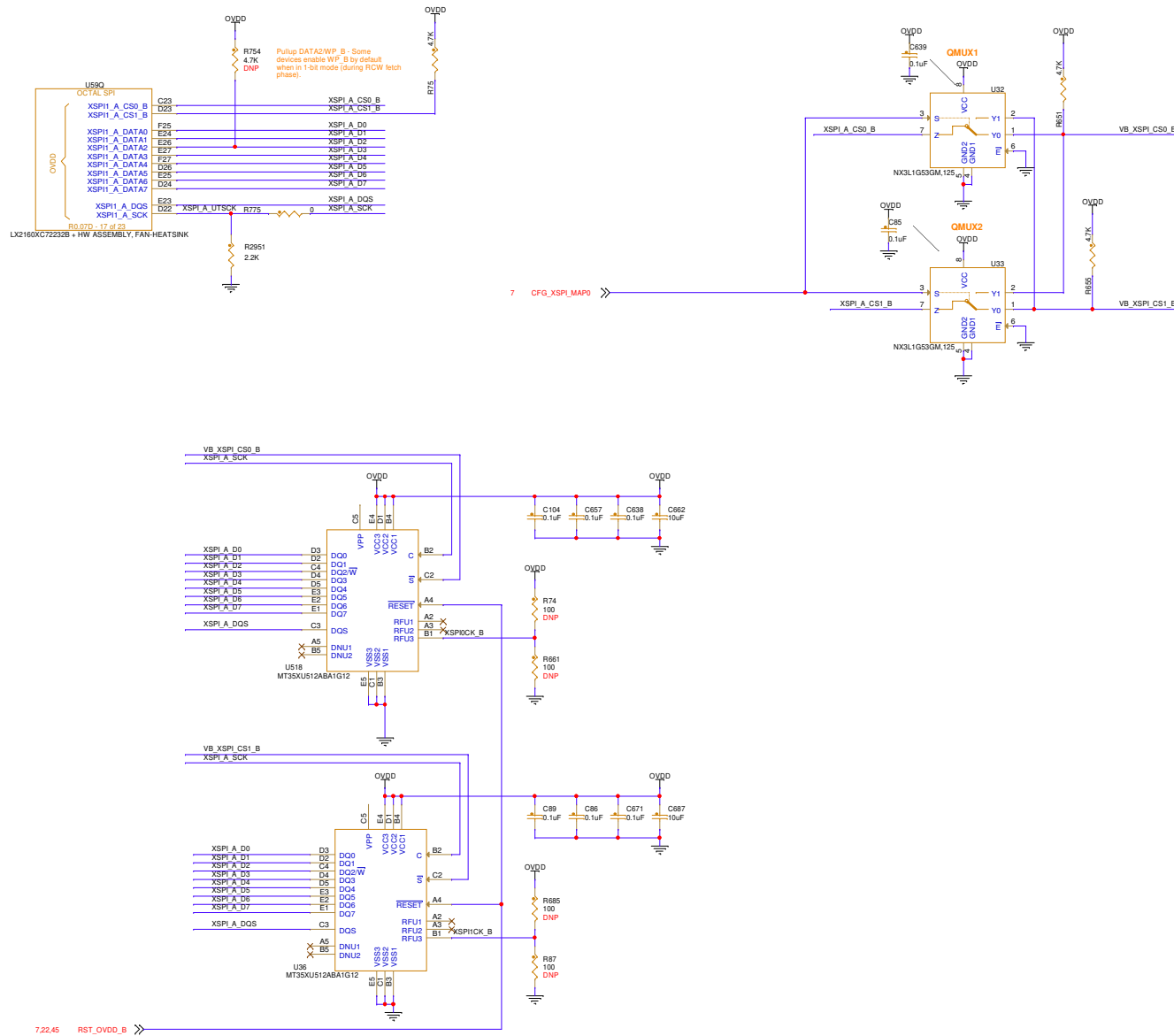
Date:

Tuesday, June 07, 2012

Sheet

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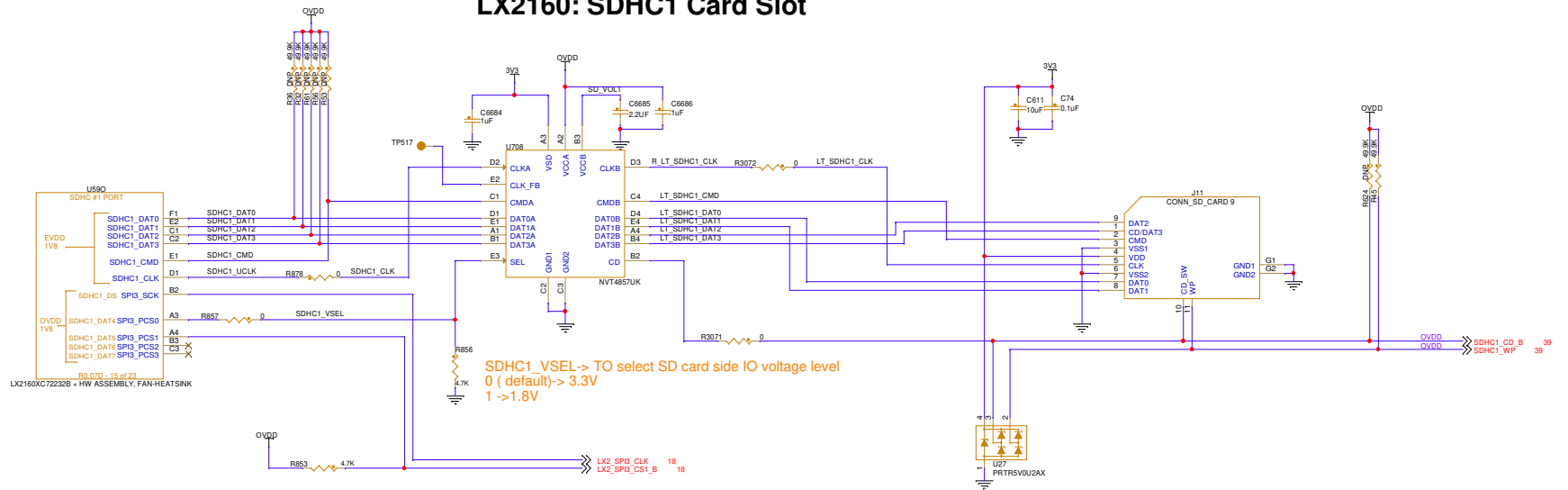
# LX2160 Octal SPI Memory



|                                      |                        |                          |       |
|--------------------------------------|------------------------|--------------------------|-------|
| Classification: Public Information   |                        |                          |       |
| Drawing Title: <b>LA1224-RD8-BLS</b> |                        |                          |       |
| Page Title: <b>LX2160 XSPI</b>       |                        |                          |       |
| Size C                               | Document Number        | SCH-54892/PDF: SPF-54892 | Rev A |
| Date:                                | Tuesday, June 07, 2022 | Sheet 20 of 87           |       |

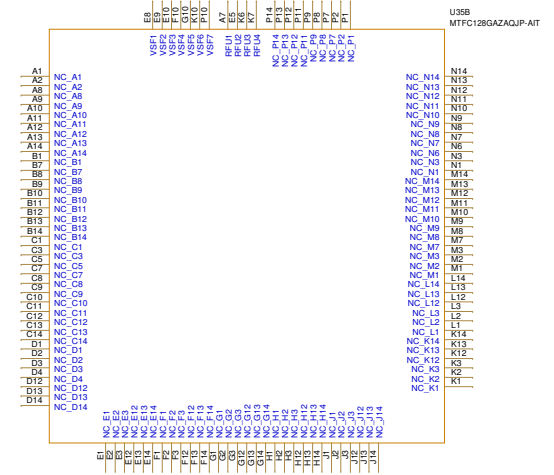
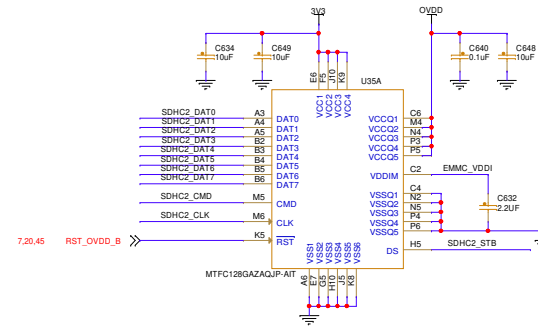


# LX2160: SDHC1 Card Slot

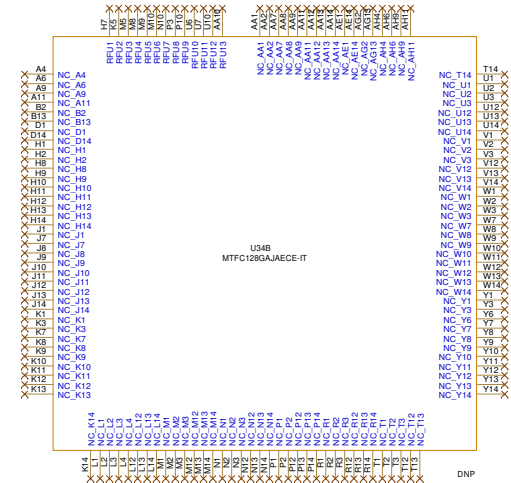
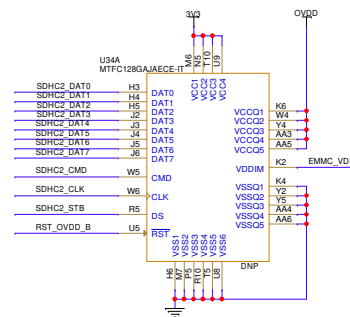


|                                      |                                          |       |  |
|--------------------------------------|------------------------------------------|-------|--|
| Classification: Public Information   |                                          |       |  |
| Drawing Title: LA1224-RD8-BLS        |                                          |       |  |
| Page Title: LX2160 SDHC1 Port & Slot |                                          |       |  |
| Size C                               | Document Number SCH-54892/PDF: SPF-54892 | Rev A |  |
| Date: Tuesday, June 07, 2022         | Sheet 21 of 87                           |       |  |

## eMMC MEMORY



NOTE: U47 and U48 are Overlapped (common) footprints.  
Option 1: Install U35- FBGA153 footprint  
Option 2: Install U34 - FBGA169 footprint  
Only one device is or can be installed.



### ROUTING RULES

1. The 169-pad package (U48) is designed to overlay the 153-pad package (U47). Only one part is ever installed.
2. SDHC2: DAT[7:0]+CMD+CLK+STB: Match <= 1mm
3. SDHC2: DAT[7:0]+CMD must route through pin 2 of the pullup resistors.
4. For bypass capacitors: 0.1uF is nearest the pin, 2.2 or greater is furthest. Both are near the device pin.
5. Since the packages overlap only one set of bypass capacitors are used.
6. 50 ohm impedance (nominal)
6. Series termination for CLK is near the LX2160A DUT.



Classification: Public Information

Drawing Title: **LA1224-RD8-BLS**

Page Title: **LX2160 SDHC2 + eMMC**

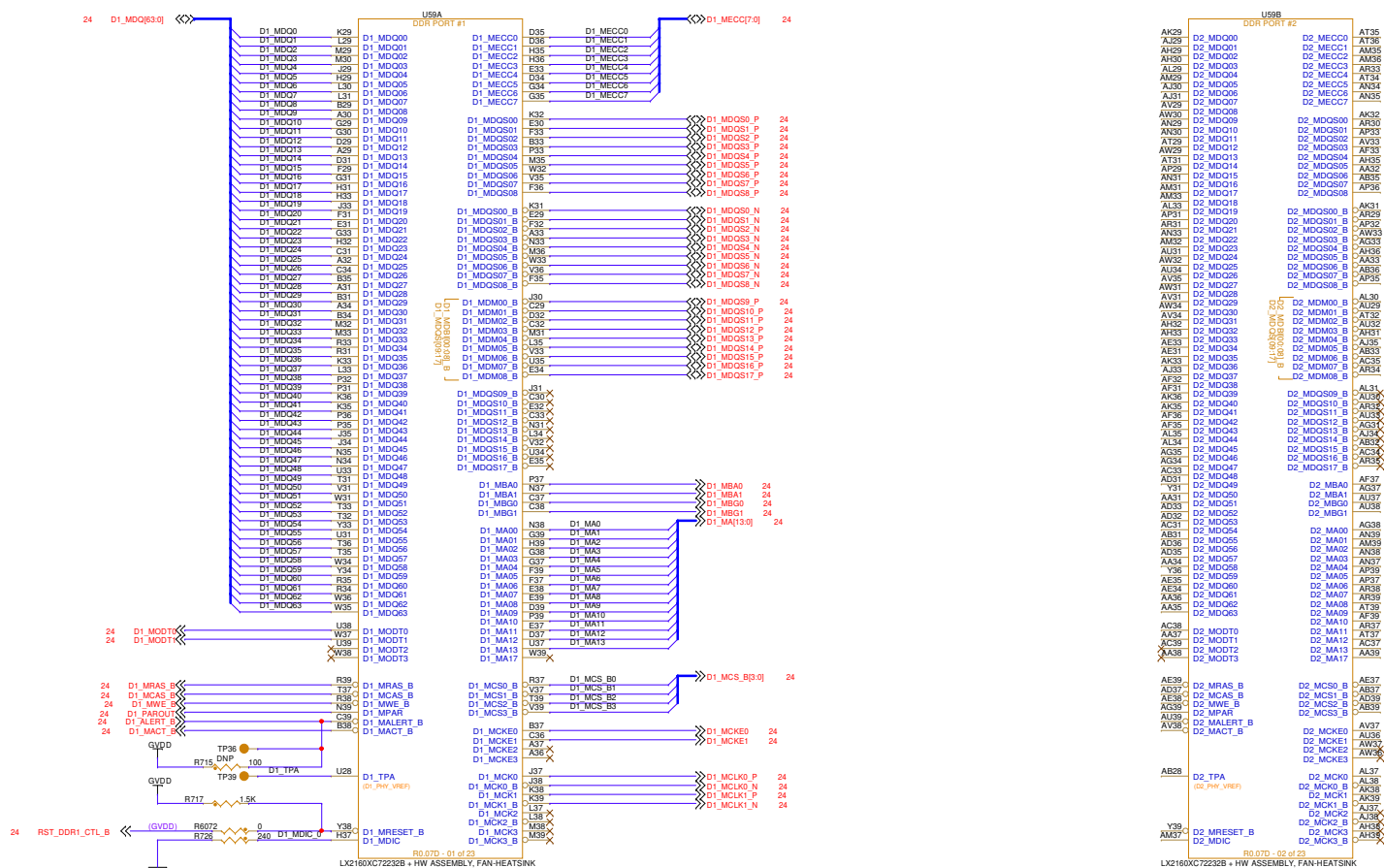
Size: Document Number SCH-54892/PDF: SPF-54892

Date: Tuesday, June 07, 2012

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## DDR4 CONTROLLERS #1 & #2



Added a 0 ohm series resistor to D1\_MRESET\_B signal (RST\_DDR1\_CTL\_B net). This provides the option for managing possible overshoot



Classification: Public Information

Drawing Title: **LA1224-RDB-BLS**

Page Title: LX2160 DDR Ports

|           |                                             |
|-----------|---------------------------------------------|
| Size<br>C | Document Number<br>SCH-54992/PDF: SPF-54992 |
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|       |                           |       |          |
|-------|---------------------------|-------|----------|
| C     | SFF-54992 / Dr. SFF-54992 |       |          |
| Date: | Tuesday, June 07, 2022    | Sheet | 23 of 67 |

[illegible]



Place near CPU RX pins

10G PHY #1  
10G PHY #2  
25G PHY

29 SD1\_10G\_RX0\_P  
29 AGR113  
31 SD1\_10G\_RX1\_P  
31 SD1\_10G\_RX1\_N  
27 SD1\_25G\_RX2\_P  
27 SD1\_25G\_RX2\_N

PCIE Core  
[For LC1224 Modem card]

SD1\_RX4\_P  
SD1\_RX4\_N  
SD1\_RX5\_N

SD1\_RX0\_P  
SD1\_RX0\_N  
SD1\_RX1\_P  
SD1\_RX1\_N  
SD1\_RX2\_P  
SD1\_RX2\_N  
SD1\_RX3\_P  
SD1\_RX3\_N  
SD1\_RX4\_P  
SD1\_RX4\_N  
SD1\_RX5\_P  
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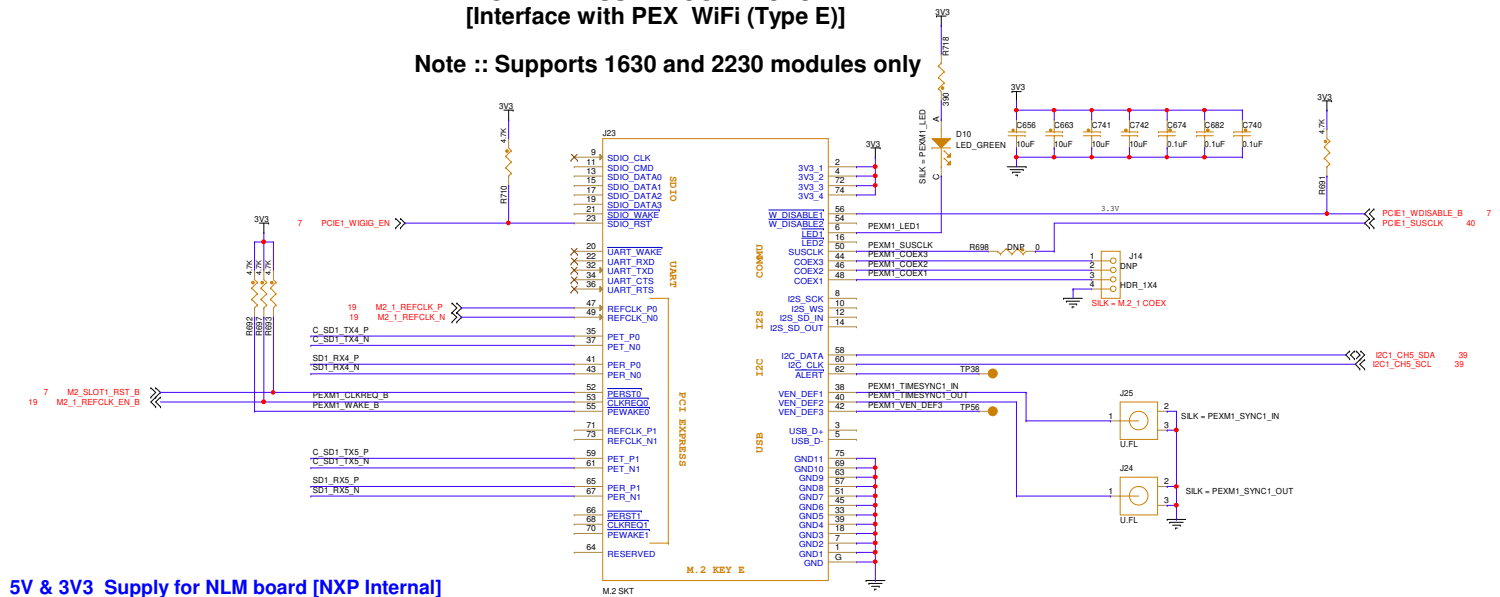
```

LX2160: # 22 - USXGMII.3 + USXGMII.4 + XXXXXX + XXXXXX + PCIe.2 x2 + XXXXXX + XXXXXX PLL Mapping
PLL Mapping + S555 + FF55
CLOCK-) SD1_PLLS_REF_CLK: 161.1328125 MHz + SD1_PLLF_REF_CLK: 100.00 MHz

LX2160: # 18 - USXGMII.3 + USXGMII.4 + 25G.E.5 + 25G.E.6 + XXXXXX + XXXXXX + XXXXXX + XXXXXX
PLL Mapping + SFFF + S555
CLOCK-) SD1_PLLS_REF_CLK: 161.1328125 MHz + SD1_PLLF_REF_CLK: 161.1328125 MHz

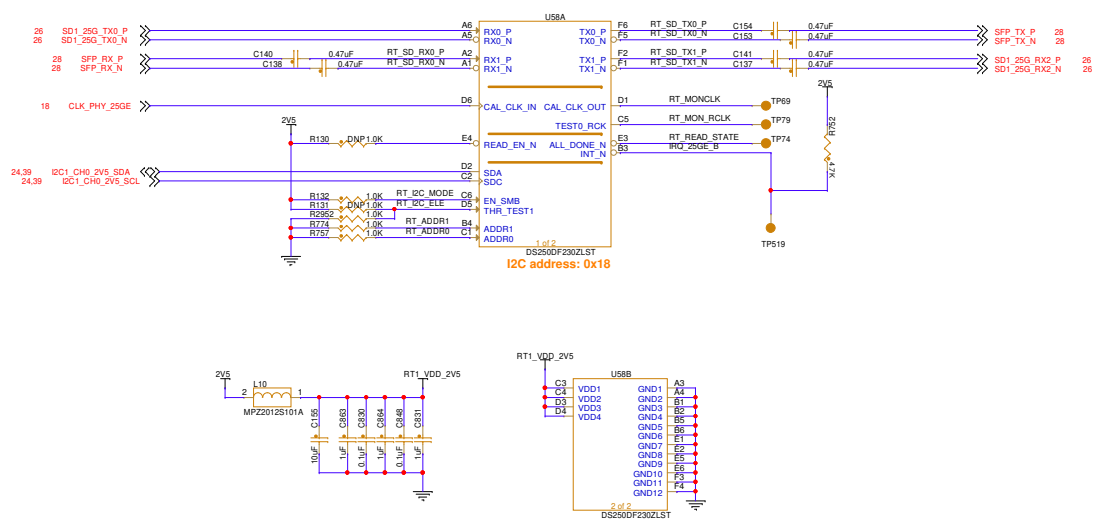
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**Note :: Supports 1630 and 2230 modules only**



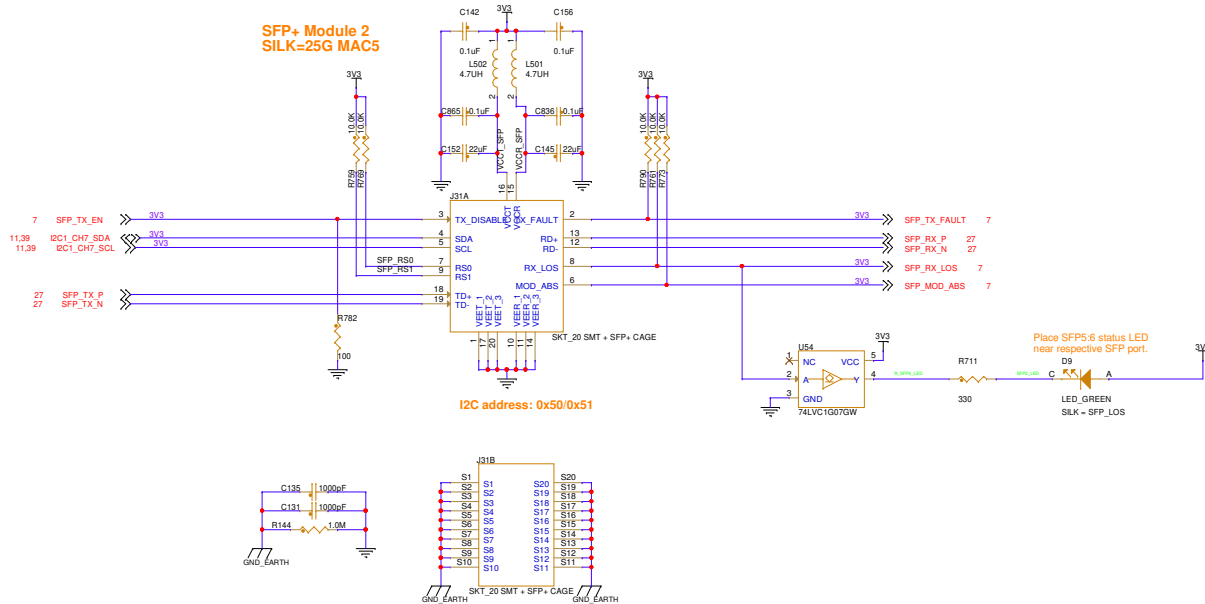
Two circuit diagrams illustrating the connection of the NLM5V0\_PWR pin. The left diagram shows a 5V0 supply connected to the pin through a 10uF capacitor (C7783) and a 0.1uF capacitor (C7784). The right diagram shows a 3V3 supply connected to the pin through a 10uF capacitor (C7781). Both diagrams show the pin connected to ground.

# 25GE Retimer Ethernet Interface



|                                     |                        |                          |       |
|-------------------------------------|------------------------|--------------------------|-------|
| Classification: Public Information  |                        |                          |       |
| Drawing Title: LA1224-RDB-BLS       |                        |                          |       |
| Page Title: DS250DF230 25GE Retimer |                        |                          |       |
| Size C                              | Document Number        | SCH-54892/PDF: SPF-54892 | Rev A |
| Date:                               | Tuesday, June 07, 2022 | Sheet 27 of 87           |       |

## 25GE SFP+ Interfaces



**Classification: Public Information**

Drawing Title: **LA1224-RDB-BLS**

|             |                             |
|-------------|-----------------------------|
| Page Title: | <b>DS250DF230 25GE SFP+</b> |
|-------------|-----------------------------|

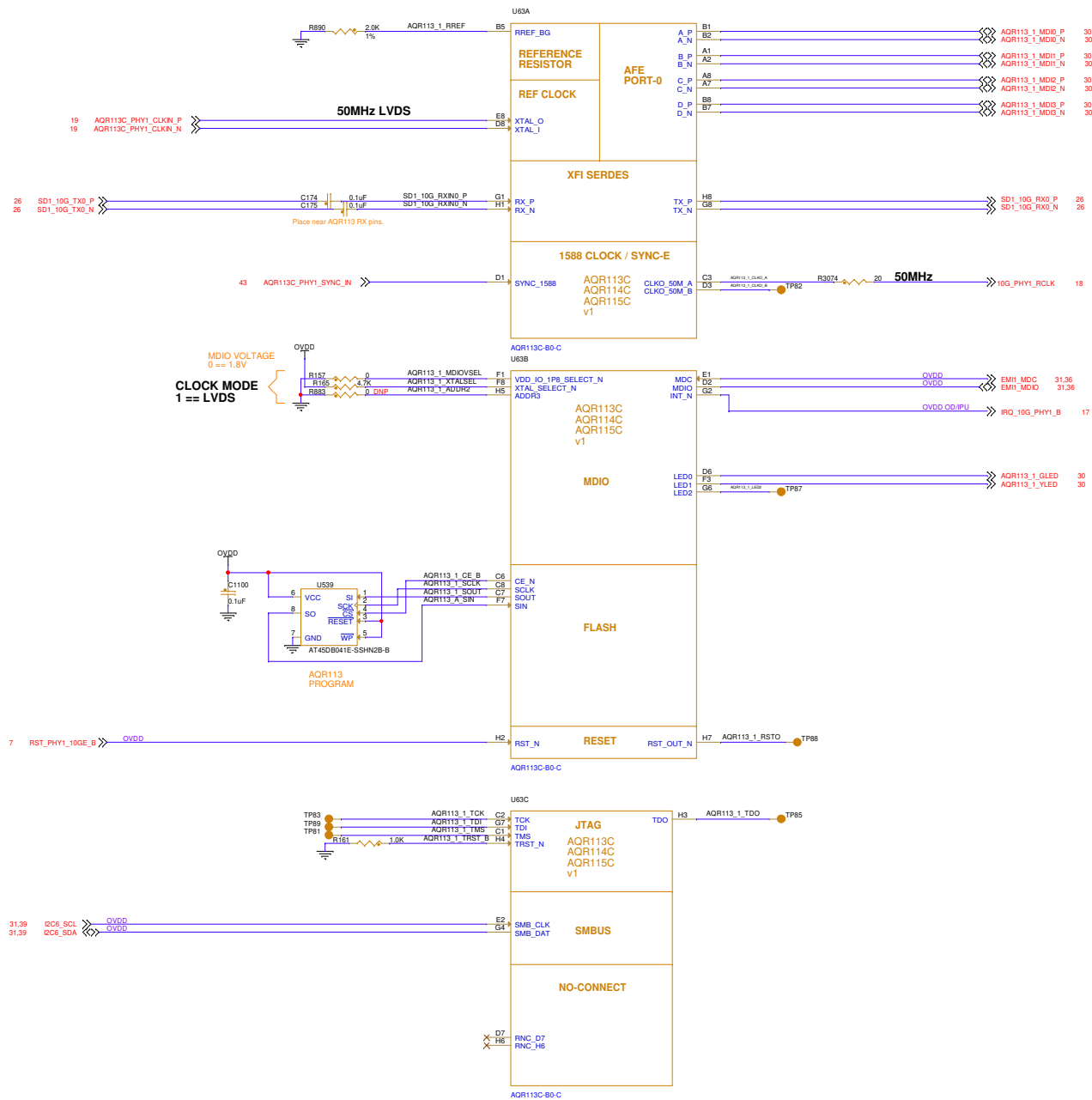
|           |                                             |
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| Size<br>C | Document Number<br>SCH-54992/PDF: SPF-54992 |
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|       |                        |       |    |    |    |
|-------|------------------------|-------|----|----|----|
| Date: | Tuesday, June 07, 2022 | Sheet | 28 | of | 67 |
|-------|------------------------|-------|----|----|----|

Rev  
A

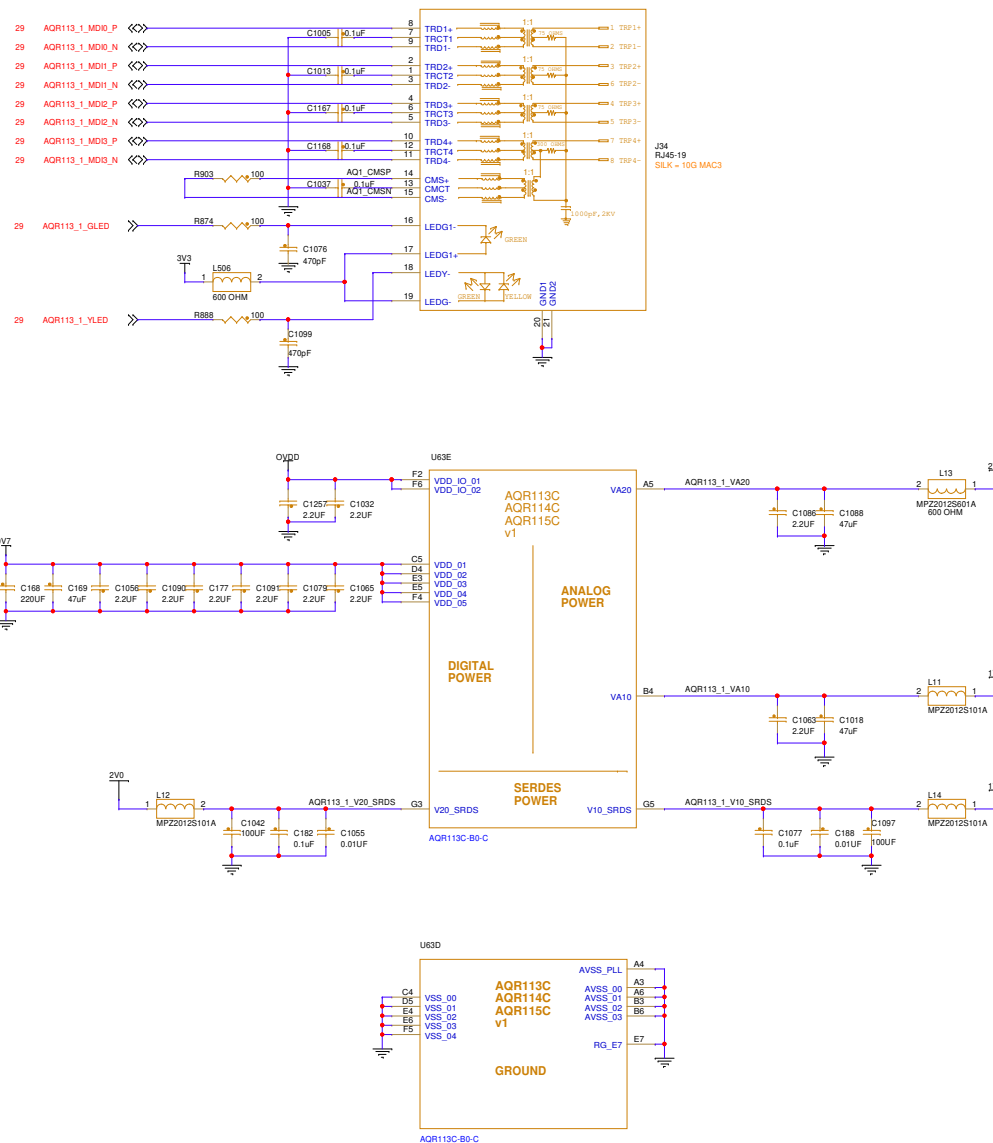


# AQR113 #1 10GE USXGMII Ethernet: Control



|                                              |                        |                         |       |
|----------------------------------------------|------------------------|-------------------------|-------|
| Classification: Public Information           |                        |                         |       |
| Drawing Title: <b>LA1224-RDB-BLS</b>         |                        |                         |       |
| Page Title: <b>AQR113 #1 10G PHY Control</b> |                        |                         |       |
| Size C                                       | Document Number        | SCH-54992/PDF-SPF-54992 | Rev A |
| Date:                                        | Tuesday, June 07, 2012 | Sheet 29 of 87          |       |

# AQR113 #1 Power & Connector



|                                     |                        |                          |       |
|-------------------------------------|------------------------|--------------------------|-------|
| Classification: Public Information  |                        |                          |       |
| Drawing Title: LA1224-RDB-BLS       |                        |                          |       |
| Page Title: AQR113 #1 10G PHY Power |                        |                          |       |
| Size C                              | Document Number        | SCH-54892/PDF: SPF-54892 | Rev A |
| Date:                               | Tuesday, June 07, 2022 | Sheet 30 of 87           |       |

**AQR113 #2 10GE USXGMII Ethernet: Control**

**U71A**

**REFERENCE RESISTOR**

**REF CLOCK**

**XTAL\_O**

**XTAL\_I**

**50MHz LVDS**

**50MHz**

**1588 CLOCK / SYNC-E**

**MDIO**

**FLASH**

**RESET**

**JTAG**

**SMBUS**

**NO-CONNECT**

**AQR113C-80-C**

**U71B**

**U71C**

**LA1224-RDB-BLS**

**AQR113 #2 10G PHY Control**

**Size C**

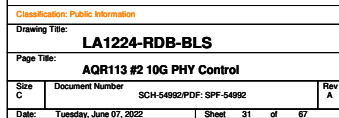
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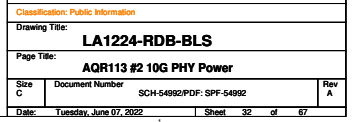
**SCH-54992/PDF: SPF-54992**

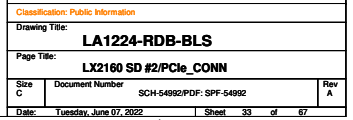
**Date: Tuesday, June 07, 2022**

**Sheet 31 of 67**

**Rev A**





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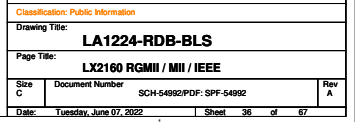
**Note :: Supports 1630 and 2230 modules only**





The schematic diagram illustrates the electrical connections for the LX2160XC72232B HW Assembly, Fan-Heatsink. It features several key components and signal paths:

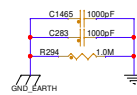
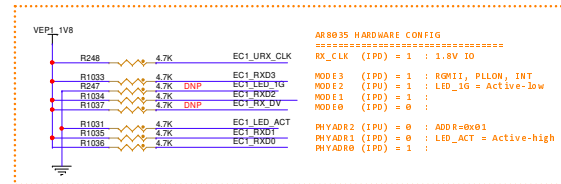
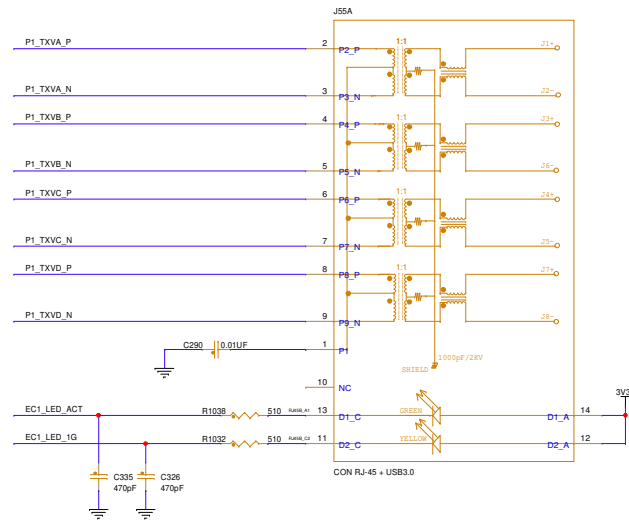
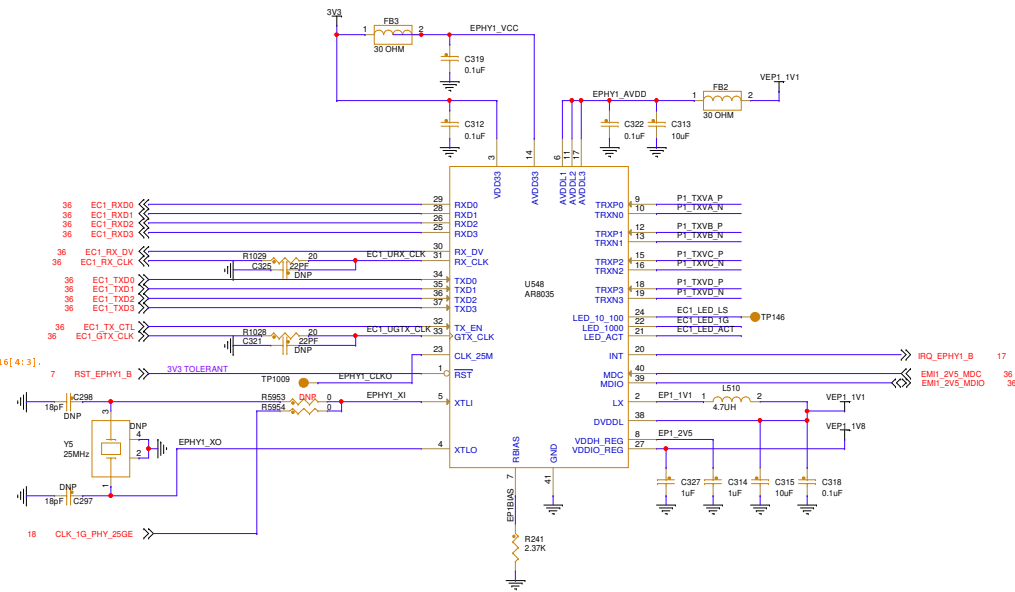
- U595 (RGMI PORTS [OVDD]):** A central component with multiple pins (J1, J2, F3, G1, N2, N1, M1, L2, K3, L1, P3, N6, N8) connected to various signal and power lines.
- U59W (EMI PORTS):** A component with pins R2, R1, R4, R3 connected to EMI1\_MDC, EMI1\_MDIO, EMI2\_MDC, and EMI2\_MDIO.
- NTSX2102GUH:** A component with pins A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60, A61, A62, A63, A64, A65, A66, A67, A68, A69, A70, A71, A72, A73, A74, A75, A76, A77, A78, A79, A80, A81, A82, A83, A84, A85, A86, A87, A88, A89, A90, A91, A92, A93, A94, A95, A96, A97, A98, A99, A100, A101, A102, A103, A104, A105, A106, A107, A108, A109, A110, A111, A112, A113, A114, A115, A116, A117, A118, A119, A120, A121, A122, A123, A124, A125, A126, A127, A128, A129, A130, A131, A132, A133, A134, A135, A136, A137, A138, A139, A140, A141, A142, A143, A144, A145, A146, A147, A148, A149, A150, A151, A152, A153, A154, A155, A156, A157, A158, A159, A160, A161, A162, A163, A164, A165, A166, A167, A168, A169, A170, A171, A172, A173, A174, A175, A176, A177, A178, A179, A180, A181, A182, A183, A184, A185, A186, A187, A188, A189, A190, A191, A192, A193, A194, A195, A196, A197, A198, A199, A200, A201, A202, A203, A204, A205, A206, A207, A208, A209, A210, A211, A212, A213, A214, A215, A216, A217, A218, A219, A220, A221, A222, A223, A224, A225, A226, A227, A228, A229, A230, A231, A232, A233, A234, A235, A236, A237, A238, A239, A240, A241, A242, A243, A244, A245, A246, A247, A248, A249, A250, A251, A252, A253, A254, A255, A256, A257, A258, A259, A260, A261, A262, A263, A264, A265, A266, A267, A268, A269, A270, A271, A272, A273, A274, A275, A276, A277, A278, A279, A280, A281, A282, A283, A284, A285, A286, A287, A288, A289, A290, A291, A292, A293, A294, A295, A296, A297, A298, A299, A300, A301, A302, A303, A304, A305, A306, A307, A308, A309, A310, A311, A312, A313, A314, A315, A316, A317, A318, A319, A320, A321, A322, A323, A324, A325, A326, A327, A328, A329, A330, A331, A332, A333, A334, A335, A336, A337, A338, A339, A340, A341, A342, A343, A344, A345, A346, A347, A348, A349, A350, A351, A352, A353, A354, A355, A356, A357, A358, A359, A360, A361, A362, A363, A364, A365, A366, A367, A368, A369, A370, A371, A372, A373, A374, A375, A376, A377, A378, A379, A380, A381, A382, A383, A384, A385, A386, A387, A388, A389, A390, A391, A392, A393, A394, A395, A396, A397, A398, A399, A400, A401, A402, A403, A404, A405, A406, A407, A408, A409, A410, A411, A412, A413, A414, A415, A416, A417, A418, A419, A420, A421, A422, A423, A424, A425, A426, A427, A428, A429, A430, A431, A432, A433, A434, A435, A436, A437, A438, A439, A440, A441, A442, A443, A444, A445, A446, A447, A448, A449, A450, A451, A452, A453, A454, A455, A456, A457, A458, A459, A460, A461, A462, A463, A464, A465, A466, A467, A468, A469, A470, A471, A472, A473, A474, A475, A476, A477, A478, A479, A480, A481, A482, A483, A484, A485, A486, A487, A488, A489, A490, A491, A492, A493, A494, A495, A496, A497, A498, A499, A500, A501, A502, A503, A504, A505, A506, A507, A508, A509, A510, A511, A512, A513, A514, A515, A516, A517, A518, A519, A520, A521, A522, A523, A524, A525, A526, A527, A528, A529, A530, A531, A532, A533, A534, A535, A536, A537, A538, A539, A540, A541, A542, A543, A544, A545, A546, A547, A548, A549, A550, A551, A552, A553, A554, A555, A556, A557, A558, A559, A560, A561, A562, A563, A564, A565, A566, A567, A568, A569, A570, A571, A572, A573, A574, A575, A576, A577, A578, A579, A580, A581, A582, A583, A584, A585, A586, A587, A588, A589, A590, A591, A592, A593, A594, A595, A596, A597, A598, A599, A600, A601, A602, A603, A604, A605, A606, A607, A608, A609, A610, A611, A612, A613, A614, A615, A616, A617, A618, A619, A620, A621, A622, A623, A624, A625, A626, A627, A628, A629, A630, A631, A632, A633, A634, A635, A636, A637, A638, A639, A640, A641, A642, A643, A644, A645, A646, A647, A648, A649, A650, A651, A652, A653, A654, A655, A656, A657, A658, A659, A660, A661, A662, A663, A664, A665, A666, A667, A668, A669, A670, A671, A672, A673, A674, A675, A676, A677, A678, A679, A680, A681, A682, A683, A684, A685, A686, A687, A688, A689, A690, A691, A692, A693, A694, A695, A696, A697, A698, A699, A700, A701, A702, A703, A704, A705, A706, A707, A708, A709, A710, A711, A712, A713, A714, A715, A716, A717, A718, A719, A720, A721, A722, A723, A724, A725, A726, A727, A728, A729, A730, A731, A732, A733, A734, A735, A736, A737, A738, A739, A740, A741, A742, A743, A744, A745, A746, A747, A748, A749, A750, A751, A752, A753, A754, A755, A756, A757, A758, A759, A





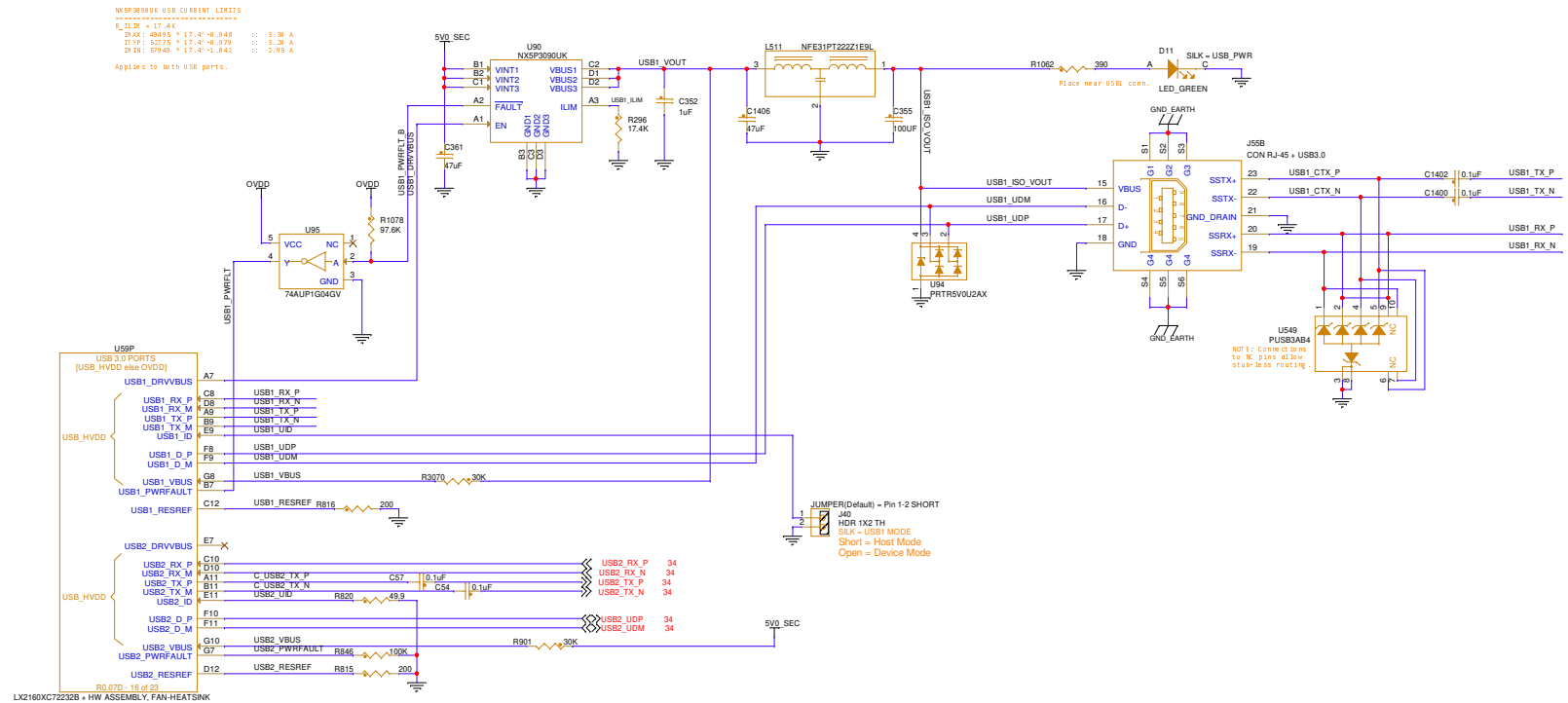
# 1G RGMII Ethernet #1

NOTE: CLK\_25M default outputs 25MHz,  
Please config it to can 125MHz by register MM07 0016[4:3].

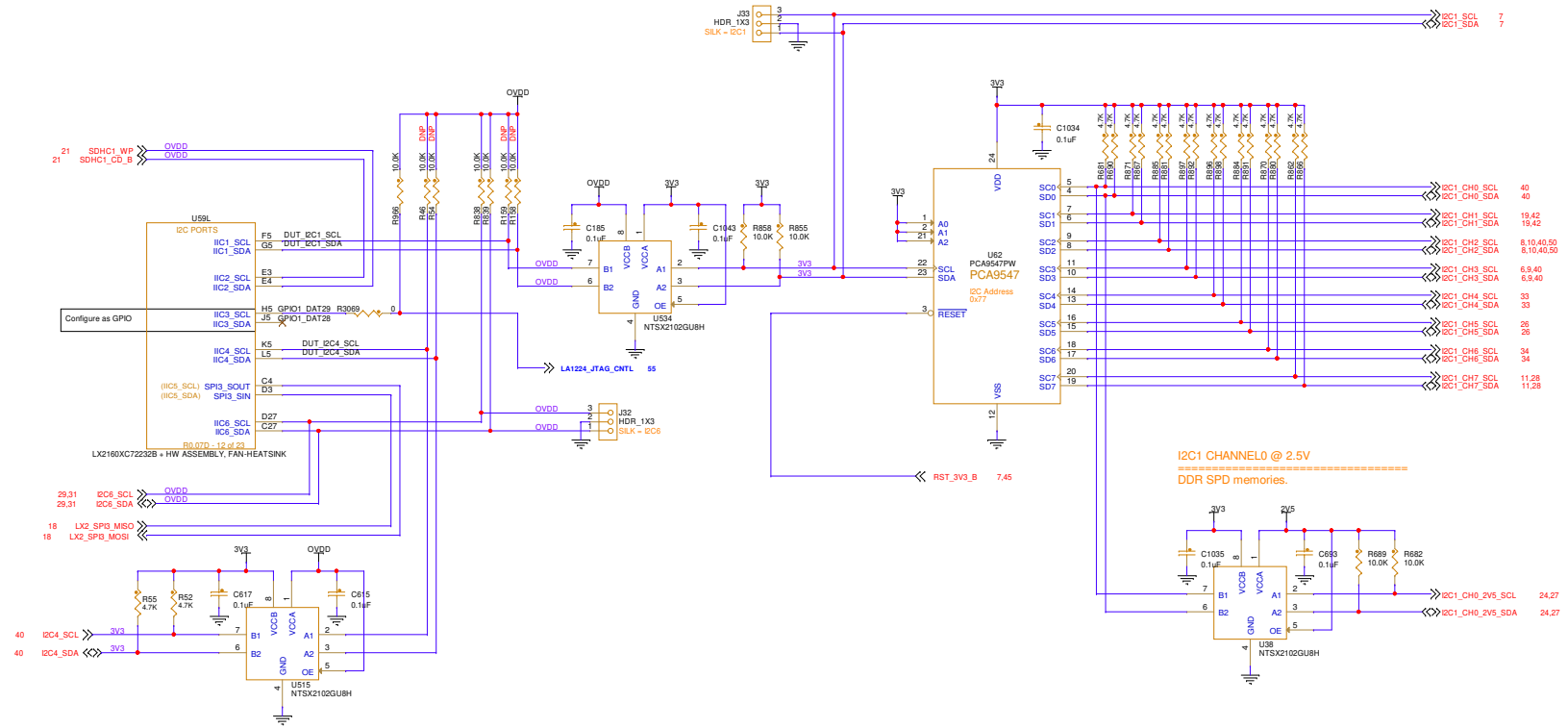


|                                                 |                        |                         |       |
|-------------------------------------------------|------------------------|-------------------------|-------|
| Classification: Public Information              |                        |                         |       |
| Drawing Title: <b>LA1224-RDB-BLS</b>            |                        |                         |       |
| Page Title: <b>RGMII PHY #1 &amp; Connector</b> |                        |                         |       |
| Size C                                          | Document Number        | SCH-54892/PDF-SPF-54892 | Rev A |
| Date:                                           | Tuesday, June 07, 2022 | Sheet 37 of 87          |       |

# LX2160 USB 3.0 PORTS



# LX2160 I2C Ports and Multiplexers



Classification: Public Information

Drawing Title: **LA1224-RD8-BLS**

Page Title: **LX2160 I2C Ports / Muxes**

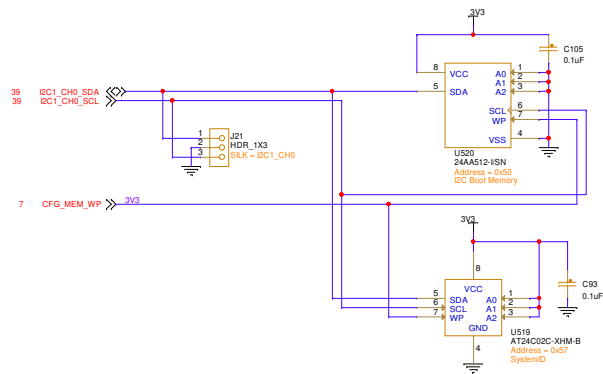
Size C Document Number SCH-54892/PDF: SPF-54892

Date: Tuesday, June 07, 2012 Sheet 39 of 87

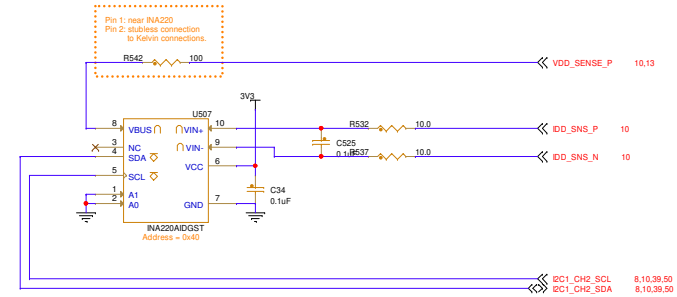
Rev A

## Misc. I2C Devices

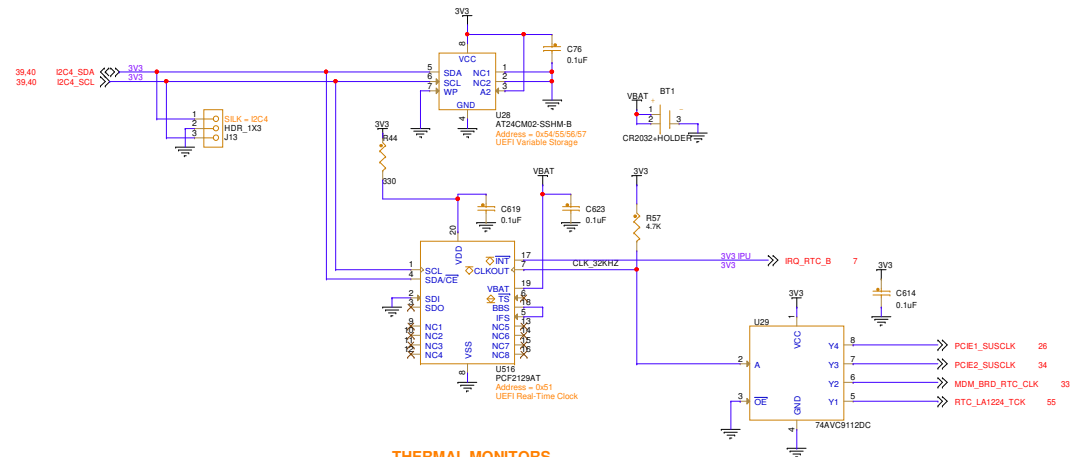
## I2C BOOT AND SYSTEM ID EEPROMS



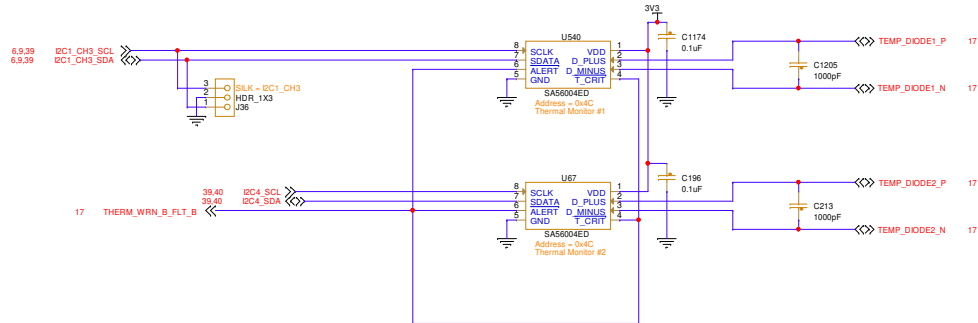
## CURRENT MEASUREMENT



## UEFI DOMAIN



## THERMAL MONITORS



**Classification: Public Information**

Drawing Title:

**LA1224-RDB-BLS**

Page Title:

## Misc. I2C Devices

Size

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|-----------------|--|
| Document Number |  |
|-----------------|--|

SCH-54992/PDF: SPF-54992

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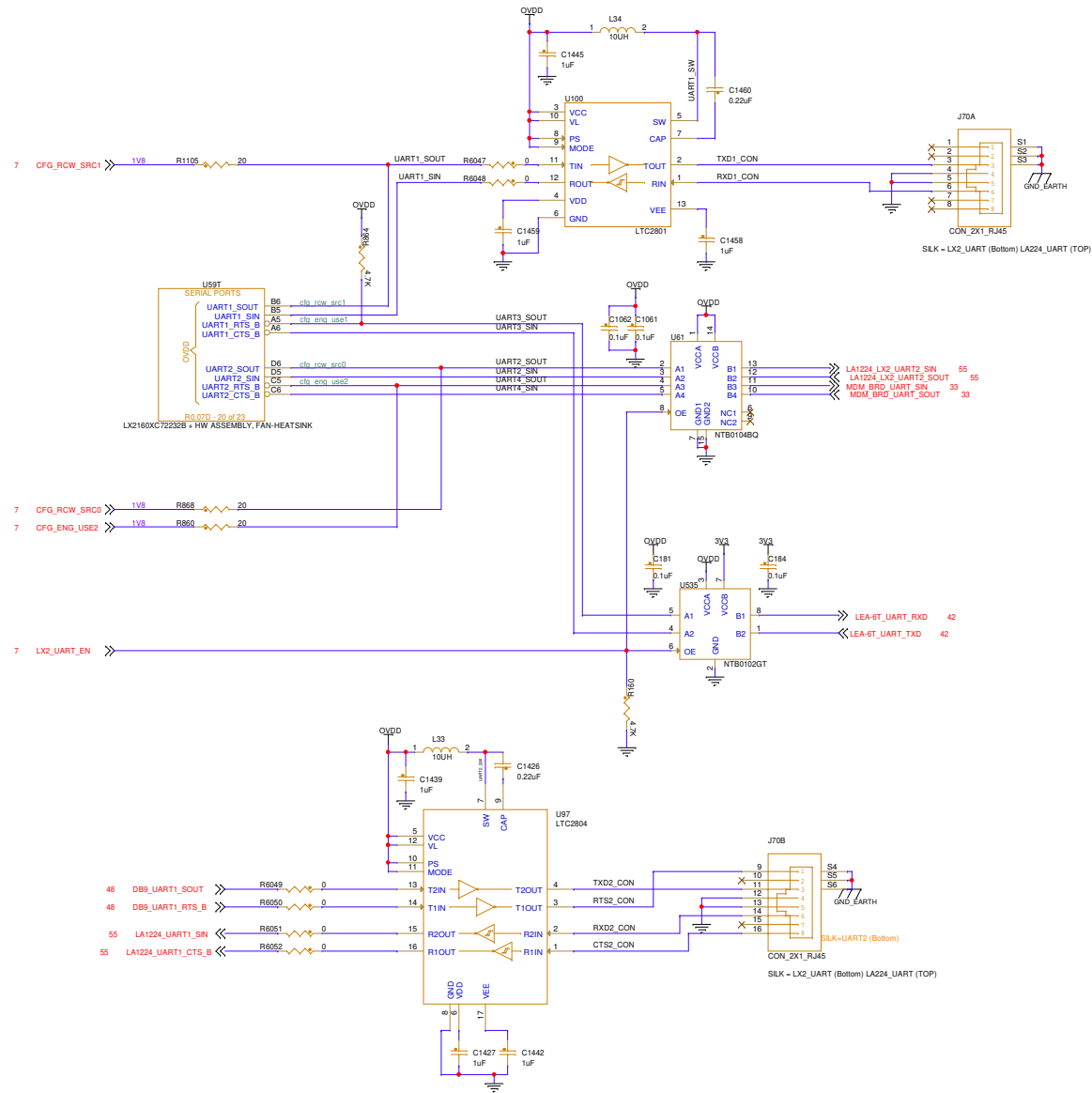
Tuesday, June 07, 2011

2022

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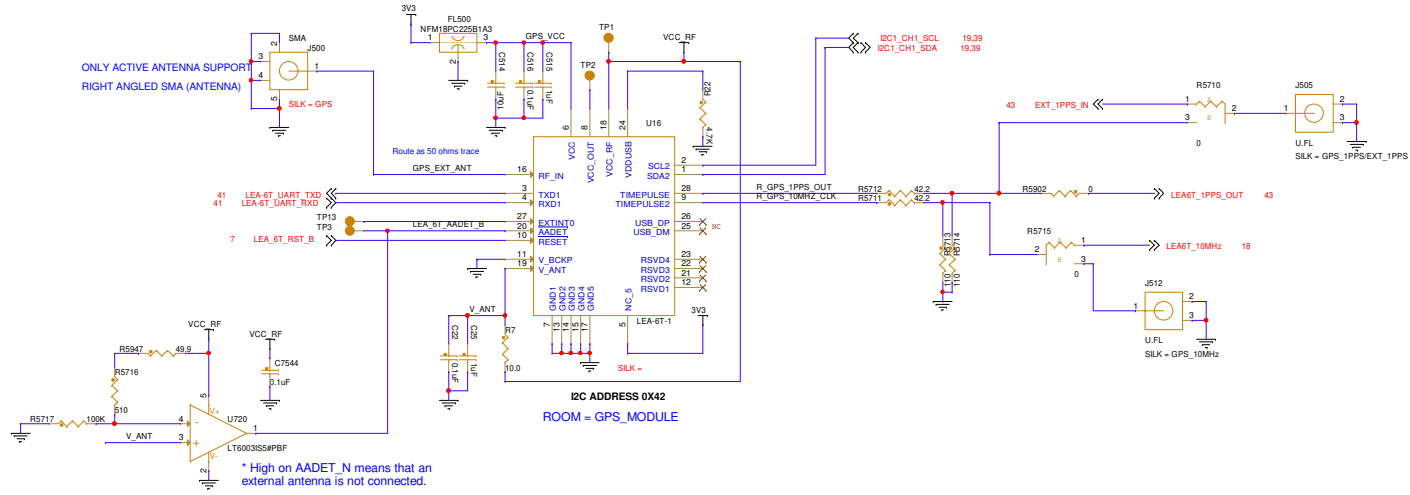
Rev

# UART INTERFACES

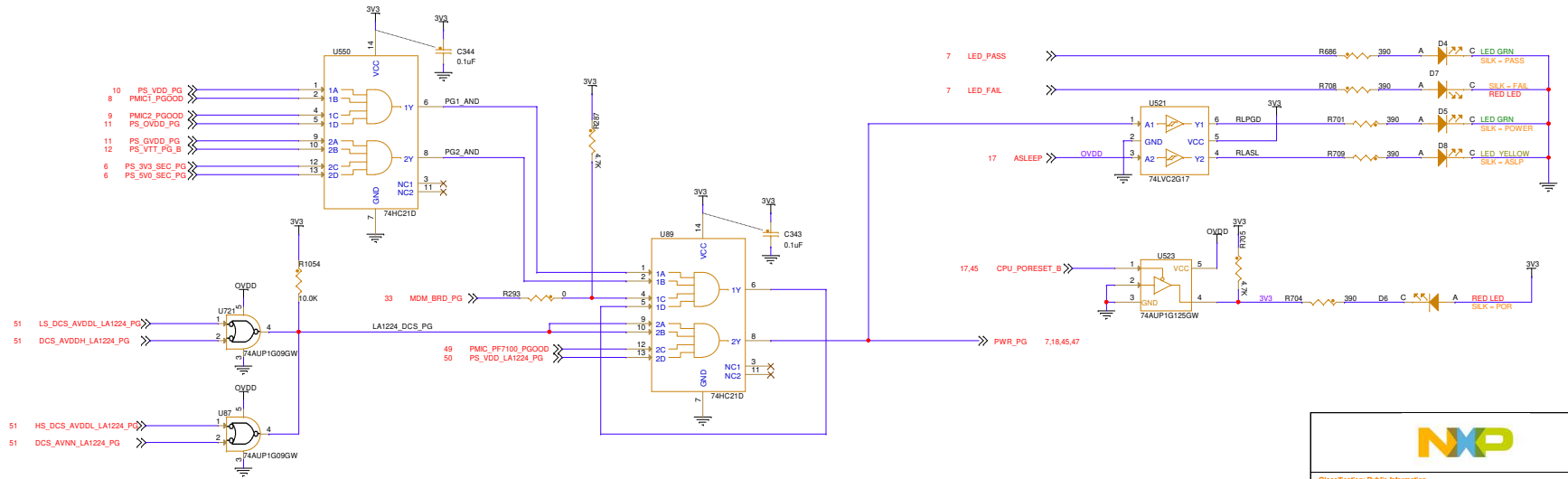


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|------------------------------------------|------------------------------------------|-------|--|
| Classification: Public Information       |                                          |       |  |
| Drawing Title: <b>LA1224-RDB-BLS</b>     |                                          |       |  |
| Page Title: <b>RS232 UART and CAN IO</b> |                                          |       |  |
| Size C                                   | Document Number SCH-54892/PDF: SPF-54892 | Rev A |  |
| Date: Tuesday, June 07, 2022             | Sheet 41 of 87                           |       |  |

## GPS MODULE



## SYSTEM MONITORING



**Classification: Public Information**

Drawing Title: **LA1224-RDB-BLS**

Page Title: **LEA6T & Misc**

|           |                                             |
|-----------|---------------------------------------------|
| Size<br>C | Document Number<br>SCH-54992/PDF: SPF-54992 |
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|-------|------------------------|-------|----|----|----|
| Date: | Tuesday, June 07, 2022 | Sheet | 42 | of | 67 |
|-------|------------------------|-------|----|----|----|

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# PPS\_SYNC\_MAPPING

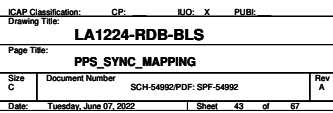
The schematic diagram illustrates the PPS\_SYNC\_MAPPING circuit. It features several key components and signal paths:

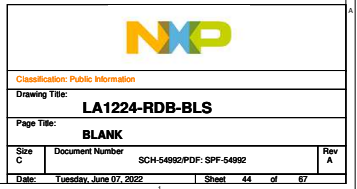
- Input Pins:** 42 LEA6T\_1PPS\_OUT, 42 EXT\_1PPS\_IN, 36 LX2\_1588\_PULSE\_OUT, 7 CFG\_MUX\_1PPS\_ATIME, 6 LX2\_TRIG\_IN, 3 LX2\_1588\_OUT, 10 reserved, 11 LX2\_1PPS\_OUT.
- ICs:** U905 (NX3L451PW, 118), U906 (NX3DV42GU), U907 (SI53365-B-GT), U928 (SP61110PGG8).
- Resistors:** R5892, R5893, R5894, R5895, R5896, R5897, R5898, R5899, R5900, R5901.
- Capacitors:** C7667, C7669, C7670, C7671, C7672.
- Signal Paths:** 1PPS\_OUT, LX2\_1588\_PULSE\_OUT1, LX2\_1588\_TRIG\_IN, 1PPS\_MUX\_OUT, CLK, DNP, UFL\_1PPS\_OUT, SLK = 1PPS\_OUT.
- Legend:** CFG\_MUX\_1PPS\_S(0:1) - 1PPS Source Selection, 0: GPS\_1PPS, 01: EXT\_1PPS, 10: reserved, 11: LX2\_1PPS\_OUT.

U907 & U928 are for dual footprint support

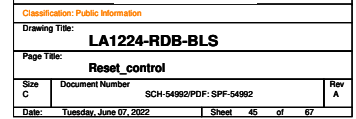
| Size | Document Number          | Rev |
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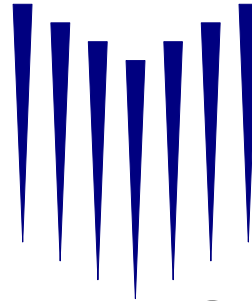
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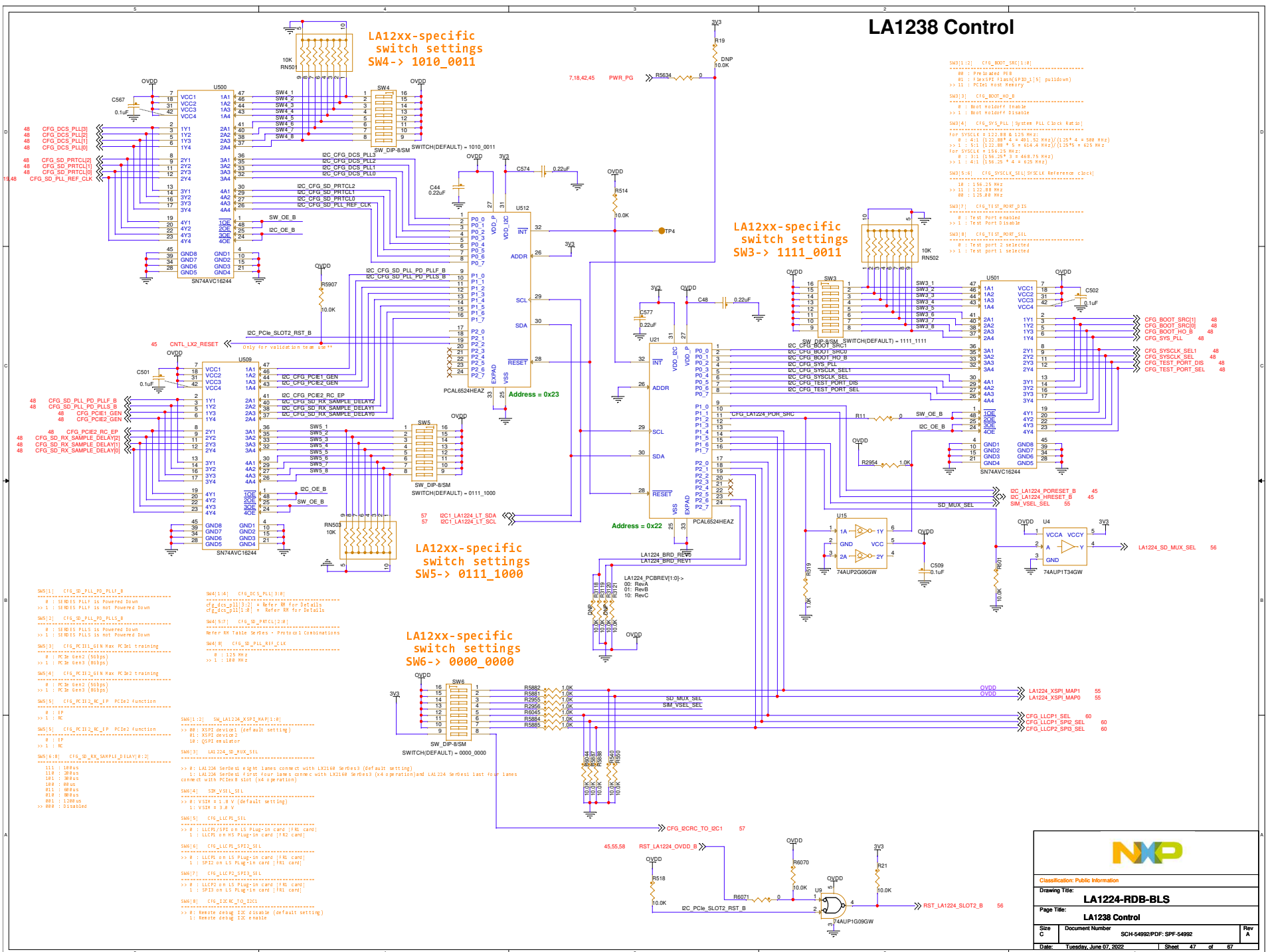




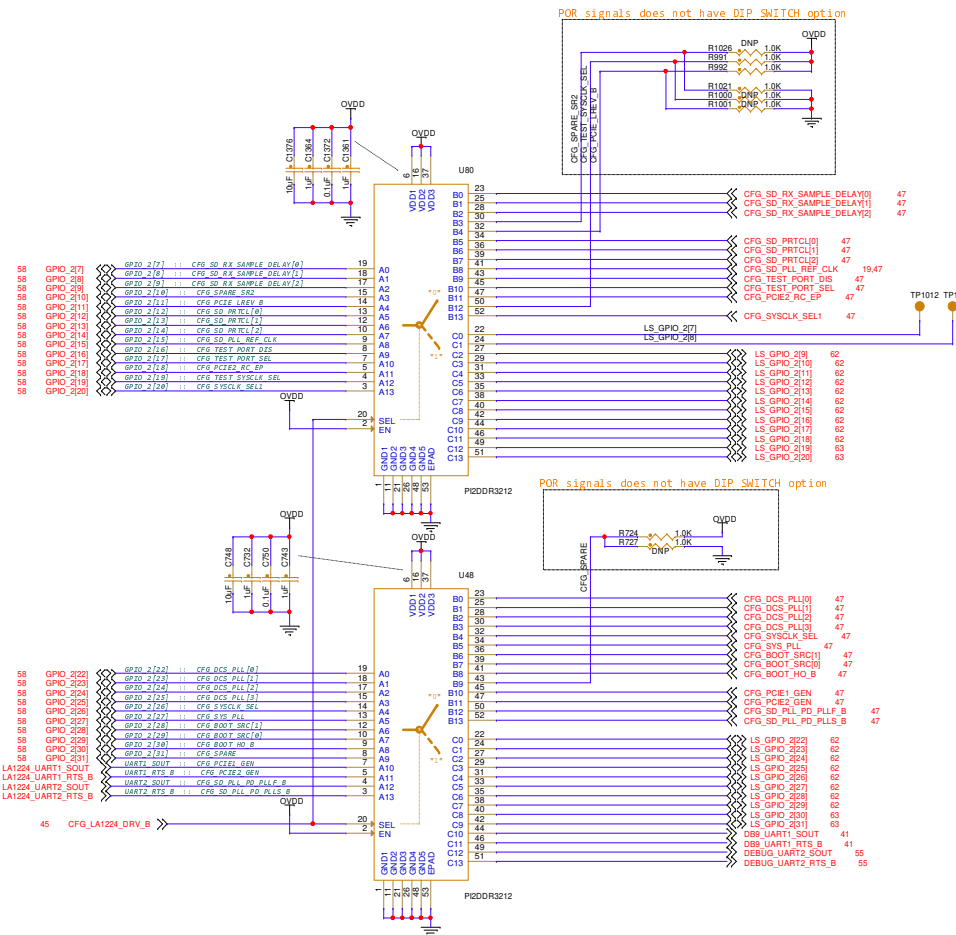
# *LA1238 SECTION*



|                                      |                                             |          |
|--------------------------------------|---------------------------------------------|----------|
| EAP Classification: CP: BUC: X PUB:  |                                             |          |
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| Page Title: <b>LA1238 SECTION</b>    |                                             |          |
| Size<br>C                            | Document Number<br>SCH-54892/PDF: SPF-54892 | Rev<br>A |
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## LA1238 POR CONFIGURATION



```

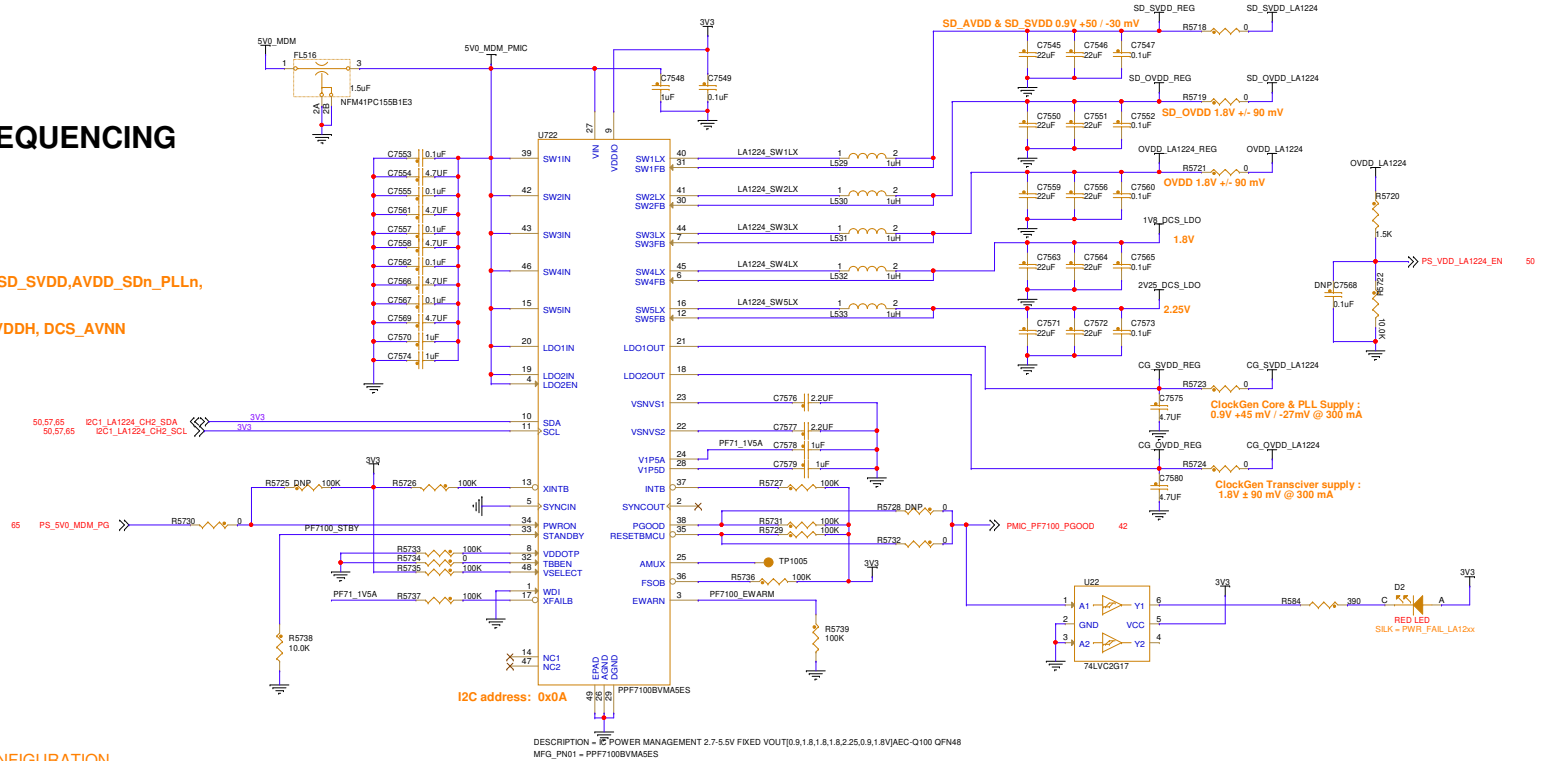
GPIO_2[27] :: CFG50_RX_SAMPLE_DELAY[0]
GPIO_2[8] :: CFG50_RX_SAMPLE_DELAY[1]
GPIO_2[19] :: CFG50_RX_SAMPLE_DELAY[2]
GPIO_2[10] :: CFG50_SPARE_SR2
GPIO_2[11] :: CFG50_PCIE1_LVB_B
GPIO_2[12] :: CFG50_SR2_PRTCL[0]
GPIO_2[13] :: CFG50_PRTCL[1]
GPIO_2[14] :: CFG50_PRTCL2
GPIO_2[15] :: CFG50_SR2_PLL_REF_CLK
GPIO_2[16] :: CFG50_TEST_PORT_SEL
GPIO_2[17] :: CFG50_TEST_PORT_SEL
GPIO_2[18] :: CFG50_PCIE2_RC_EP
GPIO_2[19] :: CFG50_TEST_SYSCLK_SEL
GPIO_2[20] :: CFG50_SYSCLK_SEL
GPIO_2[22] :: CFG50_DCS_PLL[0]
GPIO_2[23] :: CFG50_DCS_PLL[1]
GPIO_2[24] :: CFG50_DCS_PLL[2]
GPIO_2[25] :: CFG50_DCS_PLL[3]
GPIO_2[26] :: CFG50_SYSCLK_SEL
GPIO_2[27] :: CFG50_SYSCLK_SEL
GPIO_2[28] :: CFG50_BOOT_SRC[1]
GPIO_2[29] :: CFG50_BOOT_SRC[0]
GPIO_2[30] :: CFG50_BOOT_MD_B
GPIO_2[31] :: CFG50_SPARE
UART1_SOUT :: CFG50_PCIE1_GEN
UART1_RTS_B :: CFG50_PCIE2_GEN
UART1_TXD :: CFG50_SR2_PLT_PD_PLIF_B
UART2_RTS_B :: CFG50_SR2_PLT_PD_PLIF_B

```

# PF7100 PMIC SUPPLIES FOR LA12XX

## LA1238 POWER SEQUENCING

TIER 0  
\*\*OVDD  
#####  
TIER 1  
\*\* VDD  
#####  
TIER 2  
, CG\_OVDD, CG\_SVDD, SD\_OVDD, SD\_SVDD, AVDD\_SDn\_PLLn,  
#####  
TIER 3  
LS/HS DCS\_AVDDL/CVDD, DCS\_AVDDH, DCS\_AVNN  
#####



### PF7100 CONFIGURATION

\*\* SW[1] -> 0.90V [SD\_SVDD:LA12xx]  
\*\* SW[2] -> 1.80V [SD\_OVDD:LA12xx]  
\*\* SW[3] -> 1.80V [OVDD:LA12xx]---> ENABLE VDD SUPPLY  
\*\* SW[4] -> 1.80V [LDO input for LS\_AVDD&CVDD][0.8/1.2V], HS\_AVDD 1.2V:LA12xx]---> ENABLE AVNN SUPPLY  
\*\* SW[5] -> 2.25V [LDO input for HS\_LS\_AVDDH 1.8V:LA12xx]  
\*\* LDO[1] -> 0.9V [CG\_SVDD,CG\_AVDD:LA12xx]  
\*\* LDO[2] -> 1.8V [CG\_OVDD:LA12xx]

### SEQUENCE:

-> SW[3]  
<----- Delay >-----> PF200 tONSWx=310uS max  
-> LDO1.LDO2 SW[1].SW[2]  
<----- Delay >----->  
-> SW[4].SW[5]  
<----- Delay >----->  
-> PGOOD, MCU\_RESET\_B



Classification: Public Information

Drawing Title:

LA1224-RDB-BLS

Page Title:

PF7100 PMIC SUPPLY

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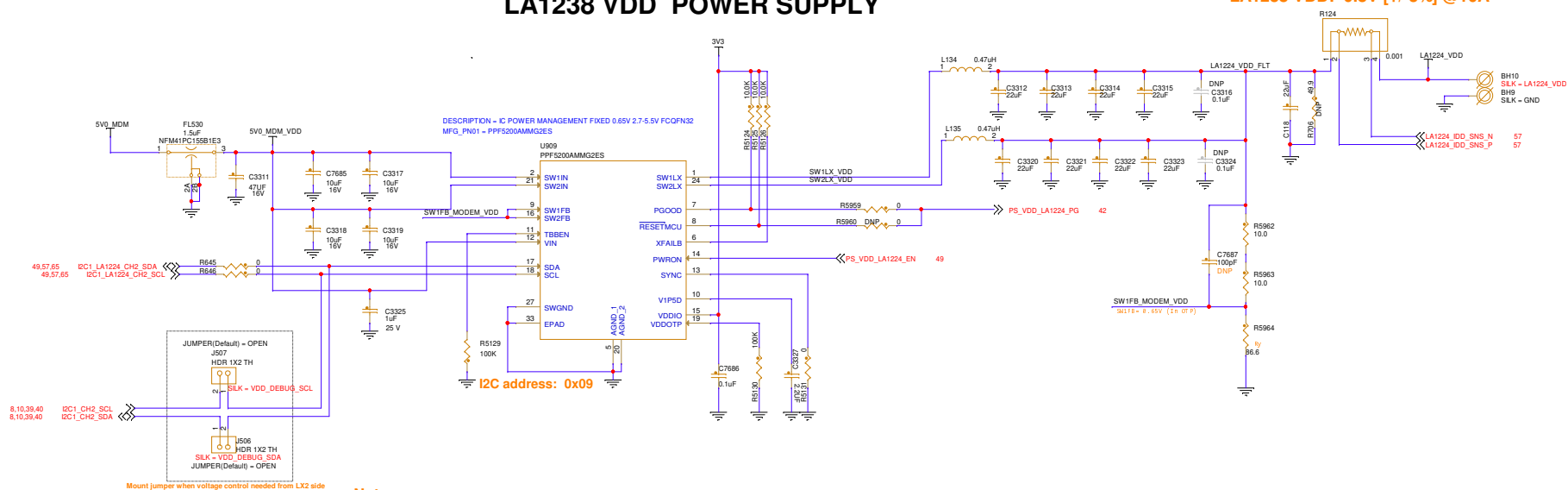
of

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Rev

A

**LA1238 VDD: 0.8V [ $\pm 3\%$ ] @16A**



\*\* PPF5200AMMG2ES OTP programmed set to default output to 0.65V.

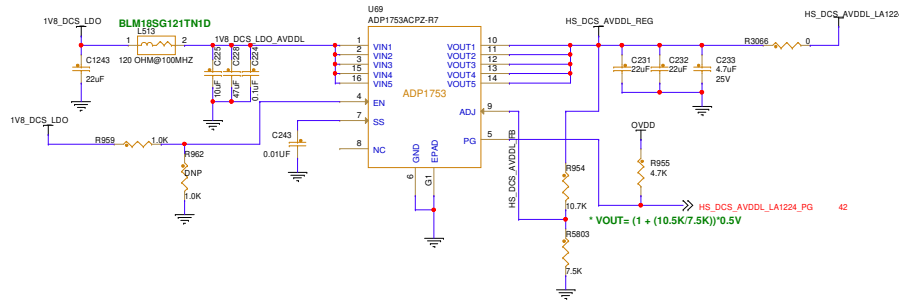
\*\* Bridge resistor will elevate the voltage on LA1224\_VDD\_FLT to 0.8V. This allow manual tuning through resistors without need for OTP change



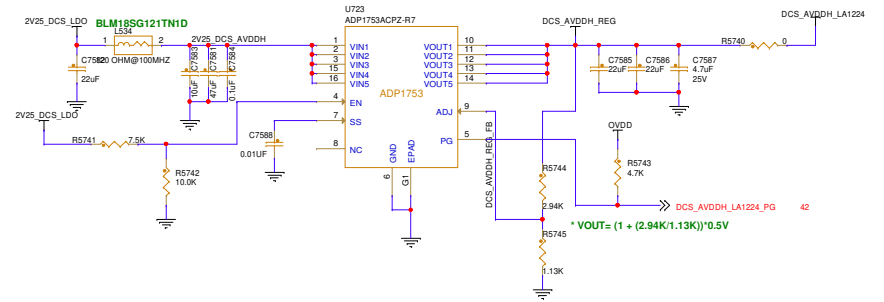
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| <b>LA1224-RDB-BLS</b> |                          |       |        |       |
| Page Title:           |                          |       |        |       |
| <b>LA1238 VDD</b>     |                          |       |        |       |
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|                       | SCH-54992/PDF: SPF-54992 |       |        |       |
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# LA1238 DCS SUPPLY

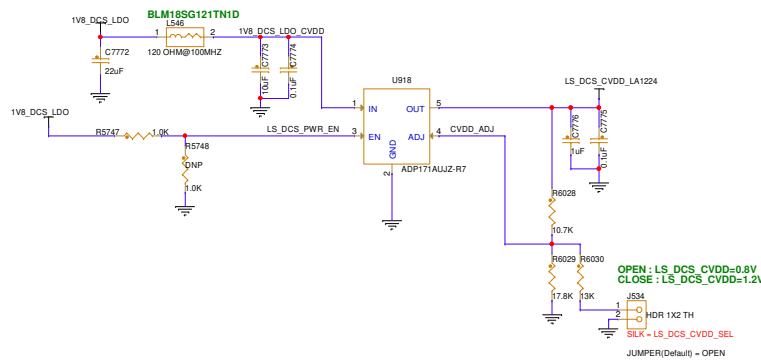
MODEM HS\_DCS\_AVDD: 1.2V @ 1.2A MAX



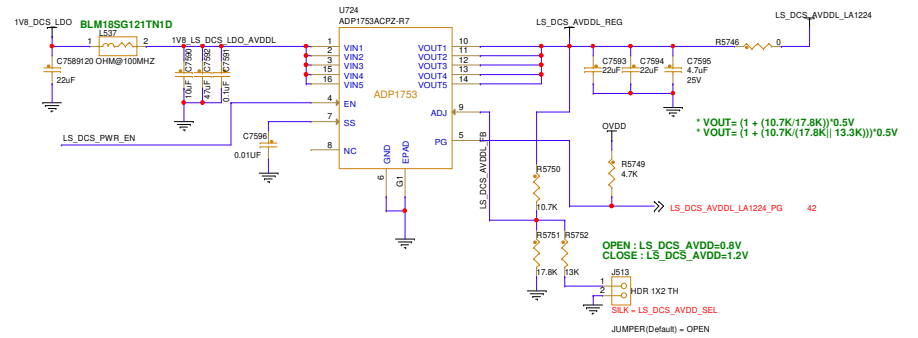
MODEM DCS\_AVDDH : 1.8V @ 800 mA MAX



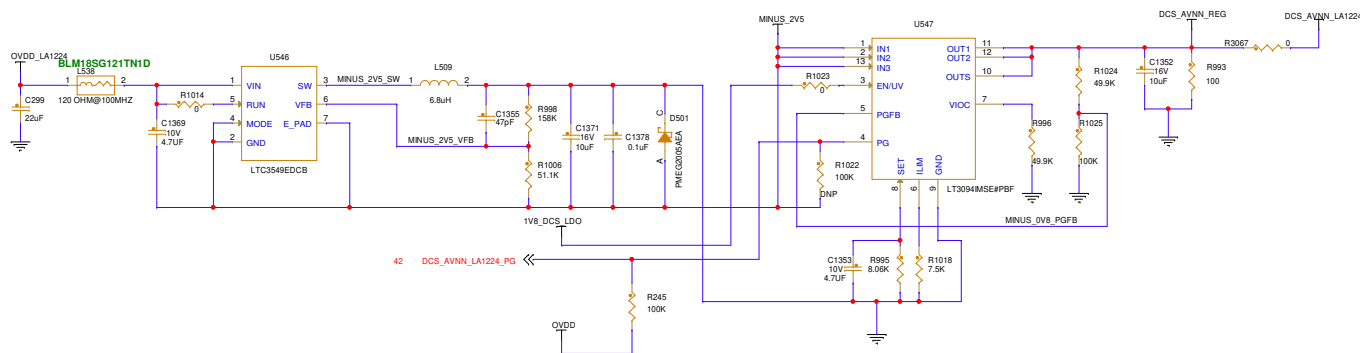
MODEM LS\_DCS\_CVDD: 0.8V/1.2V @ 300 mA MAX



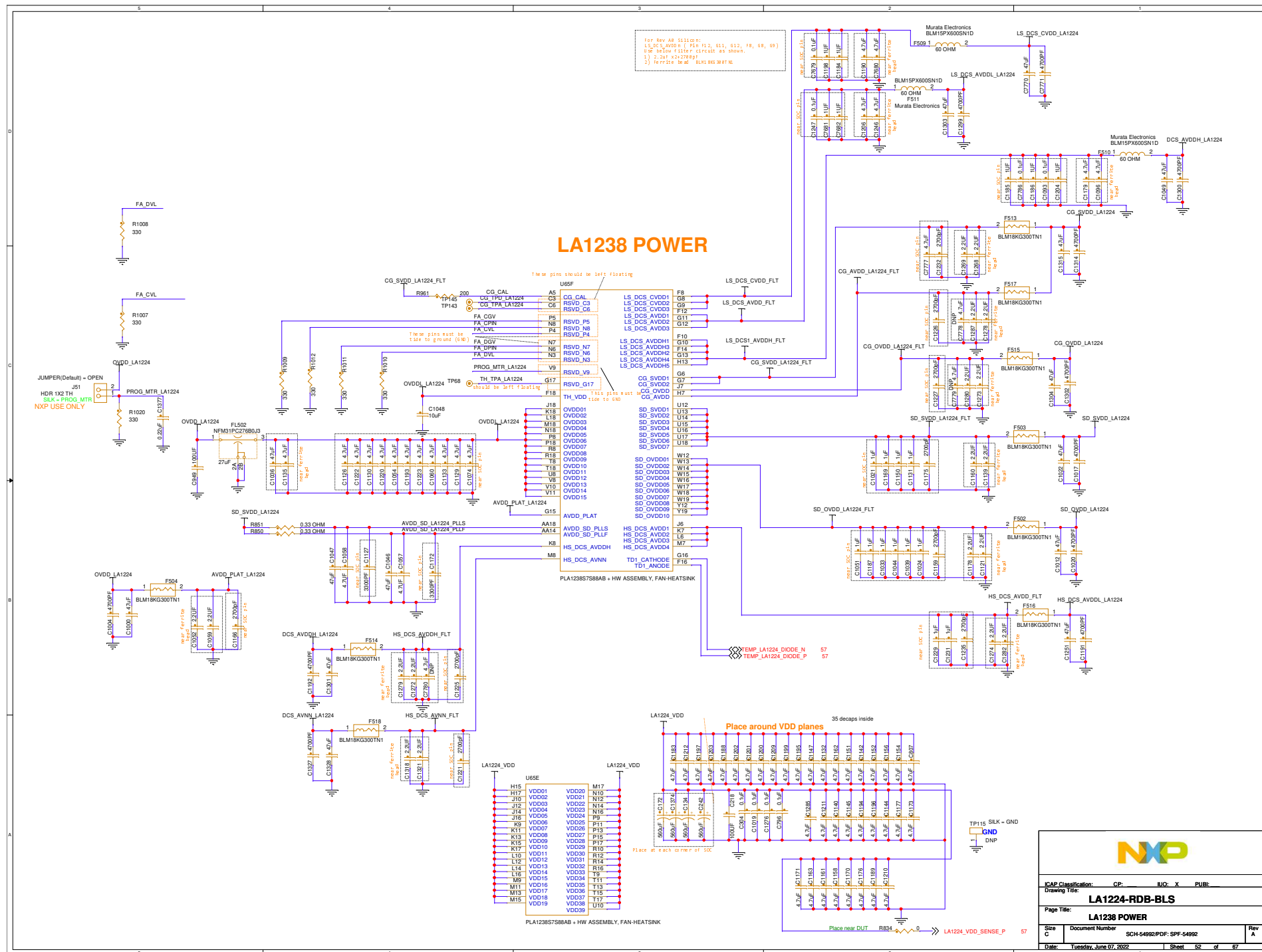
MODEM LS\_DCS\_AVDD: 0.8V/1.2V @ 800 mA MAX



DCS AVNN POWER SUPPLIES : - 0.8V ± 24 mV @ 500 mA

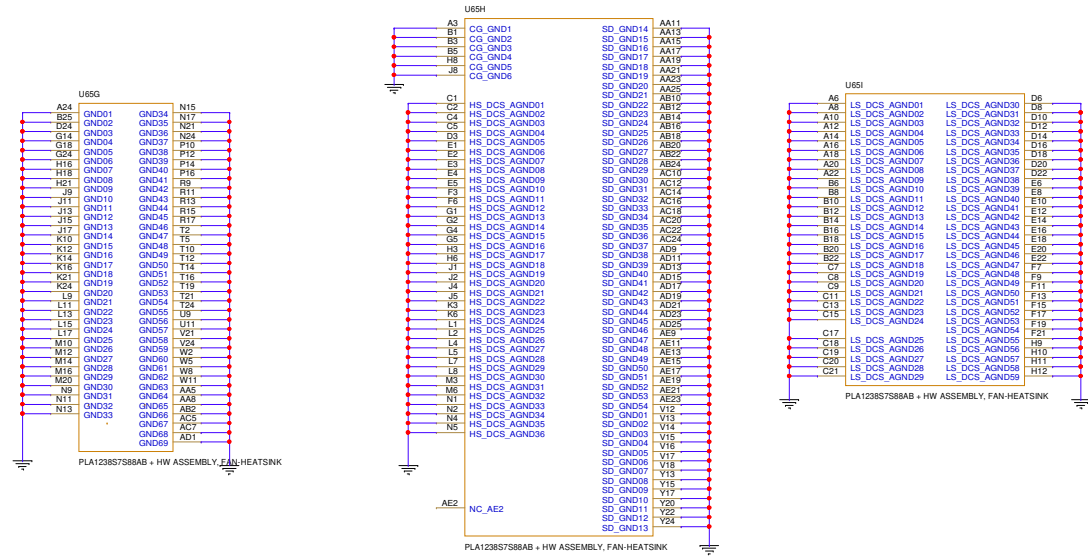


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| Drawing Title: LA1224-RDB-BLS |                 |                     |       |
| Page Title: LA1238 DCS SUPPLY |                 |                     |       |
| Size C                        | Document Number | SCH-54892/PDF-54892 | Rev A |
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# LA1238 GND



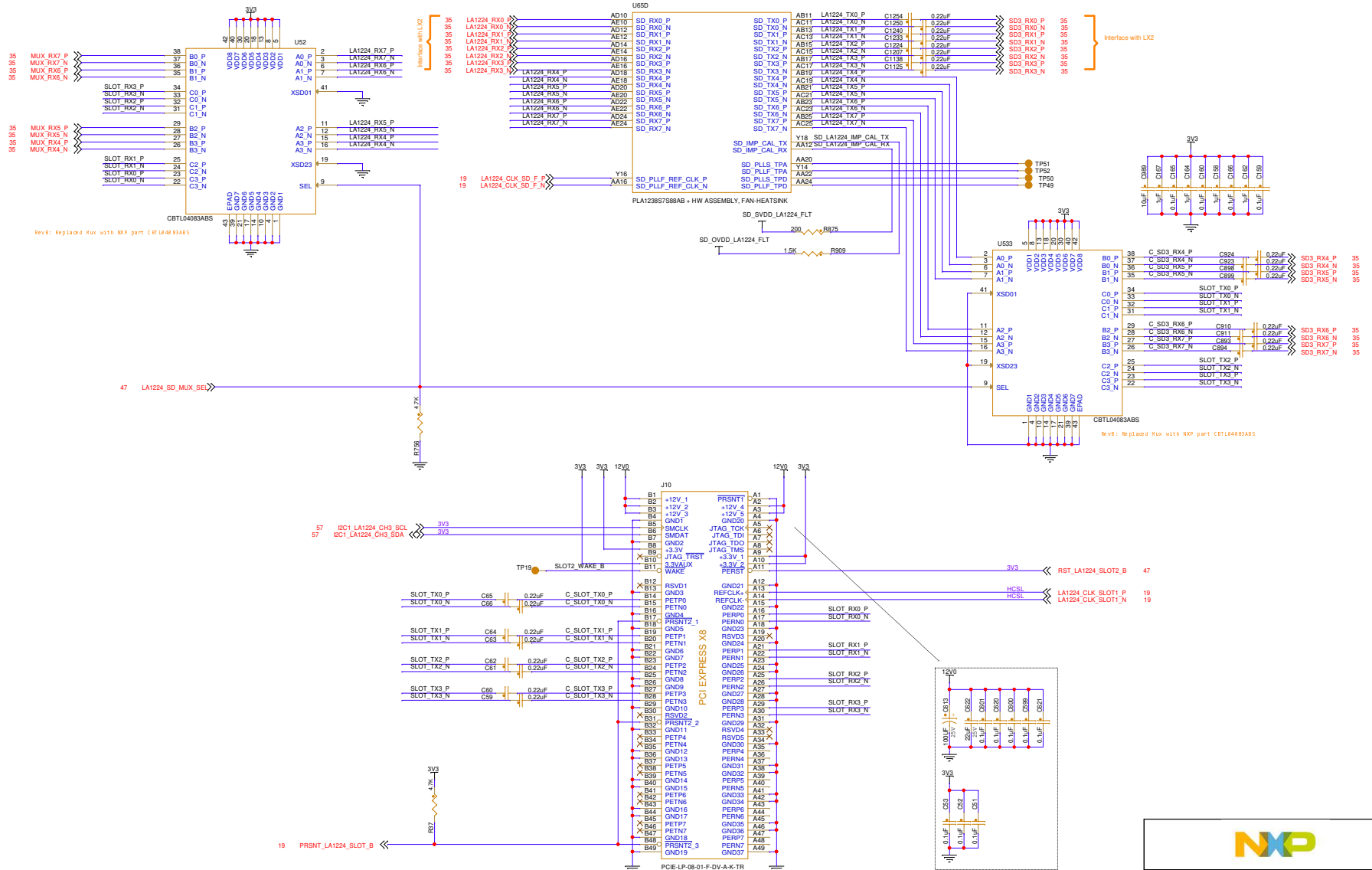
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| B |   |   |   | B |
| A |   |   |   | A |
| 5 | 4 | 3 | 2 | 1 |



|                     |                          |                |     |    |      |
|---------------------|--------------------------|----------------|-----|----|------|
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| C                   | SCH-54892/PDF: SPF-54892 |                |     |    | A    |
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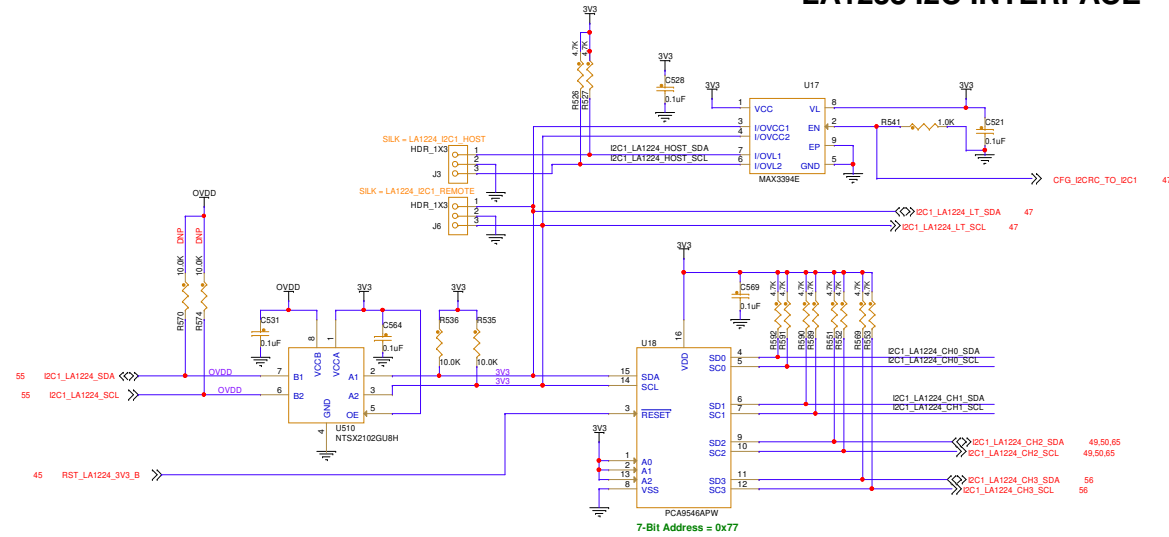
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## SERDES CONTROLLER

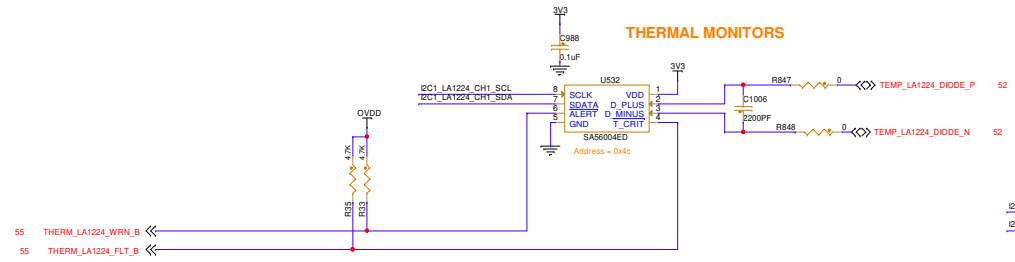
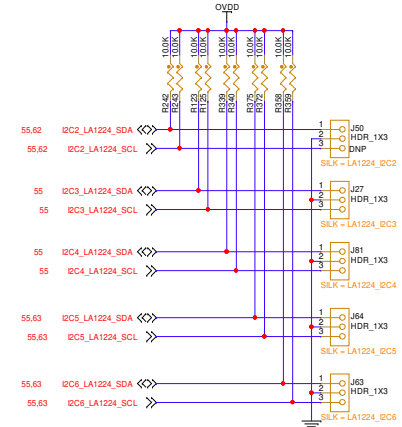


|                                 |                                          |     |        |                |
|---------------------------------|------------------------------------------|-----|--------|----------------|
| ICAP Classification:            |                                          | CP: | IJO: X | PUB:           |
| Drawing Title:                  |                                          |     |        |                |
| <b>LA1224-RDB-BLS</b>           |                                          |     |        |                |
| Page Title:                     |                                          |     |        |                |
| <b>LA1238 SERDES CONTROLLER</b> |                                          |     |        |                |
| Size C                          | Document Number SCH-54992/PDF: SPF-54992 |     |        |                |
| Date:                           | Tuesday, June 07, 2022                   |     |        | Sheet 56 of 60 |

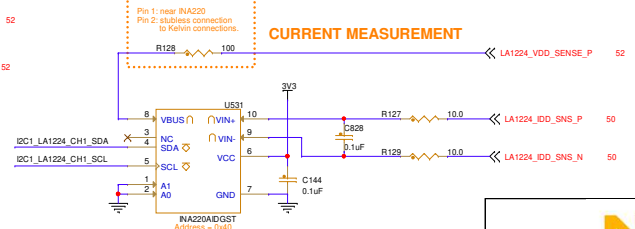
# LA1238 I2C INTERFACE



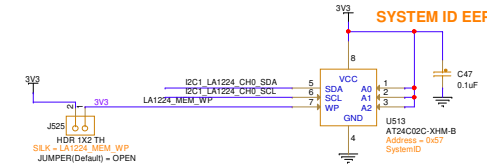
## I2C Headers



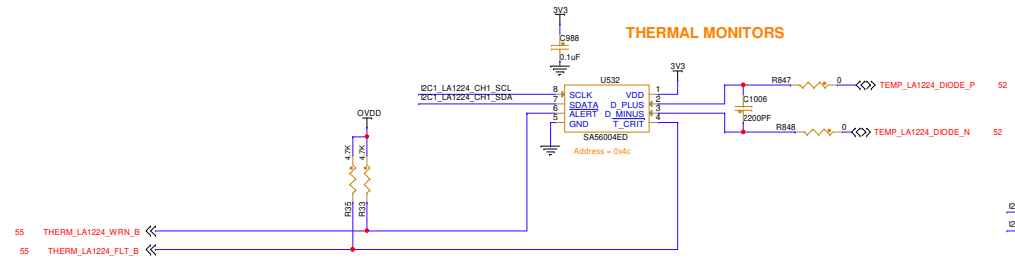
## CURRENT MEASUREMENT



## SYSTEM ID EEPROMS

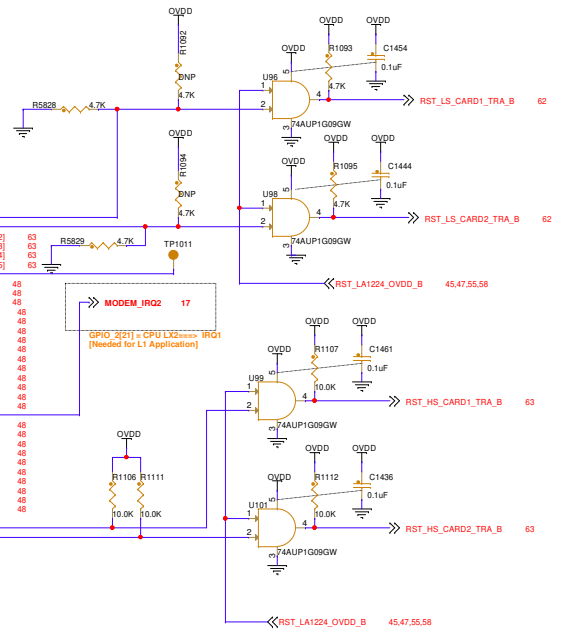
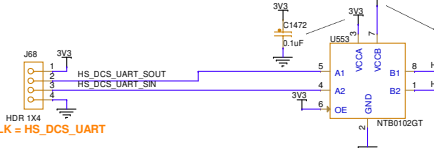
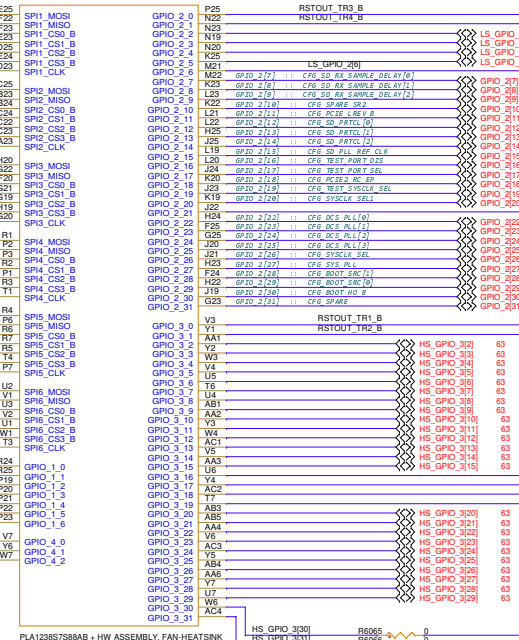
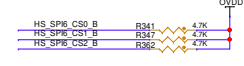
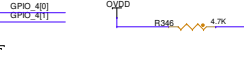
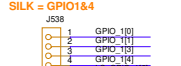
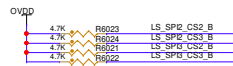
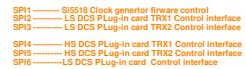


## THERMAL MONITORS



|                                               |                                             |     |                |       |
|-----------------------------------------------|---------------------------------------------|-----|----------------|-------|
| ICAP Classification:                          |                                             | CP: | IUC: X         | PUB:  |
| Drawing Title:<br><b>LA1224-RDB-BLS</b>       |                                             |     |                |       |
| Page Title:<br><b>LA1238 I2C Ports/ Muxes</b> |                                             |     |                |       |
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## RF\_CTL Subsystem for LS\_DCS & HS\_DCS



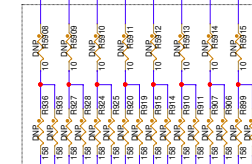
```

GPI0_2[7] : CFG_SD_RX_SAMPLE_DELAY
GPI0_2[8] : CFG_SD_RX_SAMPLE_DELAY
GPI0_2[9] : CFG_SD_RX_SAMPLE_DELAY
GPI0_2[10] : CFG_SPAR_SR2
GPI0_2[11] : CFG_PCIE_TREVB_B
GPI0_2[12] : CFG_SD_PRTCL[0]
GPI0_2[13] : CFG_SD_PRTCL[1]
GPI0_2[14] : CFG_SD_PRTCL[2]
GPI0_2[15] : CFG_SD_PLL_REF_CLK
GPI0_2[16] : CFG_FST_TEST_PORT_SEL
GPI0_2[17] : CFG_FST_TEST_PORT_SEL
GPI0_2[18] : CFG_PCIE2_EC_EP
GPI0_2[19] : CFG_FST_SYSLCK_SEL
GPI0_2[20] : CFG_SYSLCK_SEL
GPI0_2[21] : CFG_DCS_PLL[0]
GPI0_2[22] : CFG_DCS_PLL[1]
GPI0_2[23] : CFG_DCS_PLL[2]
GPI0_2[24] : CFG_DCS_PLL[2]
GPI0_2[25] : CFG_DCS_PLL[3]
GPI0_2[26] : CFG_SYSLCK_SEL
GPI0_2[27] : CFG_FST_PLL
GPI0_2[28] : CFG_BOOT_SR[1]
GPI0_2[29] : CFG_BOOT_SR[0]
GPI0_2[30] : CFG_BOOT_SR[0]
GPI0_2[31] : CFG_SPAR
UART1_S0UT : CFG_PCIE1_GEN
UART1_S0UT_B : CFG_PC2_GEN
UART2_S0UT : CFG_SD_PLL_P0_PLLF_B
UART2_RTS_B : CFG_SD_PLL_P0_PLLF_B

```

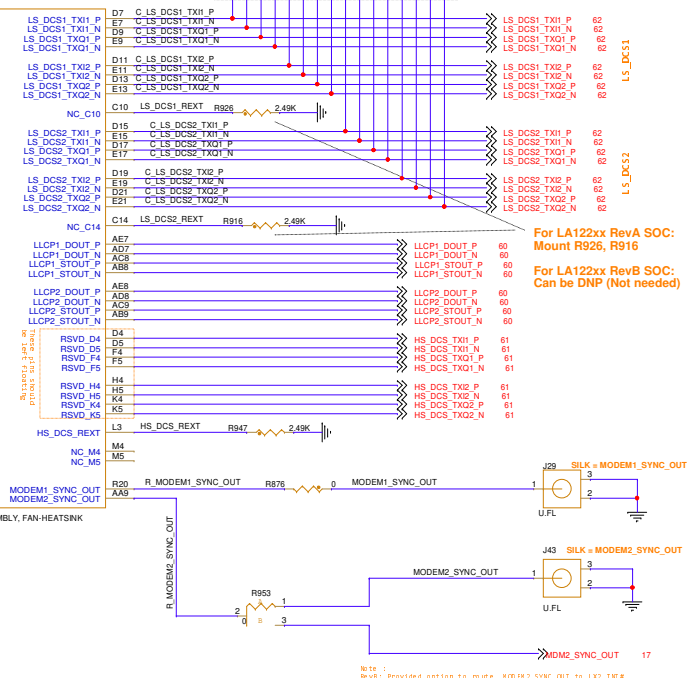
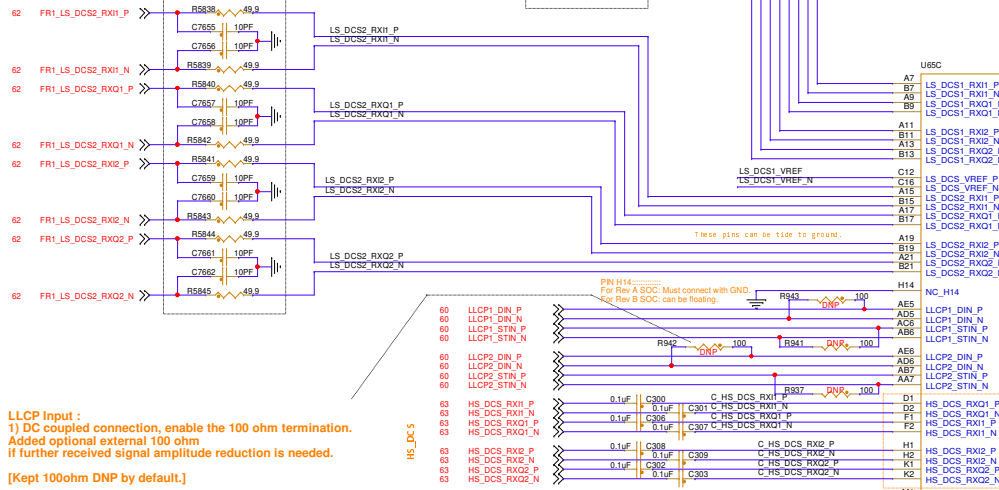
# Low-Speed & High Speed ADC/DAC Macros

I-V conversion Load resistor placed at the plug-in card.

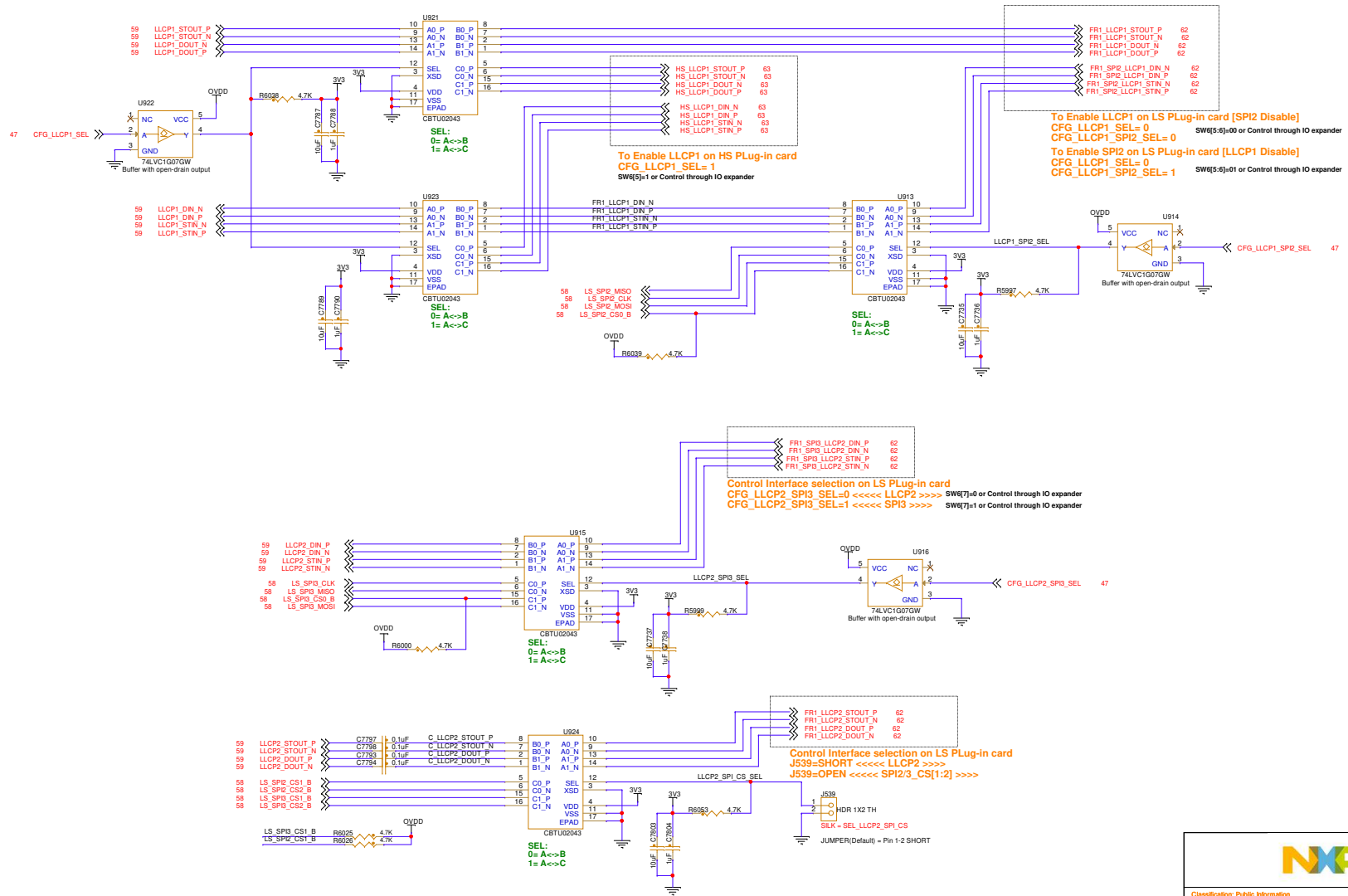


I-V conversion  
RevA LA12xx: Rdiff-> 50 ohm, Rcm-> 0 ohm  
RevB LA12xx: Rdiff-> 156 ohm, Rcm-> 10 ohm  
For full Swing output use  
RevB LA12xx: Rdiff-> 237 ohm, Rcm-> 23.2 ohm

Kick-Back Filter  
RevA LA12xx: R1-> 50 ohm, C1-> 10pF  
RevB LA12xx: R1-> 50 ohm, C1-> 10pF



## LLCP [1:2] & SPI[2:3] MUXING



**Classification: Public Information**

Drawing Title: **LA1224-RDB-BLS**

Page Title: **LLCP [1:2] MUXING**

|           |                                             |
|-----------|---------------------------------------------|
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|-----------|---------------------------------------------|

|       |                        |       |    |    |    |
|-------|------------------------|-------|----|----|----|
| Date: | Tuesday, June 07, 2022 | Sheet | 60 | of | 67 |
|-------|------------------------|-------|----|----|----|





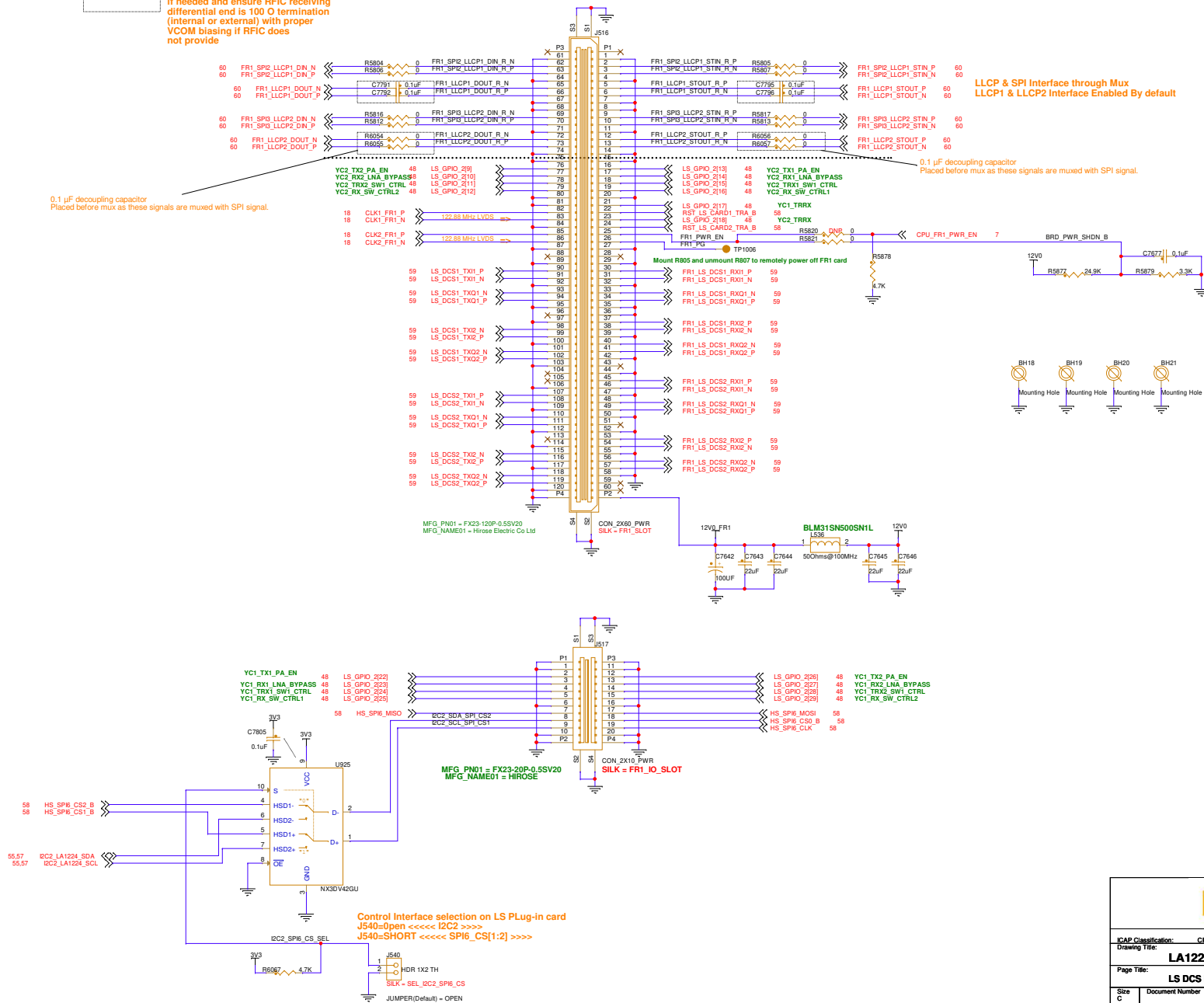
# LS DCS PLUG CARD

0.1  $\mu$ F decoupling capacitor  
if needed and ensure RFIC receiving  
differential end is 100  $\Omega$  termination  
(internal or external) with proper  
VCOM biasing if RFIC does  
not provide

0.1  $\mu$ F decoupling capacitor  
Placed before mux as these signals are muxed with SPI signal.

LLCP & SPI Interface through Mux  
LLCP1 & LLC2 Interface Enabled By default

0.1  $\mu$ F decoupling capacitor  
Placed before mux as these signals are muxed with SPI signal.



|                      |                                          |     |        |       |       |
|----------------------|------------------------------------------|-----|--------|-------|-------|
| ICAP Classification: |                                          | CP: | BUC: X |       | PUBL: |
| Drawing Title:       |                                          |     |        |       |       |
| LA1224-RDB-BLS       |                                          |     |        |       |       |
| Page Title:          |                                          |     |        |       |       |
| LS DCS PLUG CARD     |                                          |     |        |       |       |
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# HS DCS PLUG CARD

0.1  $\mu$ F decoupling capacitor if needed and ensure RFIC receiving differential end is 100  $\Omega$  termination (Internal or external) with proper VCOM biasing if RFIC does not provide

LLCP1 Interface (Routed through Mux)

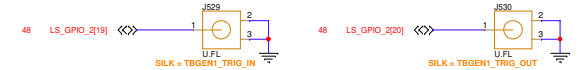
Ref\_CLK for Plug-in Card  
Note:  
Sync Clock out from RF transceiver (122.88MHz Default)  
Could be LVDS, LVPECL, HCSL and CML

HS DCS DAC Input to LA122xx (Through Buffer) (Ac-coupled)

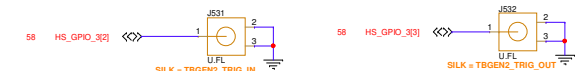
## Power Connector for Plug-in card [ Optional ]

## TBGEN TRIG\_IN, TRIG\_OUT & SYNC\_IN [1.8V]

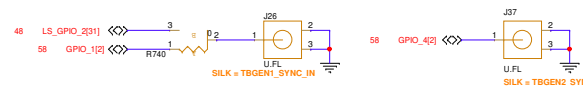
### TBGEN1\_TRIG\_IN & TRIG\_OUT



### TBGEN2\_TRIG\_IN & TRIG\_OUT



### TBGEN[1:2] SYNC\_IN



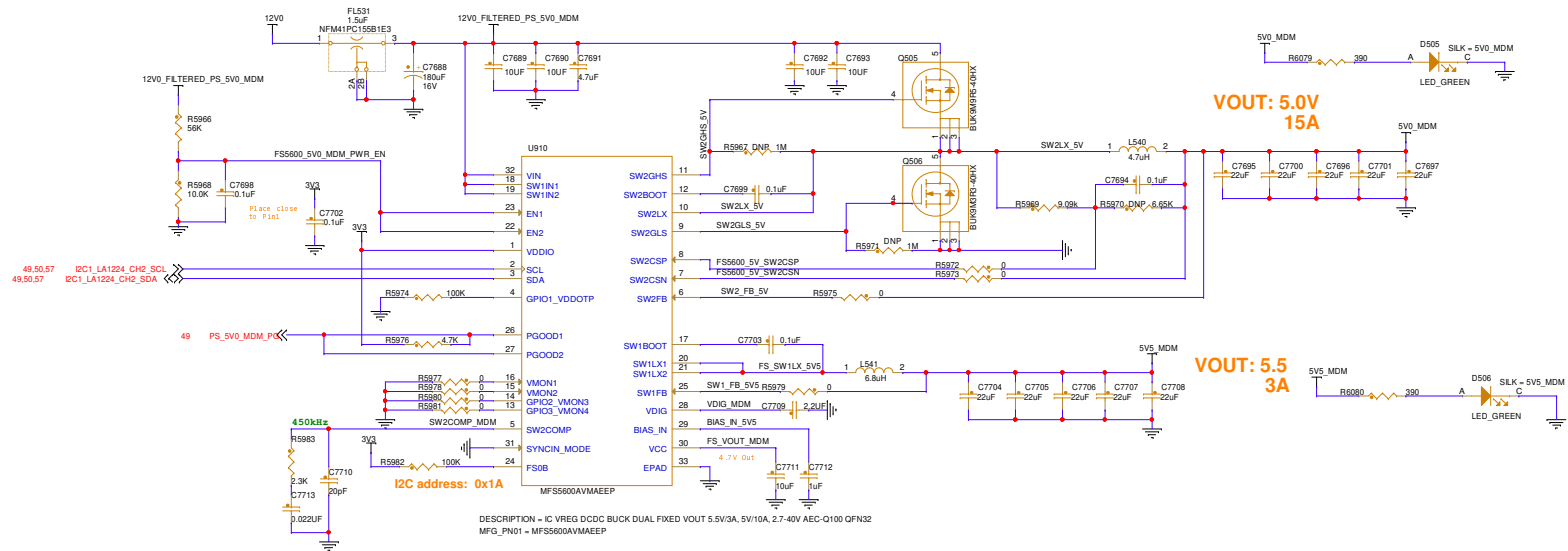
|                                      |                        |                          |       |
|--------------------------------------|------------------------|--------------------------|-------|
| RAP Classification: CP               |                        | DOC: X                   | PUBL  |
| Drawing Title: <b>LA1224-RDB-BLS</b> |                        |                          |       |
| Page Title: <b>HS DCS PLUG CARD</b>  |                        |                          |       |
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|   |   |   |   |   |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D |   |   |   | D |
| C |   |   |   | C |
| B |   |   |   | B |
| A |   |   |   | A |
| 5 | 4 | 3 | 2 | 1 |

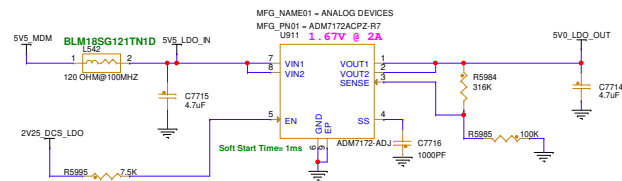


|                                    |                                          |       |  |
|------------------------------------|------------------------------------------|-------|--|
| Classification: Public Information |                                          |       |  |
| Drawing Title: LA1224-RDB-BLS      |                                          |       |  |
| Page Title: BLANK                  |                                          |       |  |
| Size C                             | Document Number SCH-54892/PDF: SPF-54892 | Rev A |  |
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## 5V0 and 5.5V POWER SUPPLY [ For LA12xx]




## 5V0 (LDO for HS DCS Buffers) POWER SUPPLY



|                                   |                          |       |        |       |
|-----------------------------------|--------------------------|-------|--------|-------|
| ICAP Classification:              |                          | CP:   | IUC: X | PUBL: |
| Drawing Title:                    |                          |       |        |       |
| <b>LA1224-RDB-BLS</b>             |                          |       |        |       |
| Page Title:                       |                          |       |        |       |
| <b>5V &amp; 5.5V POWER SUPPLY</b> |                          |       |        |       |
| Size C                            | Document Number          |       |        | Rev A |
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SWITCH(DEFAULT)-LIST

| REF DES | SWITCH(DEFAULT) | PAGE NAME            |
|---------|-----------------|----------------------|
| SW1     | 1111 0011       | 007 - CPU Control    |
| SW3     | 1111 1111       | 047 - LA1238 Control |
| SW4     | 1010 0011       | 047 - LA1238 Control |
| SW5     | 0111 1000       | 047 - LA1238 Control |
| SW6     | 0000 0000       | 047 - LA1238 Control |



EAP Classification:

CP:

DOC: X

PUBL:

Drawing Title:

LA1224-RDB-BLS

Page Title:

DIP SWITCH

Size

C

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## DNP LIST

| REF DES                                                                                                                                                                       | ASSY_OPT | PAGE NAME                       |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|---------------------------------|
| F1,J82,R5636,R5653                                                                                                                                                            |          | 006 - Power ENTRY               |
| R5637,R5639,R5654,R5656,<br>R5657,R5658,R5923,R5931,TP24,<br>TP90                                                                                                             | DNP      | 006 - Power_ENTRY               |
| R113,R728                                                                                                                                                                     | DNP      | 007 - CPU Control               |
| R977,R1016                                                                                                                                                                    | DNP      | 008 - PF8100 PMIC1 SUPPLIES     |
| R918,R957                                                                                                                                                                     | DNP      | 009 - PF8100 PMIC2 SUPPLIES     |
| R599,R602,R640                                                                                                                                                                | DNP      | 010 - VDD                       |
| C7721,C7726,R5674,R5990                                                                                                                                                       | DNP      | 011 - OVDD & GVDD               |
| R8                                                                                                                                                                            | DNP      | 012 - VTT POWER                 |
| C895,C953,C979,C1016,F500,<br>F501,F505,F507,J19                                                                                                                              | DNP      | 014 - LX2160 GVDD/OVDD/SDVDD    |
| R177,R179,R771,R826,R827,<br>R830,R843,R933,R939                                                                                                                              | DNP      | 017 - LX2160 System Ctl. & JTAG |
| Y6                                                                                                                                                                            |          | 018 - Si5518 SYSTEM CLK         |
| C7629,R5775,R5777,R5800,<br>R5825,R6004,R6085,R6086,Y8                                                                                                                        | DNP      | 018 - Si5518 SYSTEM CLK         |
| R667,R671                                                                                                                                                                     | DNP      | 019 - SYSTEM CLK2               |
| R74,R87,R661,R685,R754                                                                                                                                                        | DNP      | 020 - LX2160 XSPI               |
| R32,R36,R53,R56,R61,R624                                                                                                                                                      | DNP      | 021 - LX2160 SDHC1 Port & Slot  |
| U34A,U34B                                                                                                                                                                     | DNP      | 022 - LX2160 SDHC2 + eMMC       |
| R715                                                                                                                                                                          | DNP      | 023 - LX2160 DDR Ports          |
| J14,R698                                                                                                                                                                      | DNP      | 026 - LX2160 SD #1              |
| R130,R131                                                                                                                                                                     | DNP      | 027 - DS250DF230 25GE Retimer   |
| R883                                                                                                                                                                          | DNP      | 029 - AQR113 #1 10G PHY Control |
| R153,R155,R887,R893                                                                                                                                                           | DNP      | 033 - LX2160 SD #2/PCle CONN    |
| J5,R568,R603                                                                                                                                                                  | DNP      | 034 - PCIe M.2 SLOT             |
| C1040,C1050,R877,R904                                                                                                                                                         | DNP      | 036 - LX2160 RGMII / MII / IEEE |
| C297,C298,C321,C325,R247,<br>R1037,R5953,Y5                                                                                                                                   | DNP      | 037 - RGMII PHY #1 & Connector  |
| R46,R54,R158,R159                                                                                                                                                             | DNP      | 039 - LX2160 I2C Ports / Muxes  |
| BT1                                                                                                                                                                           |          | 040 - Misc. I2C Devices         |
| U907                                                                                                                                                                          | DNP      | 043 - PPS SYNC MAPPING          |
| R730,R5906                                                                                                                                                                    | DNP      | 045 - Reset control             |
| R19,R3118,R3120                                                                                                                                                               | DNP      | 047 - LA1238 Control            |
| R727,R1000,R1001,R1026                                                                                                                                                        | DNP      | 048 - LA1238 POR CONFIG         |
| C7568,R5725,R5728                                                                                                                                                             | DNP      | 049 - PF7100 PMIC SUPPLY        |
| C3316,C3324,C7687,R706,R5960                                                                                                                                                  | DNP      | 050 - LA1238 VDD                |
| R5752,R6030                                                                                                                                                                   |          | 051 - LA1238 DCS SUPPLY         |
| R962,R1022,R5748                                                                                                                                                              | DNP      | 051 - LA1238 DCS SUPPLY         |
| C1021,C1024,C1033,C1039,<br>C1044,C1051,C1131,C1150,<br>C1169,C1187,C1229,C1231                                                                                               |          | 052 - LA1238 POWER              |
| C7778,C7779,C7780,TP115                                                                                                                                                       | DNP      | 052 - LA1238 POWER              |
| R115,R609,R633,R700,R806,<br>R945,R946,R980,R5852,R5855                                                                                                                       | DNP      | 055 - LA1238 JTAG, IRQ, XSPI    |
| J50,R570,R574                                                                                                                                                                 | DNP      | 057 - LA1238 I2C Ports/ Muxes   |
| R1092,R1094                                                                                                                                                                   | DNP      | 058 - LA1238 RF CTL Subsystem   |
| R921,R922                                                                                                                                                                     |          | 059 - LA1238 DCS IQ             |
| C1180,R899,R902,R906,R907,<br>R910,R911,R914,R915,R919,<br>R920,R924,R925,R927,R928,<br>R935,R936,R937,R941,R942,<br>R943,R5908,R5909,R5910,R5911,<br>R5912,R5913,R5914,R5915 | DNP      | 059 - LA1238 DCS IQ             |
| U551,U552                                                                                                                                                                     |          | 061 - HS DCS BUFFER             |
| R1079,R1080,R1081,R1082,<br>R1084,R1085,R1086,R1087,<br>R1088,R1089,R1090,R1091,<br>R1097,R1098,R1099,R1100,<br>R1101,R1102,R1103,R1104                                       |          | 061 - HS DCS_BUFFER             |
| R5820                                                                                                                                                                         | DNP      | 062 - LS DCS PLUG CARD          |
| R6058                                                                                                                                                                         | DNP      | 063 - HS DCS PLUG CARD          |
| R5966                                                                                                                                                                         |          | 065 - 5V & 5.5V POWER SUPPLY    |
| R5967,R5970,R5971                                                                                                                                                             | DNP      | 065 - 5V & 5.5V POWER SUPPLY    |

## JUMPER(DEFAULT)- LIST

| REF DES   | JUMPER(DEFAULT) | PAGE NAME                       |
|-----------|-----------------|---------------------------------|
| J12       | OPEN            | 010 - VDD                       |
| J19,J20   | OPEN            | 014 - LX2160 GVDD/OVDD/SDVDD    |
| J22       | Pin 1-2 SHORT   | 014 - LX2160 GVDD/OVDD/SDVDD    |
| J39       | OPEN            | 017 - LX2160 System Ctl. & JTAG |
| J44       | Pin 1-2 SHORT   | 017 - LX2160 System Ctl. & JTAG |
| J535,J536 | OPEN            | 018 - Si5518 SYSTEM CLK         |
| J40       | Pin 1-2 SHORT   | 038 - LX2160 USB 3.0 Ports      |
| J527      | OPEN            | 045 - Reset control             |
| J506,J507 | OPEN            | 050 - LA1238 VDD                |
| J513,J534 | OPEN            | 051 - LA1238 DCS SUPPLY         |
| J51       | OPEN            | 052 - LA1238 POWER              |
| J525      | OPEN            | 057 - LA1238 I2C Ports/ Muxes   |
| J515      | Pin 2-3 SHORT   | 059 - LA1238 DCS IQ             |
| J539      | Pin 1-2 SHORT   | 060 - LLC P [1:2] MUXING        |
| J540      | OPEN            | 062 - LS DCS PLUG CARD          |



Classification: Public Information

Drawing Title: **LA1224-RD8-BLS**

Page Title: **JUMPER & DNP**

|                              |                                          |       |
|------------------------------|------------------------------------------|-------|
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