


Table of Contents	
01	TITLE, TOC & REV HISTORY
02	BLOCK DIAGRAM
03	NOTES
04	CONNECTOR INTERFACE
05	HS_DCS1 TX & RX SMA PORTS
06	POWER SUPPLY

REVISION HISTORY			
Rev	Description	Date	Approved
X1	Initial Release	7-Dec-2021	Matt Carlson
X1	A070 release	17-Dec-2021	Matt Carlson
X2	Removed R1, R2, R3, R4, R89, R91, R93, R95, C1, C2, C3, C4, J32 and added J33, J34, BH5	21-Dec-2021	Matt Carlson
X3	Replaced BH1, BH2, BH3, BH4 with 280-76195	18-Jan-2022	Matt Carlson
X4	Removed R80, R81, R82, R83, R84, R85, R86, R87, R26, R27, R38, R39, R50, R51, R62, R63 are set as DNP Removed C8, C10, C11, C16, C17, C22, C23, C28	20-Jan-2022	Matt Carlson
X5	Removed LED at Reset and added 3 pin headers Replaced 49.9 resistors with 1K (R26, R27, R38, R39, R50, R51, R62, R63) Added 2 LEDs at 12v and 1.8v supply	25-Jan-2022	Matt Carlson
A	A085 release	3-feb-22	Matt Carlson

X-LA1224-FR2-BRK (54705-A)

All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your NXP representative to obtain the latest information on this product.

		6501 William Cannon Drive West Austin, TX 78735-8598	
		<small>This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.</small>	
© NXP SEMICONDUCTORS Designer: Jakki Reddy		Classification: Company Internal/Proprietary Drawing Title: X-LA1224-FR2-BRK	
Drawn by: Jakki Reddy		Page Title: TITLE, TOC & REV HISTORY	
Approved: Matt Carlson	Size: C	Document Number: SCH-54705 PDF: SPF-54705	Rev: A
Date: Thursday, February 03, 2022		Sheet 1 of 6	

Bonnyrigg Rev C

LA1224

HS BRKOUT CARD

100nF 5V2D-120P-5.0V

100nF 5V2D-120P-5.0V

12V

17007

TVS

ADP1224

Q1/2

HS-DCS-HQ OUT

HS-DCS-HQ IN

LLCP1 OUT

LLCP1 IN

SPI4_MISO

SPI4_MOSI

SPI4_CS0_B

SPI4_CS1_B

SPI4_CS2_B

SPI4_CS3_B

SPI4_CLK

SPI5_MISO

SPI5_MOSI

SPI5_CS0_B

SPI5_CS1_B

SPI5_CS2_B

SPI5_CS3_B

SPI5_CLK

RES_CLK

RES_DATA

RES_STROBE

GPIO0_00

GPIO0_01

GPIO0_02

GPIO0_03

GPIO0_04

GPIO0_05

GPIO0_06

GPIO0_07

GPIO0_08

GPIO0_09

GPIO0_10

GPIO0_11

GPIO0_12

GPIO0_13

GPIO0_14

GPIO0_15

GPIO0_16

GPIO0_17

GPIO0_18

GPIO0_19

GPIO0_20

GPIO0_21

GPIO0_22

GPIO0_23

GPIO0_24

GPIO0_25

GPIO0_26

GPIO0_27

GPIO0_28

GPIO0_29

GPIO0_30

GPIO0_31

GPIO0_32

GPIO0_33

GPIO0_34

GPIO0_35

GPIO0_36

GPIO0_37

GPIO0_38

GPIO0_39

GPIO0_40

GPIO0_41

GPIO0_42

GPIO0_43

GPIO0_44

GPIO0_45

GPIO0_46

GPIO0_47

GPIO0_48

GPIO0_49

GPIO0_50

GPIO0_51

GPIO0_52

GPIO0_53

GPIO0_54

GPIO0_55

GPIO0_56

GPIO0_57

GPIO0_58

GPIO0_59

GPIO0_60

GPIO0_61

GPIO0_62

GPIO0_63

GPIO0_64

GPIO0_65

GPIO0_66

GPIO0_67

GPIO0_68

GPIO0_69

GPIO0_70

GPIO0_71

GPIO0_72

GPIO0_73

GPIO0_74

GPIO0_75

GPIO0_76

GPIO0_77

GPIO0_78

GPIO0_79

GPIO0_80

GPIO0_81

GPIO0_82

GPIO0_83

GPIO0_84

GPIO0_85

GPIO0_86

GPIO0_87

GPIO0_88

GPIO0_89

GPIO0_90

GPIO0_91

GPIO0_92

GPIO0_93

GPIO0_94

GPIO0_95

GPIO0_96

GPIO0_97

GPIO0_98

GPIO0_99

GPIO0_100

GPIO0_101

GPIO0_102

GPIO0_103

GPIO0_104

GPIO0_105

GPIO0_106

GPIO0_107

GPIO0_108

GPIO0_109

GPIO0_110

GPIO0_111

GPIO0_112

GPIO0_113

GPIO0_114

GPIO0_115

GPIO0_116

GPIO0_117

GPIO0_118

GPIO0_119

GPIO0_120

GPIO0_121

GPIO0_122

GPIO0_123

GPIO0_124

GPIO0_125

GPIO0_126

GPIO0_127

GPIO0_128

GPIO0_129

GPIO0_130

GPIO0_131

GPIO0_132

GPIO0_133

GPIO0_134

GPIO0_135

GPIO0_136

GPIO0_137

GPIO0_138

GPIO0_139

GPIO0_140

GPIO0_141

GPIO0_142

GPIO0_143

GPIO0_144

GPIO0_145

GPIO0_146

GPIO0_147

GPIO0_148

GPIO0_149

GPIO0_150

GPIO0_151

GPIO0_152

GPIO0_153

GPIO0_154

GPIO0_155

GPIO0_156

GPIO0_157

GPIO0_158

GPIO0_159

GPIO0_160

GPIO0_161

GPIO0_162

GPIO0_163

GPIO0_164

GPIO0_165

GPIO0_166

GPIO0_167

GPIO0_168

GPIO0_169

GPIO0_170

GPIO0_171

GPIO0_172

GPIO0_173

GPIO0_174

GPIO0_175

GPIO0_176

GPIO0_177

GPIO0_178

GPIO0_179

GPIO0_180

GPIO0_181

GPIO0_182

GPIO0_183

GPIO0_184

GPIO0_185

GPIO0_186

GPIO0_187

GPIO0_188

GPIO0_189

GPIO0_190

GPIO0_191

GPIO0_192

GPIO0_193

GPIO0_194

GPIO0_195

GPIO0_196

GPIO0_197

GPIO0_198

GPIO0_199

GPIO0_200

GPIO0_201

GPIO0_202

GPIO0_203

GPIO0_204

GPIO0_205

GPIO0_206

GPIO0_207

GPIO0_208

GPIO0_209

GPIO0_210

GPIO0_211

GPIO0_212

GPIO0_213

GPIO0_214

GPIO0_215

GPIO0_216

GPIO0_217

GPIO0_218

GPIO0_219

GPIO0_220

GPIO0_221

GPIO0_222

GPIO0_223

GPIO



Classification: Company Internal/Proprietary

Drawing Title:

X-LA1224-FR2-BRK

Page Title:

BLOCK DIAGRAM

Size

Document Number	
-----------------	--

SCH-54705 PDF: SPF-54705

10

Thursday, February 03, 2022 Sheet 2

10

Thursday, February 03, 2022 Sheet 2 of 6

--	--

--	--

NOTES

DNP TABLE

REF DES	ASSY. OPT	PAGE NAME
C7,C8,C9,C13,C14,C15,C19,C20, C21,C25,C26,C27,R5,R7,R9,R11, R13,R15,R17,R19,R21,R26,R27, R32,R33,R38,R39,R44,R45,R50, R51,R56,R57,R62,R63,R98	DNP	05 HS_DCS1 TX & RX SMA PORTS

STACK UP

New Heart Technology Impedance simulation report															
Customer: H161												06473			
Part number* 170-54705															
Layer Count: 6 L															
Board thickness: 1.57 mm (± 10 %) IT180															
Copper Weight: outer inner															
Date: 2022/1/14															
Once any line width/ space doesn't design in gerber data, please remove it from list to save time for engineering checking. Thanks for your cooperation.															
PCB Stack Up						Impedance									
Layer	Type	Thickness (mil)			DK	Single end +/-10%				Diff +/-10%					
Top side solder mask					0.80	mils		trace width(mil)	Ref layer	olm	simulation result	trace width / space (mil)	Ref layer	olm	simulation result
L1	TOP	Differential & Signal	copper+plating	1.20	mils		4	L2	50	49.52	3.4/7.6	L2	100	99.46	
L2			Prepreg	2.52	mils	3.85									
			copper	1.25	mils										
			core	22.00	mils	4									
L3			copper	0.63	mils		5.5	L2/L4	50	50.15					
			Prepreg	4.15	mils	4.24									
L4			copper	0.63	mils		5.5	L3/L5	50	50.15					
			core	22.00	mils	4									
L5			copper	1.25	mils										
			Prepreg	2.52	mils	3.85									
L6	Bottom	Differential & Signal	copper+plating	1.20	mils		4	L5	50	49.52	3.4/7.6	L5	100	99.46	
Bottom side solder mask					0.80	mils									
Total board thickness					60.94	mils									
					1.55	mm									

DESIGN NOTE:

Assembly changes for the loopback through resistors:

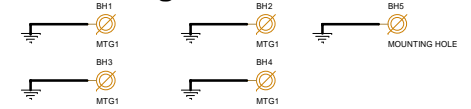
	Components need to be mount	Components need to be DNP
TX_I1	R5,R7,R21,R32	R6,R8,R25,R31
TX_Q1	R9,R11,R33,R44	R10,R12,R37,R43
TX_I2	R13,R15,R45,R56	R14,R16,R49,R55
TX_Q2	R17,R20,R57,R98	R18,R20,R61,R67



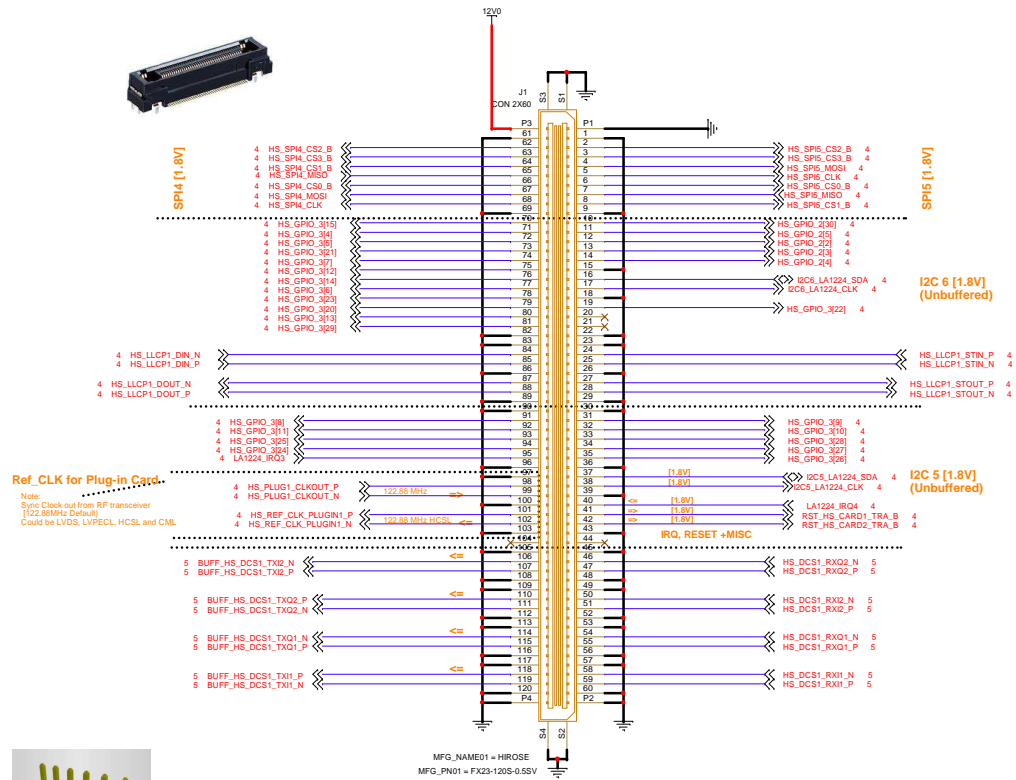
Classification: Company Internal/Proprietary			
Drawing Title: X-LA1224-FR2-BRK			
Page Title: NOTES			
Size C	Document Number	SCH-54705 PDF: SPF-54705	Rev A
Date: Thursday, February 03, 2022	Sheet	3	of 6

Interface with Bonnyrigg Main board

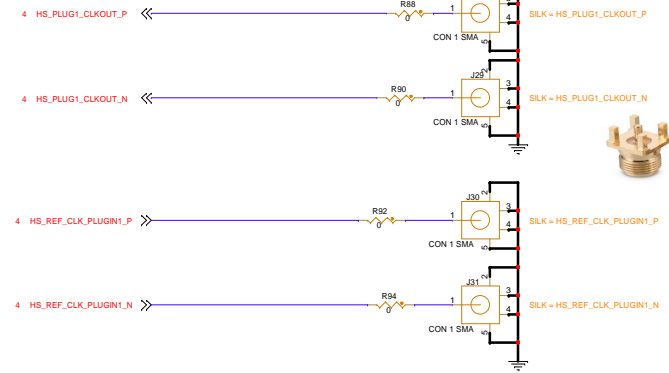
Mounting Holes



HS DCS PLUG CARD



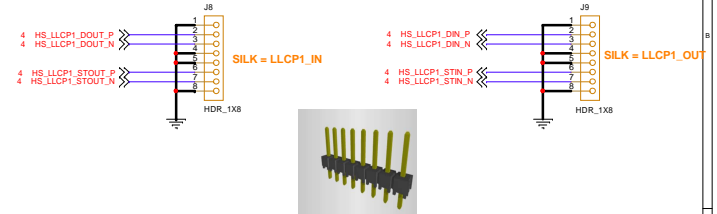
Clock SMA Conn



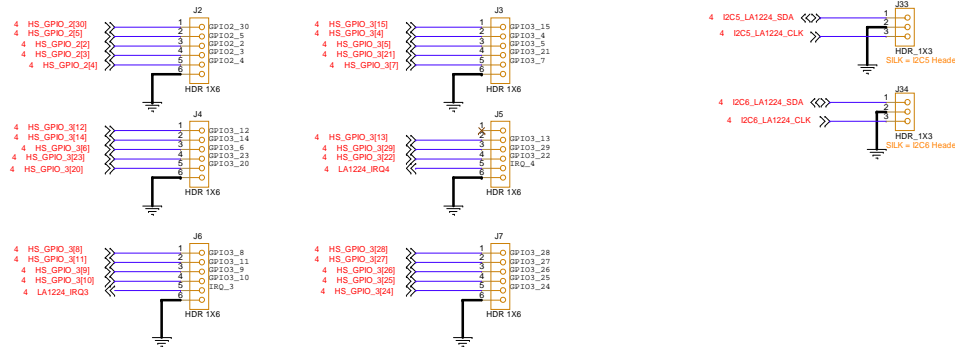
RESET Header



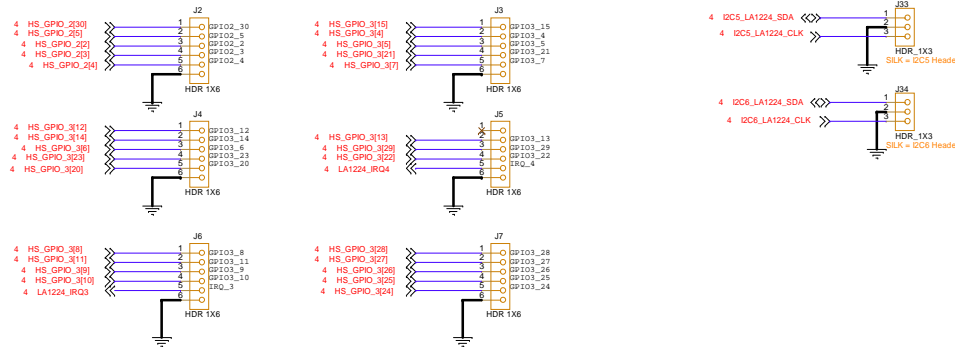
LLCP1 & SPI4/5 Headers



I2C Headers



GPIO Headers



Classification: Company Internal/Proprietary

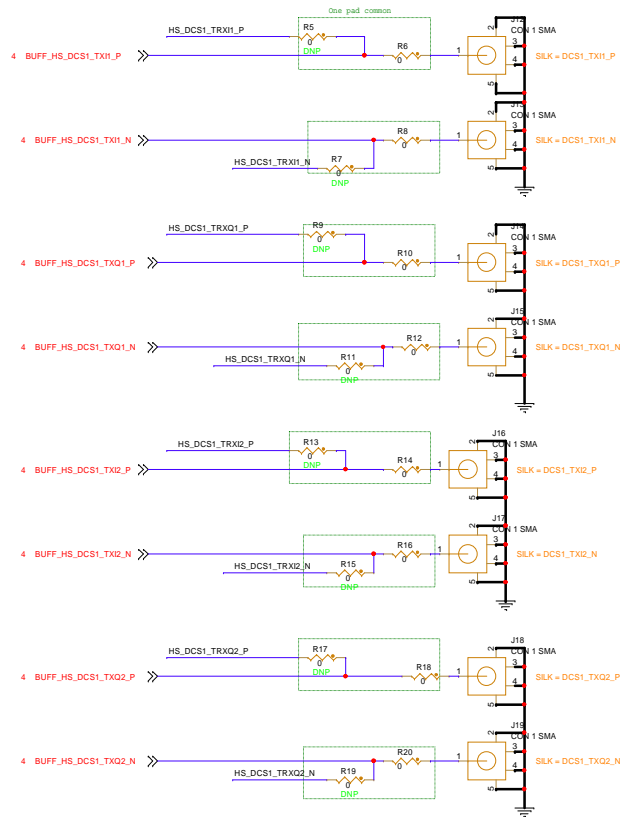
Drawing Title: X-LA1224-FR2-BRK

Page Title: CONNECTOR INTERFACE

Size: Document Number: SCH-54705 PDF: SPF-54705

Date: Thursday, February 03, 2022 Sheet: 4 of 6

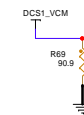
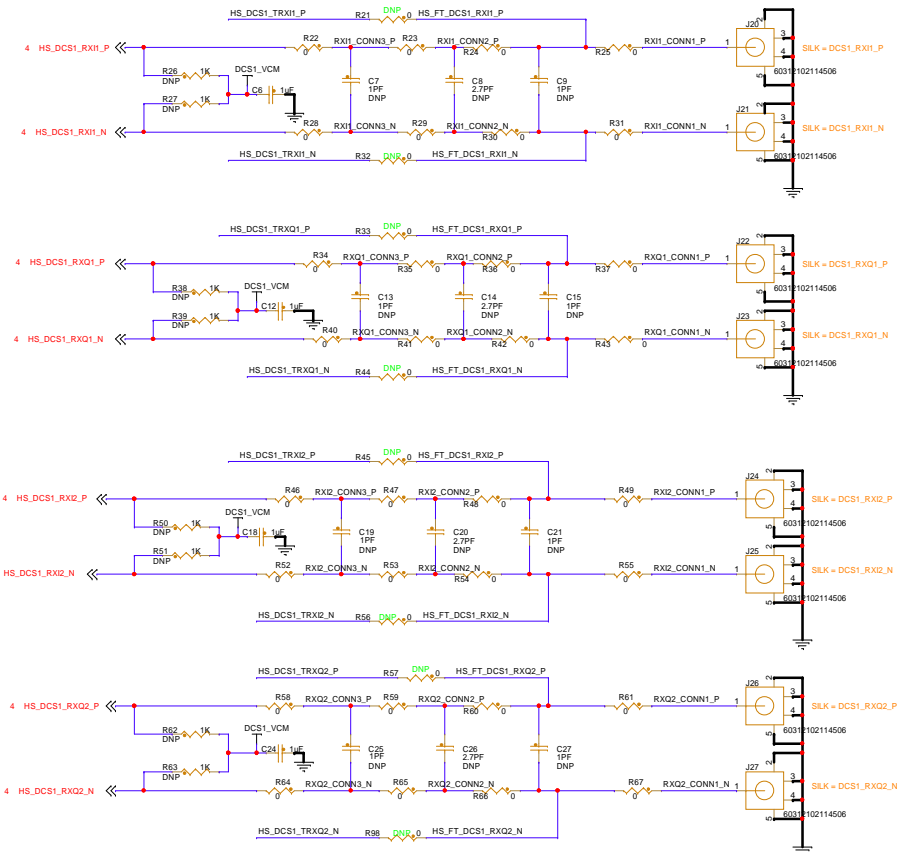
HS_DCS1 TX & RX SMA PORTs



Layout Comment:

Make the below pair of resistors one pad common:

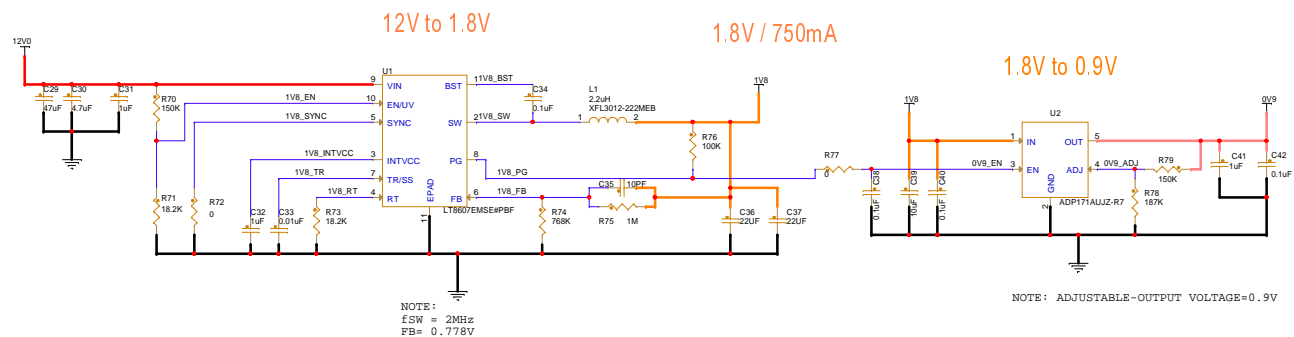
R21 - R25, R31 - R32, R33 - R37, R43 - R44,
R45 - R49, R55 - R56, R57 - R61, R67 - R68,
R5 - R6, R7 - R8, R9 - R10, R11 - R12,
R13 - R14, R15 - R16, R17 - R18, R19 - R20



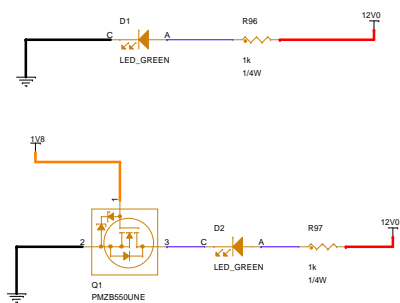
DCS1_VCM = 0.4V

NXP			
Classification: Public, Company Internal/Proprietary, Company Confidential, Company Secret			
Drawing Title: X-LA1224-FR2-BRK			
Page Title: HS_DCS1 TX & RX SMA PORTS			
Size C	Document Number SCH-64705 PDF: SPF-64705	Rev A	
Date: Thursday, February 03, 2022 Sheet 5 of 6			

POWER SUPPLY



LEDs



Classification: Public, Company Internal/Proprietary, Company Confidential, Company Secret			
Drawing Title: X-LA1224-FR2-BRK			
Page Title: POWER SUPPLY			
Size: C	Document Number: SCH-54705 PDF: SPF-54705	Rev: A	
Date: Thursday, February 03, 2022	Sheet: 6	of 6	