

# MCIMX91 9x9 package Quick Start Board

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## Revision History

## IMX91LP4QSB-09

Rev. Code	Date	By	Description
A	2024-01-12	NXF91318	Initial version
A1	2024-08-23	NXF91318	1. Change C102 from 0.22uF to 1uF for better noise suppression. 2. Change U2 LPDDR4 to NANYA NT6AN512M16AV-J11, as the old part will be EOL soon. 3. Change D18, D19 to BAT54HT1 for lower reverse current to reduce power leakage from VLS_3V3 to DCDC_5V. 4. Change U36 to MCP6546 to reduce power leakage from comparator input to power supply VDD_5V. 5. Change R299 from 249K to 226K to decrease the threshold of comparator input for VBUS detect. 6. Change C154 to 100uF, C200 to 47uF to improve the transient response of SYS_5V, when load switch U58 is enabled. 7. DNP R331 to avoid voltage conflict of CCM_CLKO1 between internal pull-up VDD_1V8 and external pull-up VDD_3V3. 8. Update U23 PF9453AHN symbol.
A2	2024-08-26	NXF91318	1. Update Title Block with new NXP logo.
A3	2025-04-16	NXF91318	1. Update U1 part number from MIMX9111CVXXJAA to MIMX9111CVXXJAB. 2. Update U23 part number from PF9453AHN to MPF9453AVMA1HN. 3. Update U23 BUCK2 output current from 2A to 2.7A.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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NXP SE

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NXP SE

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SCH-90934 PDF: SPF-90934

Rev  
A3

Date:  
Wednesday, April 16, 2025

Sheet  
1

of  
24

The diagram illustrates the NXP i.MX91 SoC and its various peripheral connections. The central component is the **NXP i.MX91** SoC, which includes an **ARM: CORTEX-A55 (1.4GHz) 9x9 Package**.

**Power and System Management:**

- PMIC NXP PF9453** is connected to **SYS PWR** (red arrow) and provides power to the SoC.
- Curr Sense PAC1934** is connected to the PMIC and the SoC.
- FTDI FT4232** is connected to the SoC.

**Storage and Memory:**

- DRAM LPDDR4: 1GB x16b** is connected to the SoC via **x16 bits**.
- eMMC 5.1 16GB HS400** is connected to the SoC via **x8 bits**.
- MicroSD SD3.0** is connected to the SoC via **x4 bits**.

**Real-time and Sensor Interfacing:**

- RTC NXP PCF2131** is connected to the SoC via **I2C1**.
- TEMP NXP P3T1085** is connected to the SoC via **I3C/I2C1**.
- ADC 2CH x12 bit** is connected to the SoC via **ADC**.
- AUX I2C I2C/GPIO** is connected to the SoC via **I2C1**.

**Communication and I/O:**

- SAI1** is connected to the SoC.
- UART5** is connected to the SoC.
- SDHC3** is connected to the SoC.
- USB1** is connected to the SoC via **USB 2.0 DRP**.
- Giga ENET Realtek RTL8211** is connected to the SoC via **RGMII**.
- UART-USB FTDI FT4232** is connected to the SoC via **UART1**.
- CAN NXP TJA1051T/3** is connected to the SoC via **CAN**.
- PDM** is connected to the SoC.
- IO Expander NXP PCAL6524** is connected to the SoC via **I2C2**.

**External Components and Interfaces:**

- DAC Cirrus Logic WM8524** is connected to the SoC via **SAI1** and provides **Line OUT**.
- M.2 NGFF KEY-E: WIFI/BT...** is connected to the SoC via **SAI1** and provides **WIFI/BT** connectivity.
- QSPI Nand GD GD5F2GM7RE** is connected to the SoC via **SDHC3**.
- TYPE-C connector** is connected to the SoC via **USB1**.
- Realtek RTL8211** is connected to the SoC via **Giga ENET**.
- UART-USB FTDI FT4232** is connected to the SoC via **UART1**.
- CAN NXP TJA1051T/3** is connected to the SoC via **CAN**.
- PDM** is connected to the SoC.
- IO Expander NXP PCAL6524** is connected to the SoC via **I2C2**.

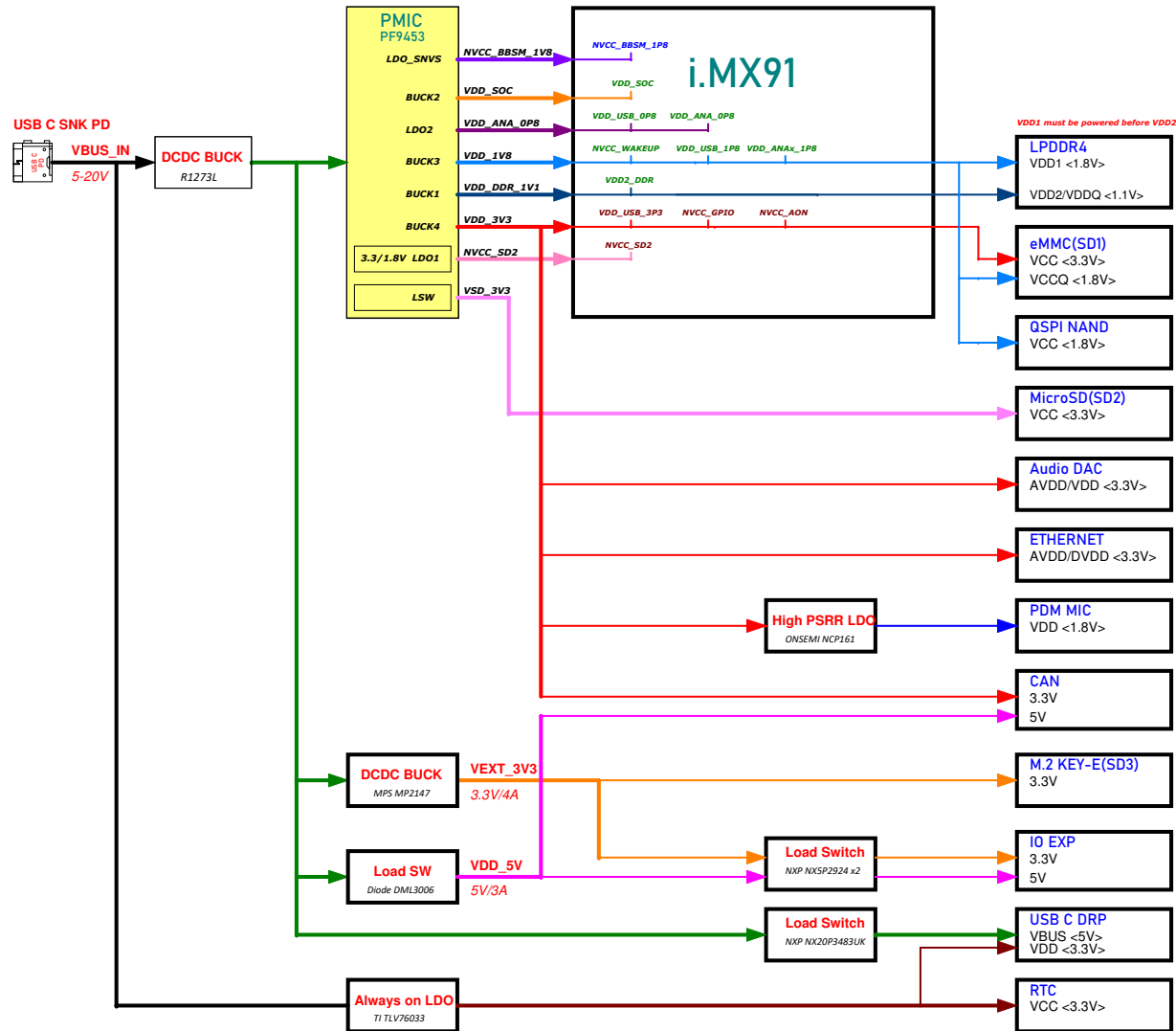
**Debug and Expansion:**

- JTAG/SWD DEBUG** is connected to the SoC via **JTAG/SWD**.
- EXP CN UART/I2C/SPI/PDM/ISI...** is connected to the SoC via **UART/I2C/SPI/PDM/ISI...**.

**Other Features:**

- ARM: CORTEX-A55 (1.4GHz) 9x9 Package** is the main processor.
- ARM: CORTEX-A55 (1.4GHz) 9x9 Package** is the main processor.
- ARM: CORTEX-A55 (1.4GHz) 9x9 Package** is the main processor.

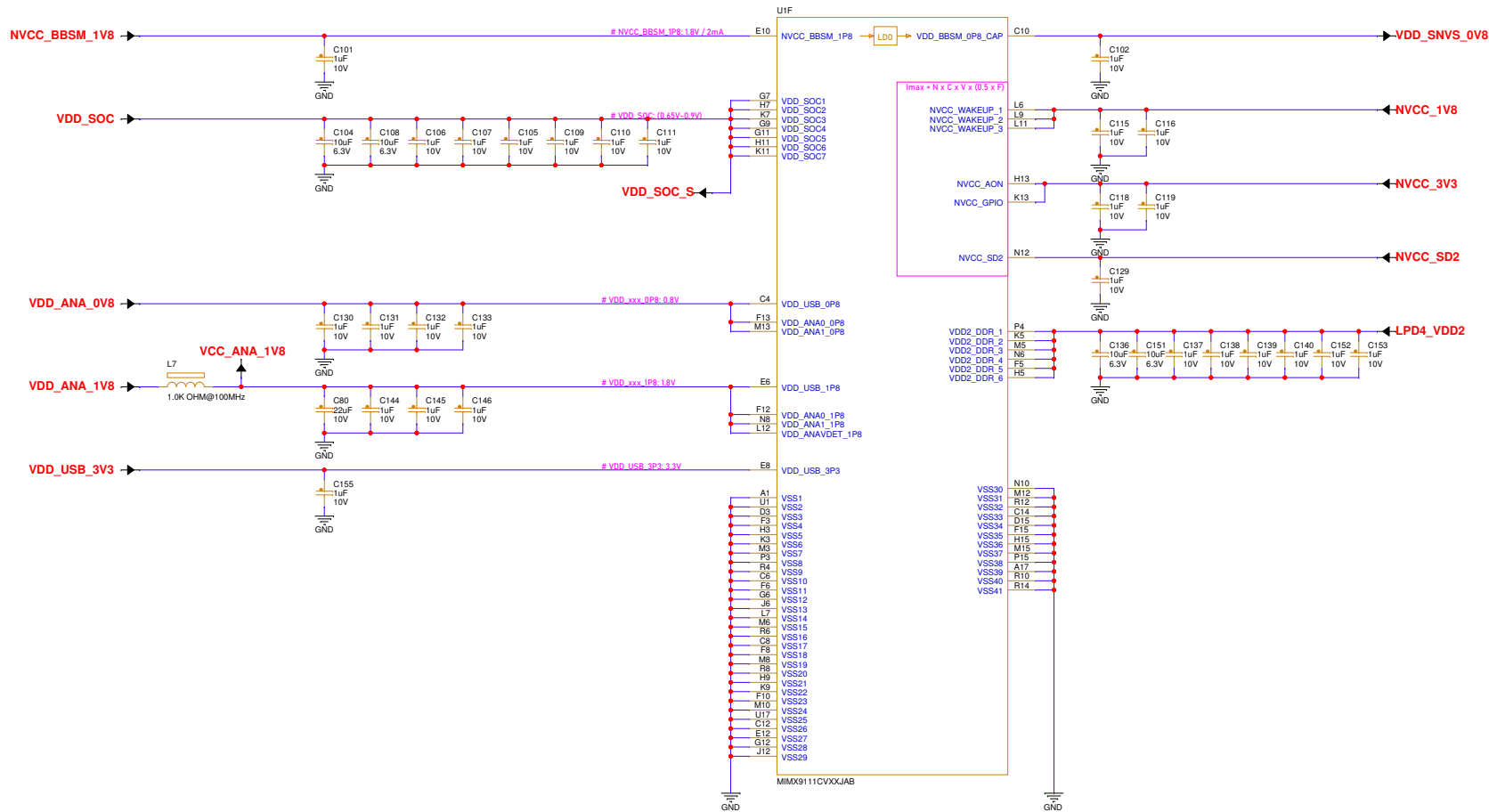
# i.MX 91 9x9 QSB PWR TREE



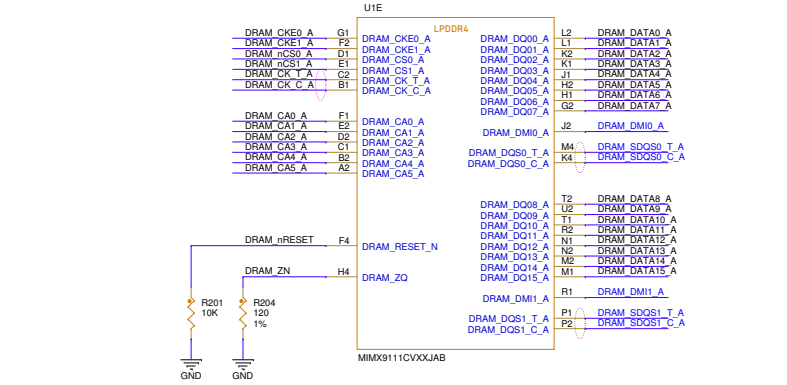
## PMIC: PF9453 CFG

SEQ	Tstep	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	RANGE(V)	Req I (mA)
0		LDO_SNVs	1.8	10	NVCC_BBSM_1P8	1.65-1.8-1.95	2
1	T1	BUCK2	0.85	2700	VDD_SOC	0.61-0.65-0.69 0.76-0.8-0.84 0.8-0.85-0.9	1500
2	T2	LDO2	0.8	200	VDD_ANA_0P8 VDD_USB_0P8	0.76-0.8-0.9	200
3	T3	BUCK3	1.8	2000	VDD_ANAX_1P8 NVCC_WAKEUP VDD_USB_1P8 DDR_VDD1 VDD_1V8	1.71-1.8-1.89	2000
4	T4	BUCK1	1.1	2000	VDD2_DDR/LPD4_VDD2	1.06-1.1-1.14	1000
5	T5	BUCK4	3.3	2500	NVCC_AON NVCC_GPI0 VDD_USB_3P3 VDD_3V3	3.0-3.3-3.45	2500
6	T5	Load Switch	3.3	400	VSD_3V3	3.3	400
7	T6	LDO1	3.3/1.8	250	NVCC_SD2	3.3/1.8	150
8	Tpor_b	POR_B	--	--	POR_B	--	--

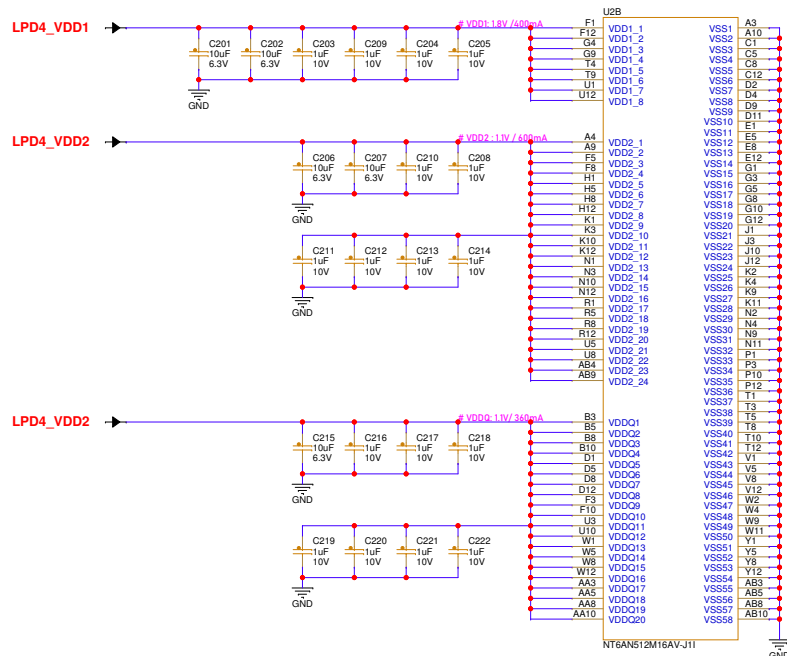
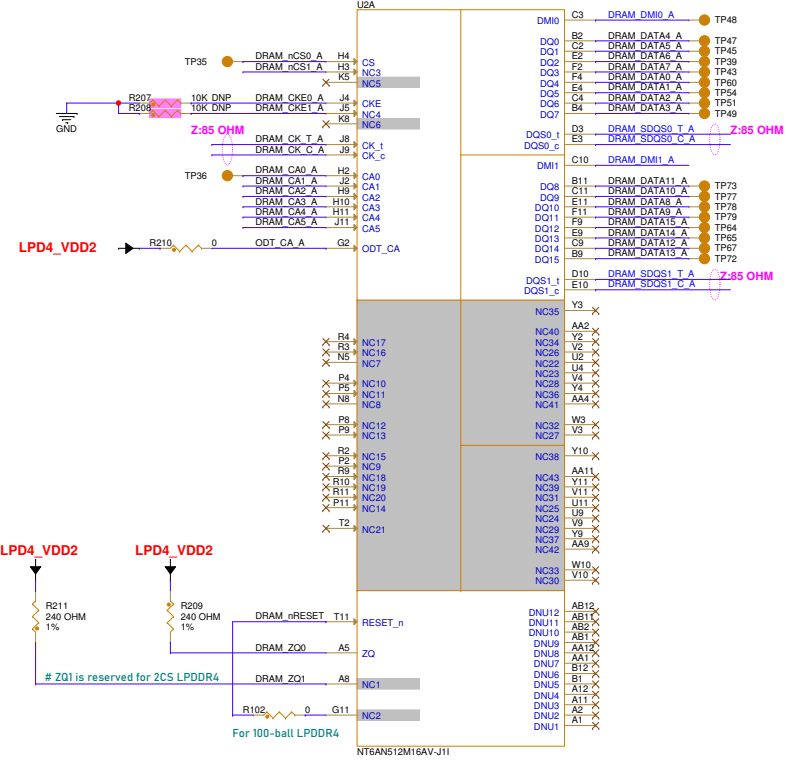
# i.MX91 PWR



16bit LPDDR4



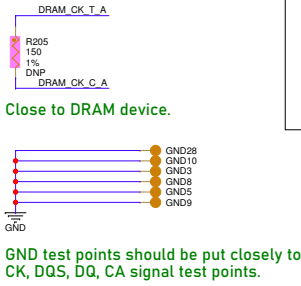
LPDDR4: 1GB (x16)



# Power Supply Voltage Sequence:

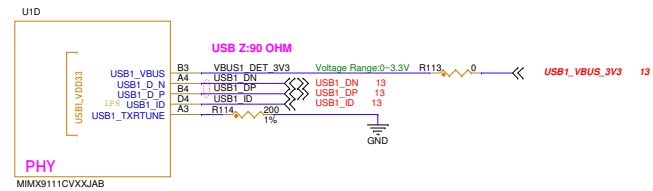
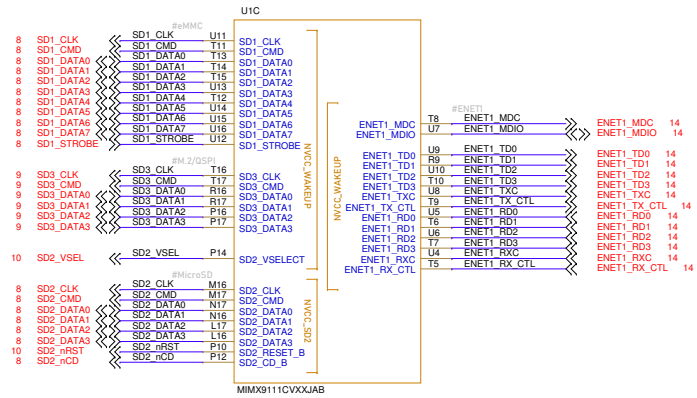
RESET\_n is held LOW.  
VDD1 >= VDD2  
VDD2 >= VDDQ-200mV

Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

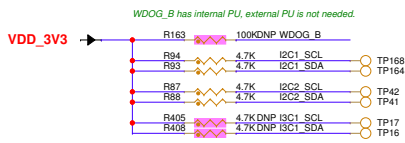
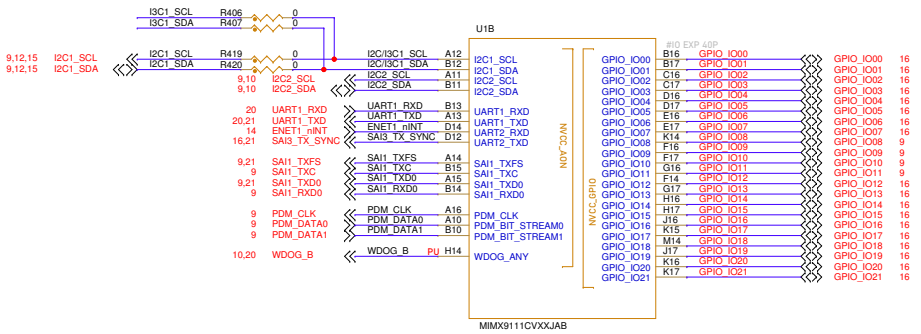


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Drawn by: NXP SE	Page Title: <b>LPDDR4</b>		
Approved: NXP SE	Size C	Document Number SCH-90934 PDF: SPF-90934	Rev A3
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CPU IO/PHY

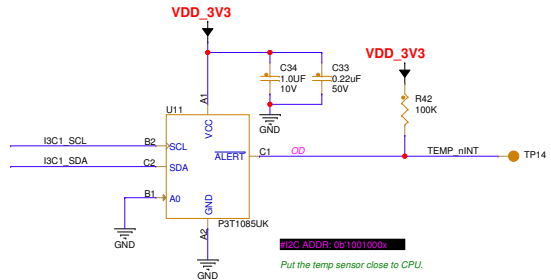


Note:  
If USB connector is MicroAB or MicroB, USBx\_VBUS MUST not be directly connected to the 5V VBUS of connector. Instead, this pin must be isolated with an external 30K 1% resistor.



External PU is necessary for SD2\_RESET\_B to enable SD card power as default!

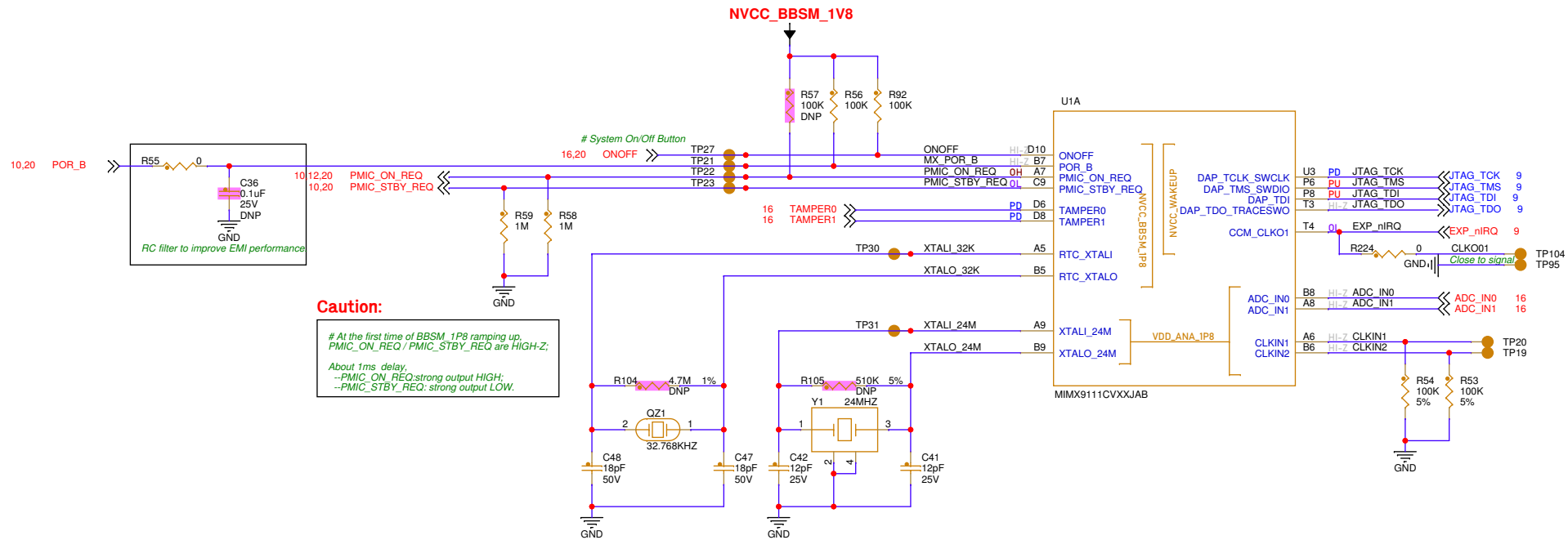
I3C TEMP SENSOR



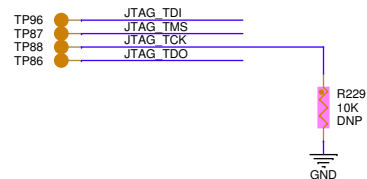
Note for using I3C:  
1. The total capacitance loading on the I3C bus must be less than 50 pF, including that of the PCB traces and I3C/I2C devices.  
2. The routing stubs on SCL/SDA traces should not exceed 1.5 inch, stubs will cause reflections and may lead to glitches on the signal edges.  
3. Strongly recommend to run SI simulation to check the signal quality of SDA and SCL, as the I3C signals have much faster edges than I2C.  
4. Avoid using level shifter for I3C devices, improper level shifter might cause the bus malfunction. If the level shifter can't be avoided, must choose the part without one-shot circuit, such as LSF0504.  
5. SCL Rise/Fall Time should be less than 60ns, IO drive strength can be adjusted to achieve this.  
6. For I3C application, external pull-up resistors on SCL and SDA are not needed, the I3C controller is equipped with internal pull-up resistors.  
7. It is recommended that only I3C devices are connected to the I3C bus. If both I3C and I2C devices are connected to the bus, make sure that the I2C devices are equipped with 50ns Spike Filter, otherwise the I3C bus max frequency will be limited to FM(400KHz)/FM+(1MHz).


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# i.MX91 MISC



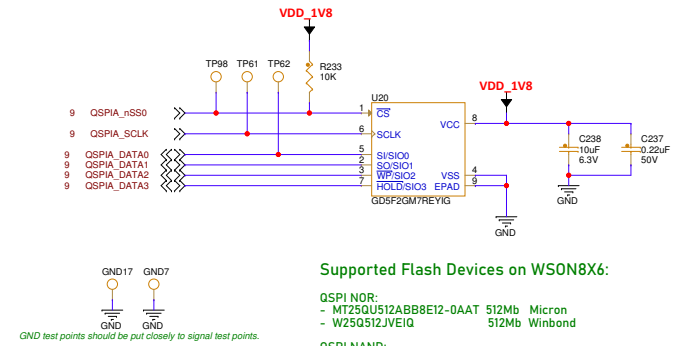
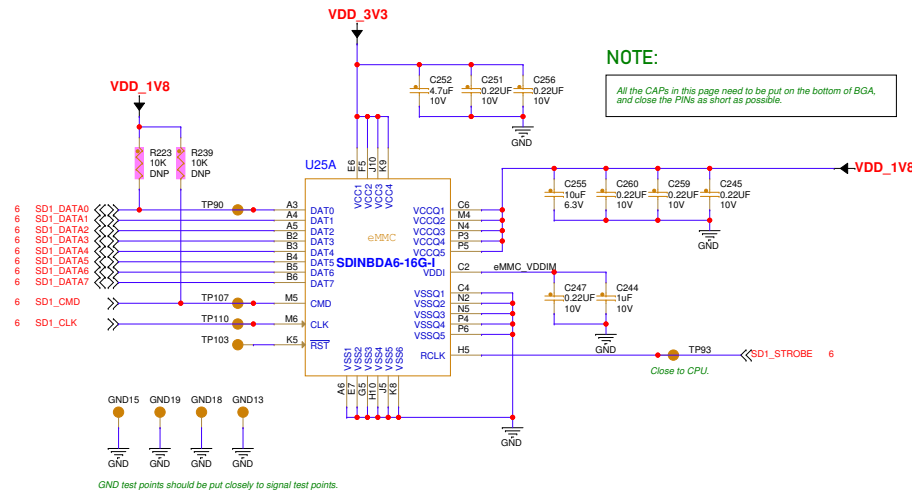
## JTAG/SWD



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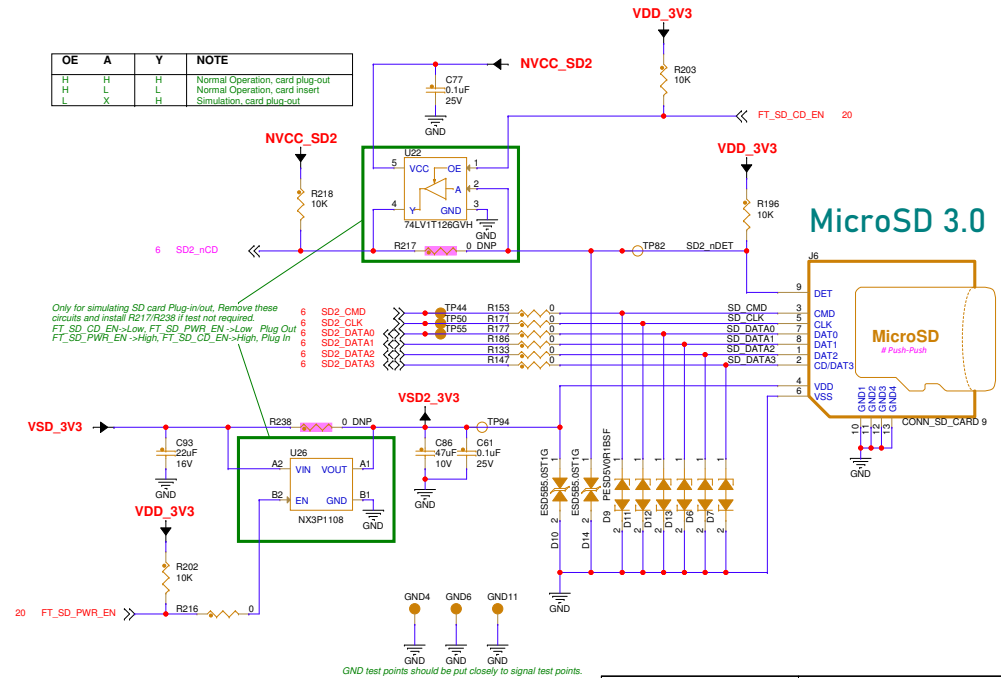
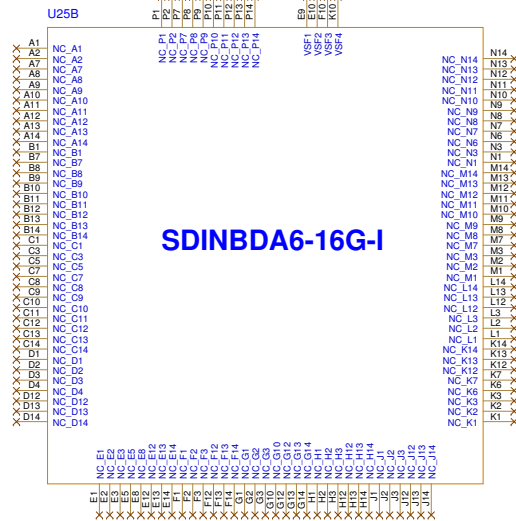
# FLASH: 16GB eMMC 5.1


# QSPI Flash on SDHC3



## Supported Flash Devices on WSON8X6:

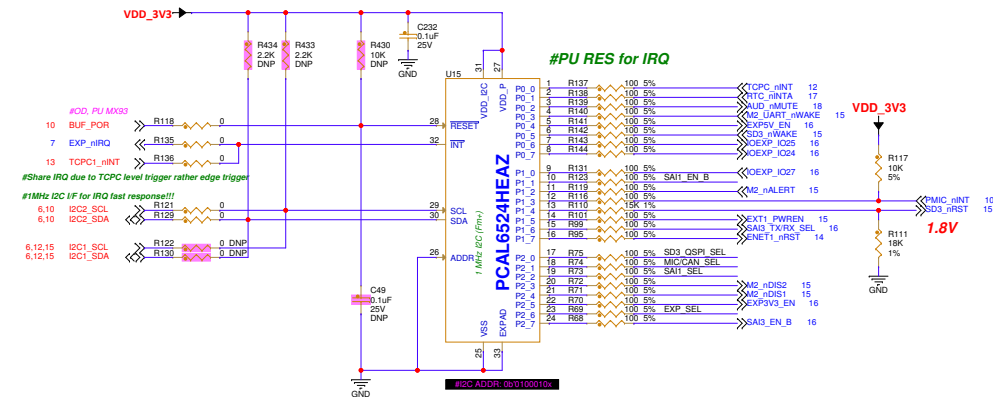
- QSPI NOR:**  
- MT25QU512ABB8E12-0AAT 512Mb Micron  
- W25Q512JVE1Q 512Mb Winbond
- QSPI NAND:**  
- GD5F2GM7REYIG 2Gb GigaDevice  
- W25N02KWZIER 2Gb Winbond



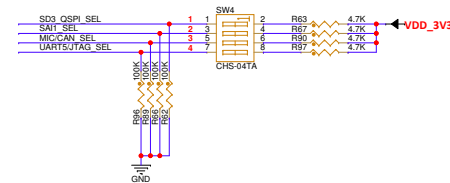
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Drawn by: NXP SE	<b>Page Title:</b>  <b>eMMC/MicroSD/QSPI</b>		
Approved: NXP SE	Size C	Document Number SCH-90934 PDF: SPF-90934	Rev A3
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## IO MUX / EXP



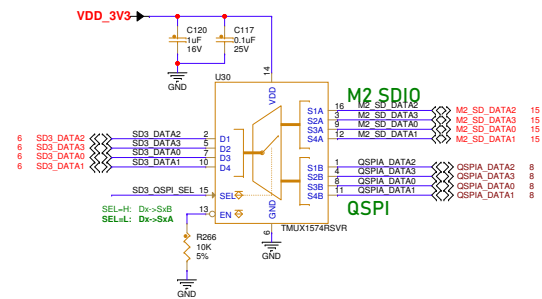
## Function Switch



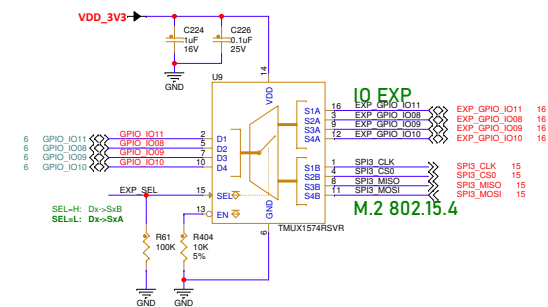
### Switch Setting Table

Signal	Setting	Description
SD3_QSPI_SEL	0	Default Low, SDIO for M.2
SW4 [1]	1	High, QSPI Flash
SA1I_SEL	0	Default Low, SA1I for Audio DAC
SW4 [2]	1	High, SA1I for M.2 Bluetooth
MIC/CAN_SEL	0	Default Low, PDM MIC
SW4 [3]	1	High, CAN1
UART5/JTAG_SEL	0	Default Low, UART5 for M.2 Bluetooth
SW4 [4]	1	High, JTAG debug

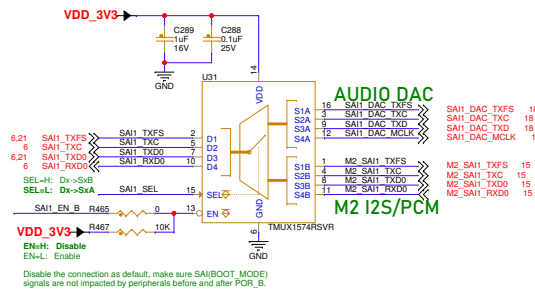
## M2 SDIO/QSPI Switch



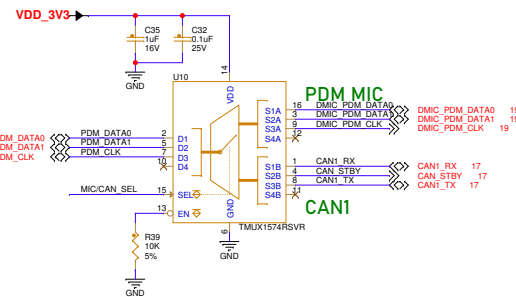
## SHARED GPIO MUX



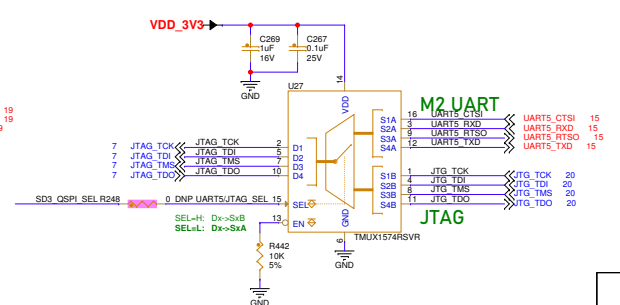
## AUDIO DAC/M2 Bluetooth Switch



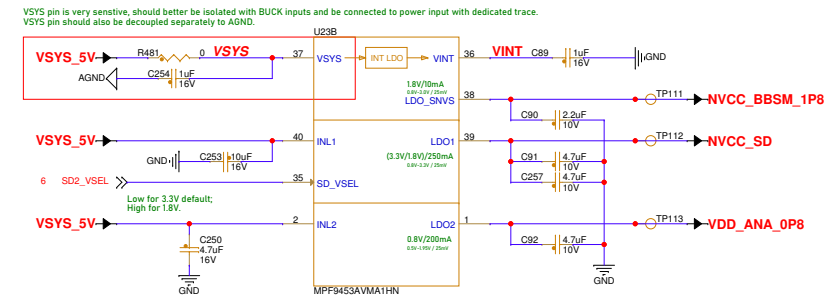
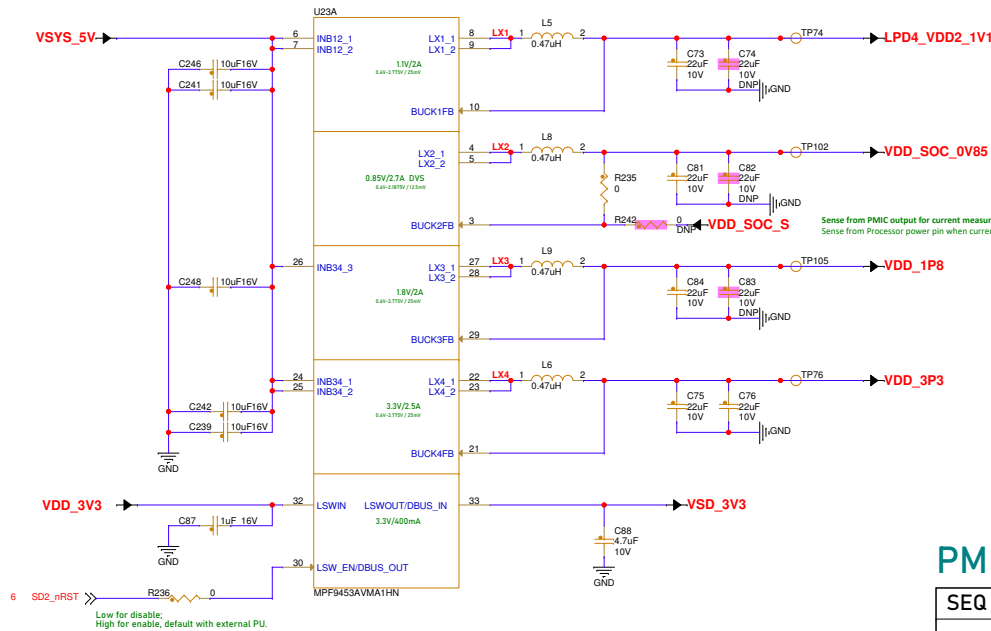
## PDM MIC/CAN Switch



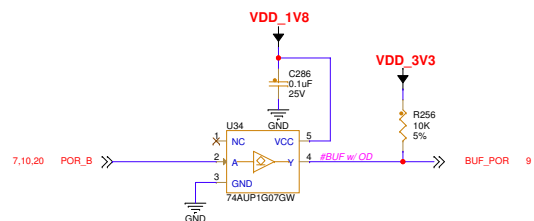
## M2 UART/JTAG Switch



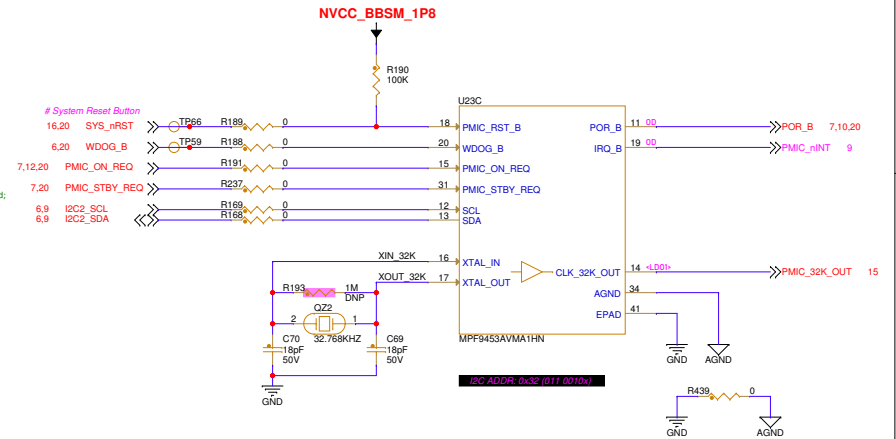
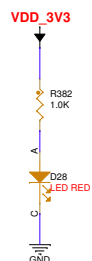
# SYS PMIC



## POR\_B Buffer



## PWR LED



Note:  
1. PMIC\_RST\_B is used as Cold Reset as default.  
2. WDOG\_B is used as Cold Reset, external pull up is needed for BSDL mode.  
3. AGND is sensitive, should be separated from GND(EPAD), don't short them directly.

## PMIC: PF9453 CFG

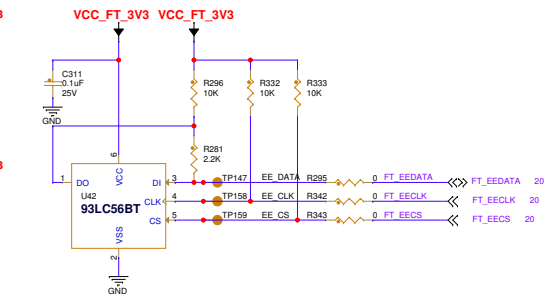
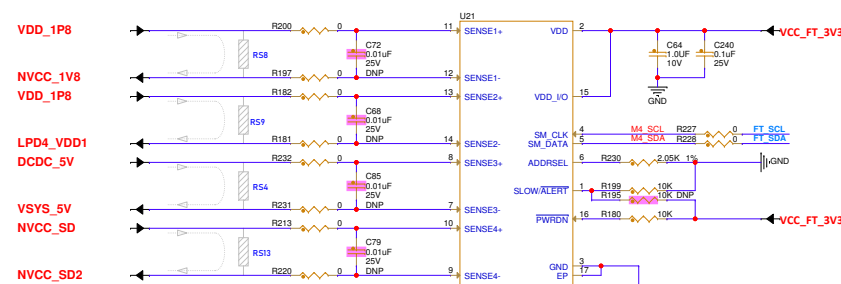
SEQ	Tstep	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	RANGE(V)	Req I (mA)
0		LDO_SNVS	1.8	10	NVCC_BBSM_1P8	1.65-1.8-1.95	2
1	T1	BUCK2	0.85	2700	VDD_SOC	0.61-0.65-0.69 0.76-0.8-0.84 0.8-0.85-0.9	1500
2	T2	LD02	0.8	200	VDD_ANA_0P8 VDD_USB_0P8	0.76-0.8-0.9	200
3	T3	BUCK3	1.8	2000	VDD_ANAx_1P8 NVCC_WAKEUP VDD_USB_1P8 DDR_VDD1 VDD_1V8	1.71-1.8-1.89	2000
4	T4	BUCK1	1.1	2000	VDD2_DDR/LPD4_VDD2	1.06-1.1-1.14	1000
5	T5	BUCK4	3.3	2500	NVCC_AON NVCC_GPIO VDD_USB_3P3 VDD_3V3	3.0-3.3-3.45	2500
6	T5	Load Switch	3.3	400	VSD_3V3	3.3	400
7	T6	LD01	3.3/1.8	250	NVCC_SD2	3.3/1.8	150
8	Tpor_b	POR_B	--	--	POR_B	--	--

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## Curr Monitors


## FT4232 I2C Address Table

## Always-on LDO for Ld SW

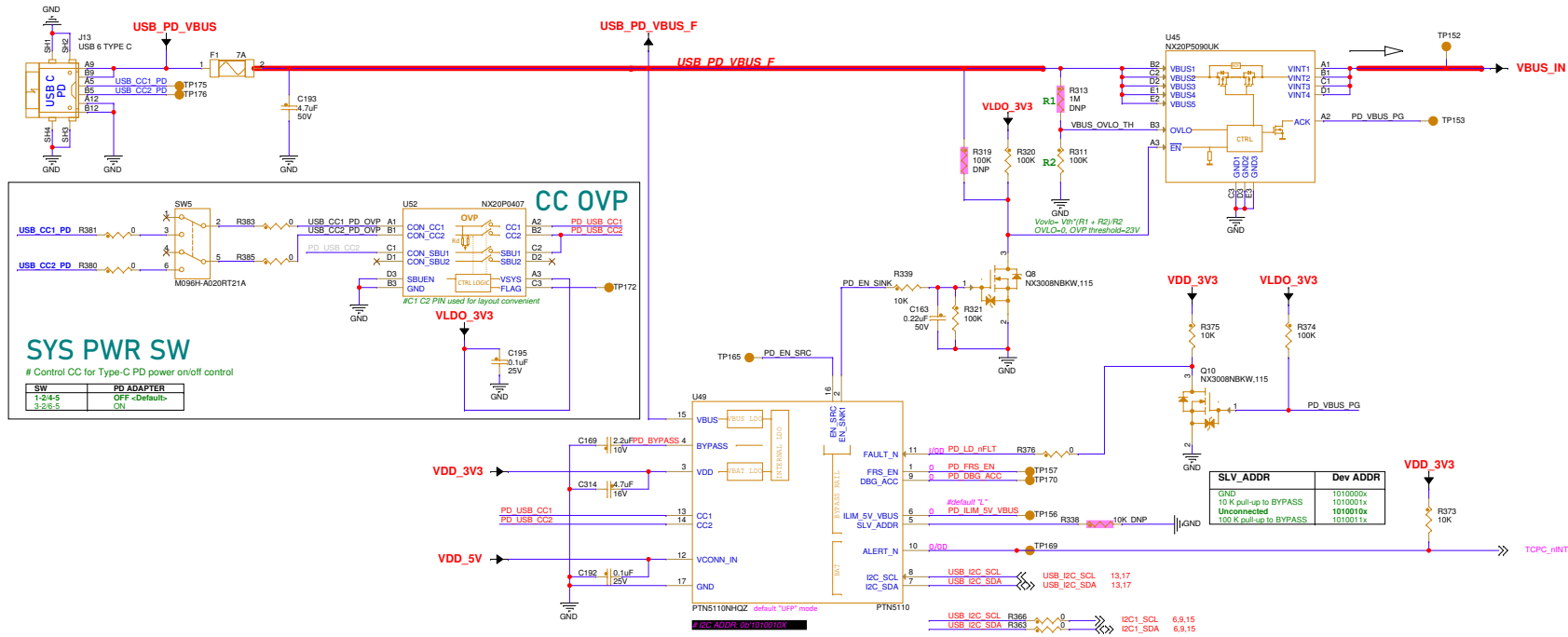


## Power Measurement Equations:

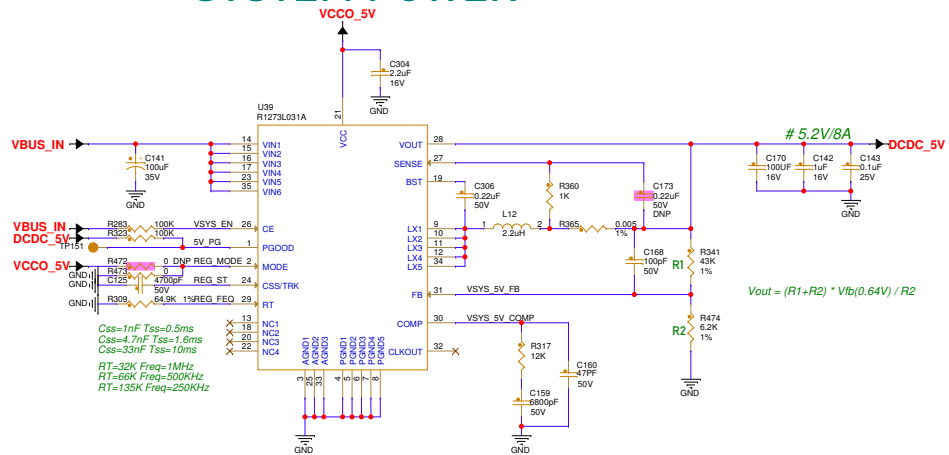
$$\begin{aligned} I_{\text{sense}} &= V_{\text{sense}} / R_s \\ V_{\text{out}} &= V_{\text{sense-}} = V(\text{sense+}) - V_{\text{sense}} \\ \text{Power} &= I_{\text{sense}} \times V_{\text{out}} \end{aligned}$$

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Drawn by: NXP SE	Page Title: <b>PWR MEAS</b>		
Approved: NXP SE	Size A2	Document Number SCH 90534 PDF: SPF-90534	Rev A3
Date: <b>Friday, May 09, 2025</b>		Sheet <b>11</b> of <b>24</b>	

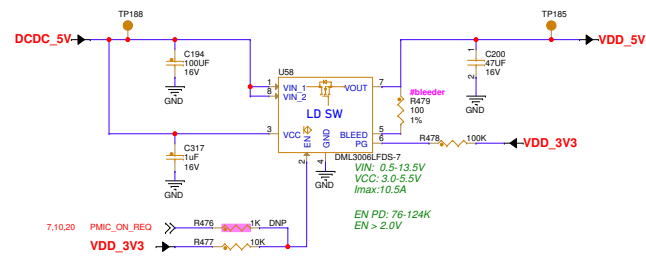
## USB TYPE-C PD



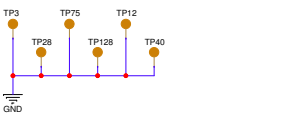
## SYSTEM POWER



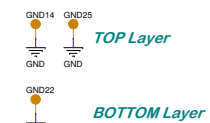
## PERIPHERAL POWER



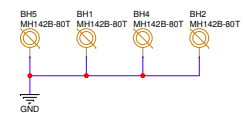
GND TP



## GND TESTLOOP

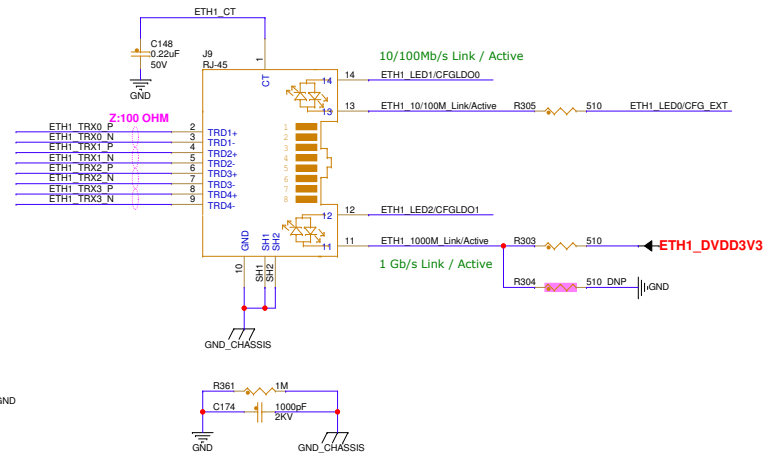
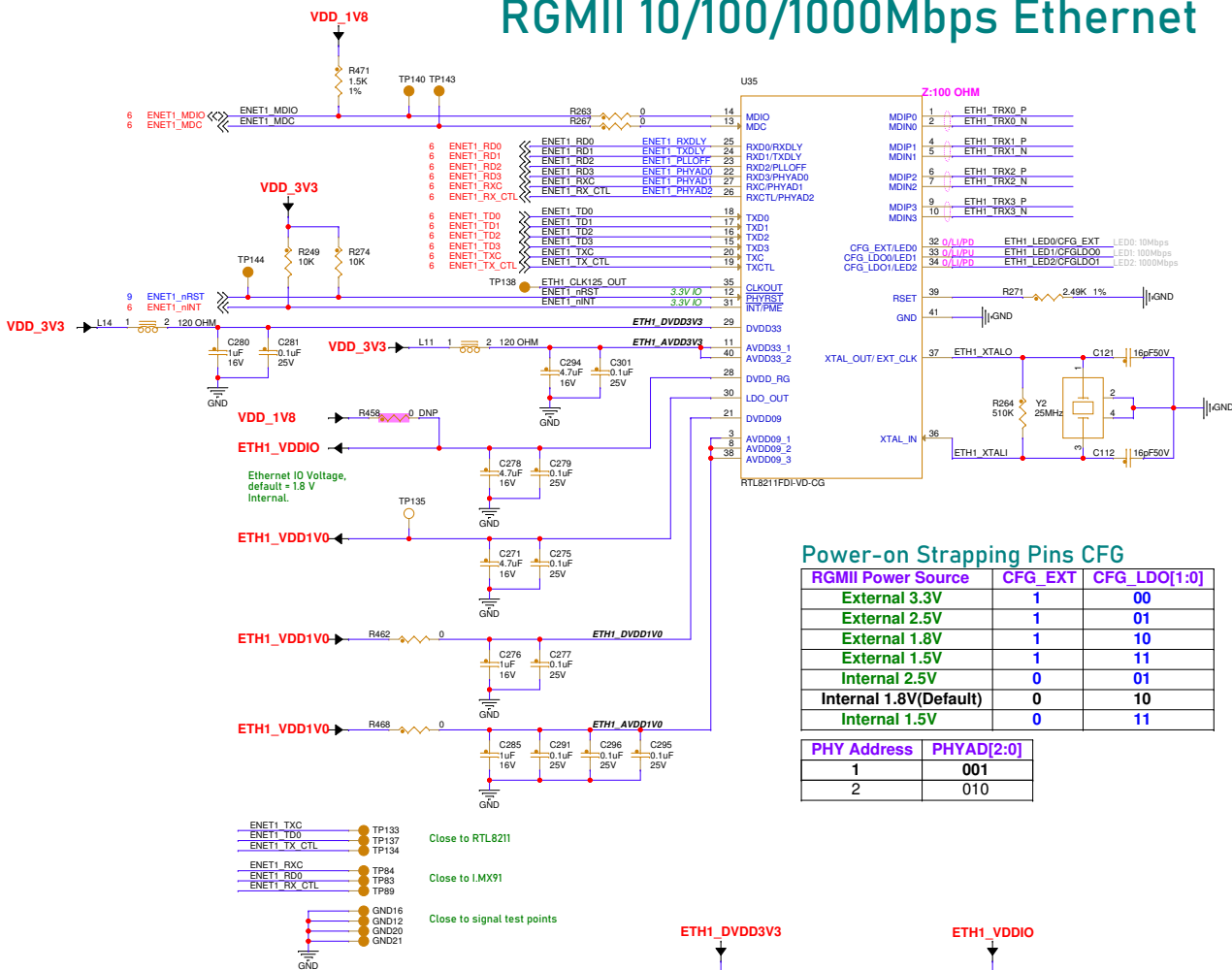


## SCREW HOLE





## RGMII 10/100/1000Mbps Ethernet

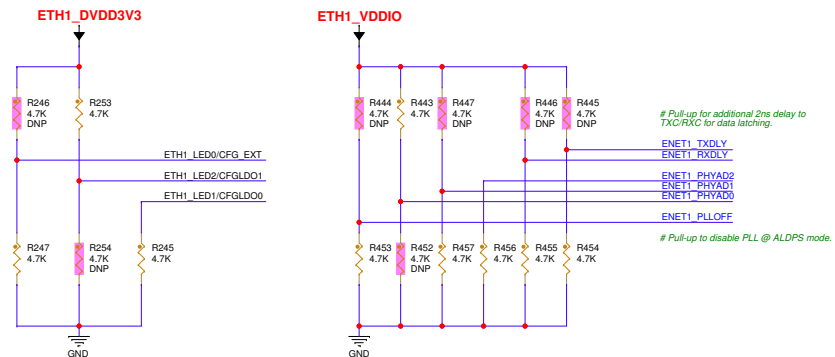
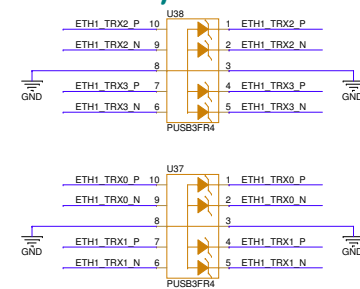


## Power-on Strapping Pins CFG

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

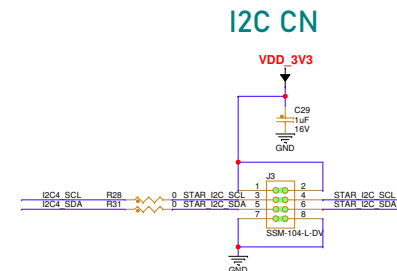
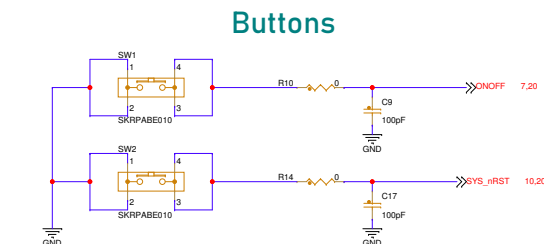
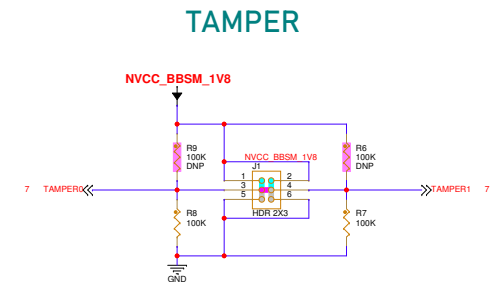
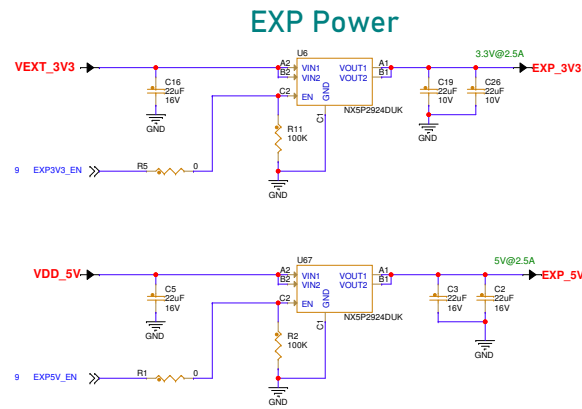
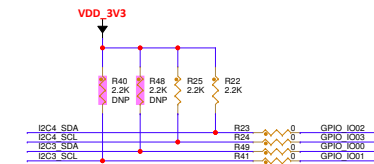
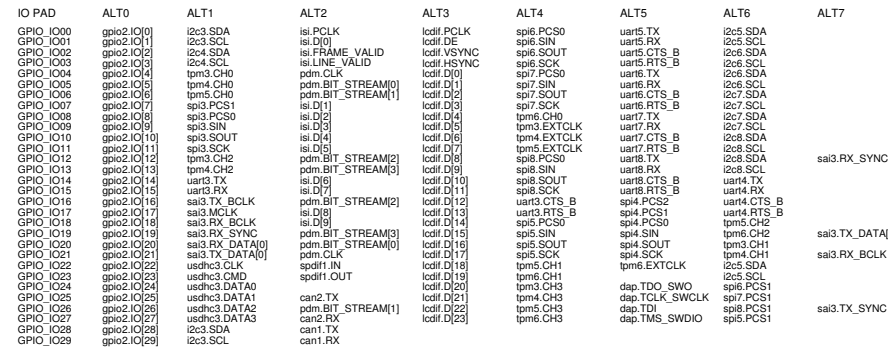
PHY Address	PHYAD[2:0]
1	001
2	010

## ESD protection



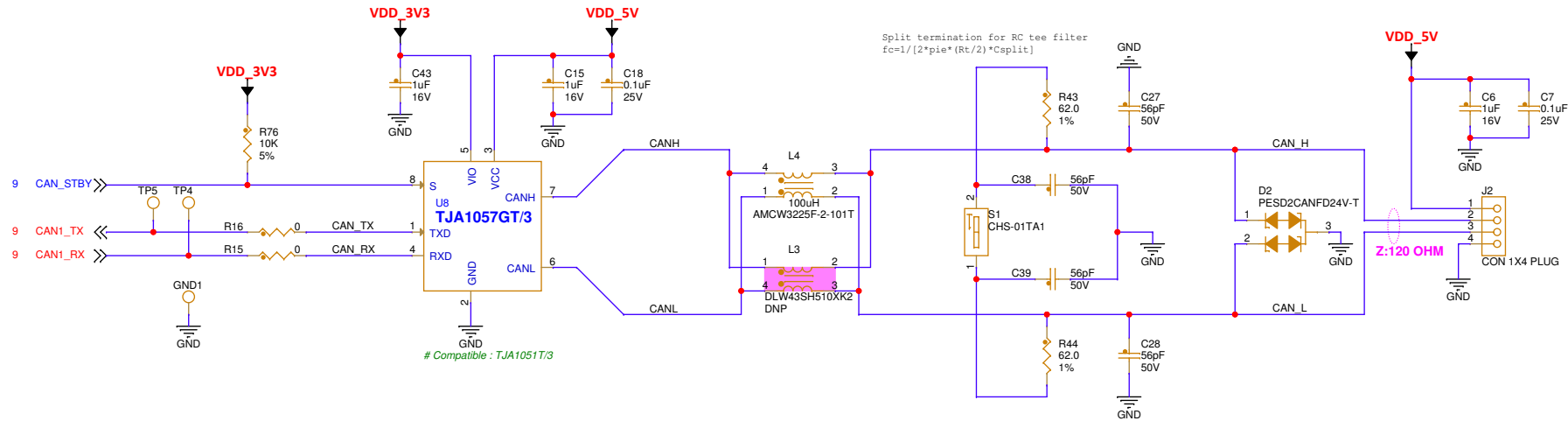




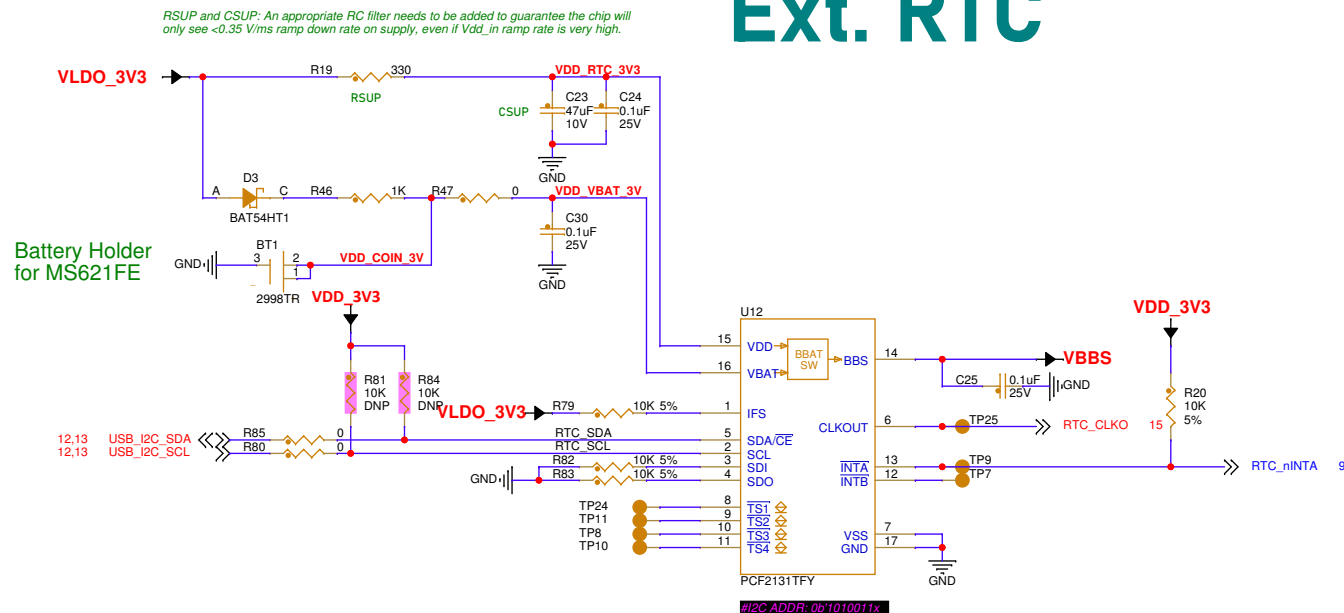





# CAN BUS



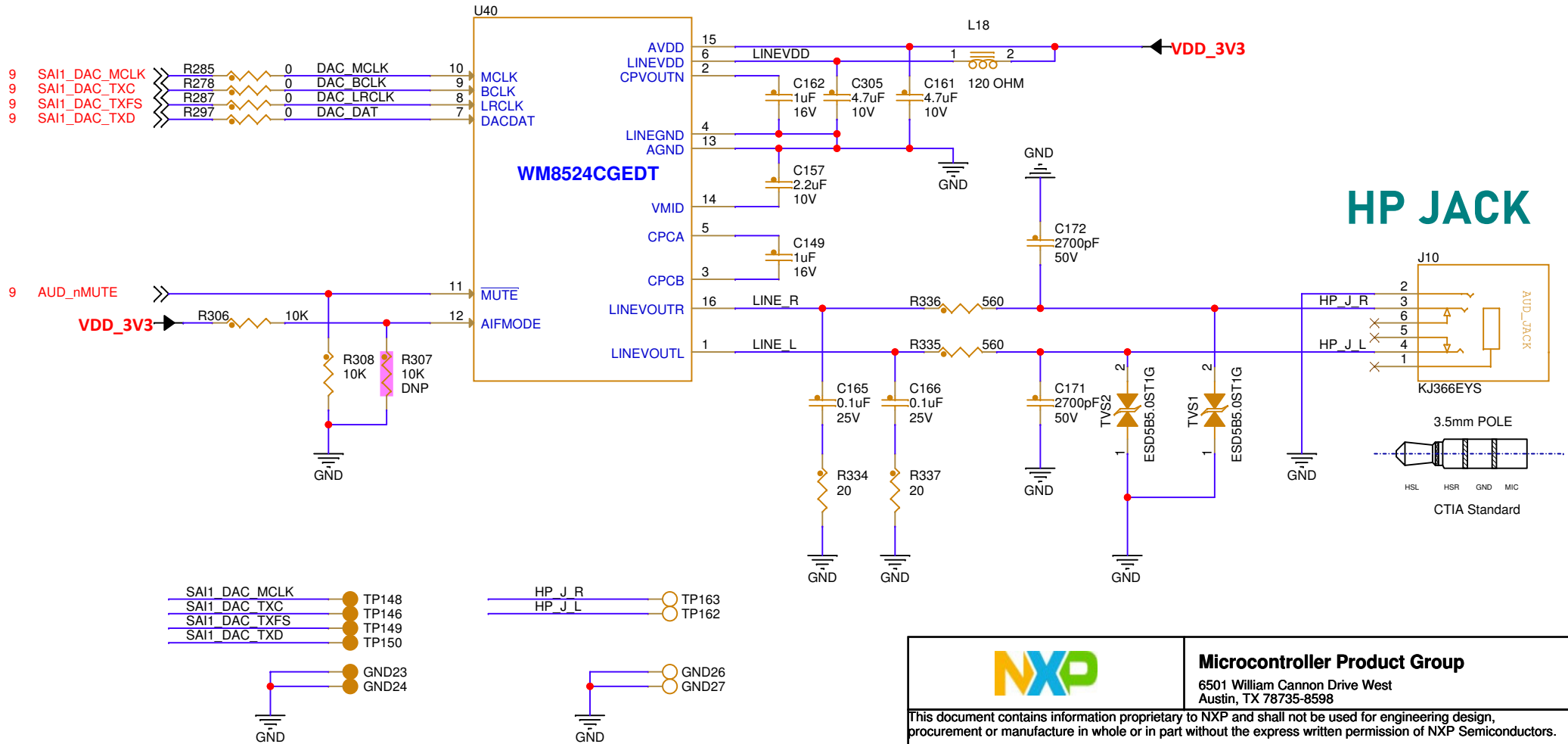
# Ext. RTC



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Drawn by: NXP SE	Page Title: <b>CAN BUS/External RTC</b>			
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Date: Friday, May 09, 2025		Sheet 17 of 24		

# AUDIO DAC

24-bit 192kHz Stereo DAC 2Vrms Line Out



## Microcontroller Product Group

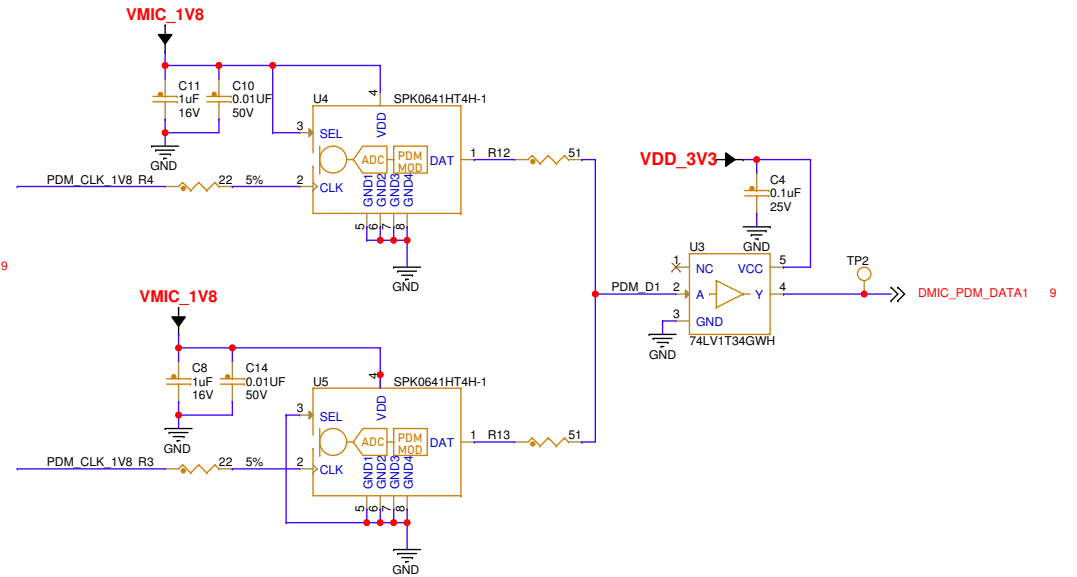
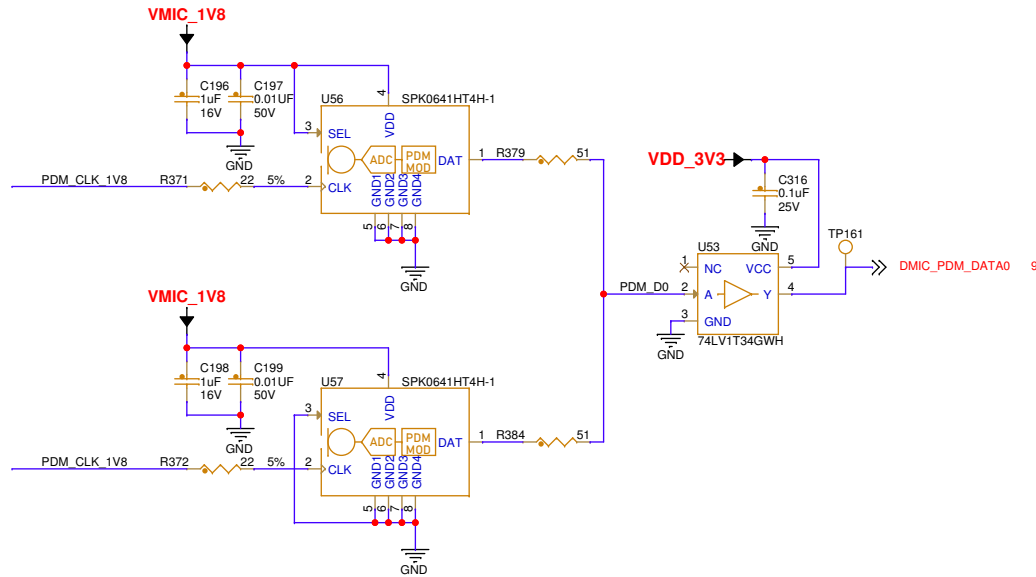
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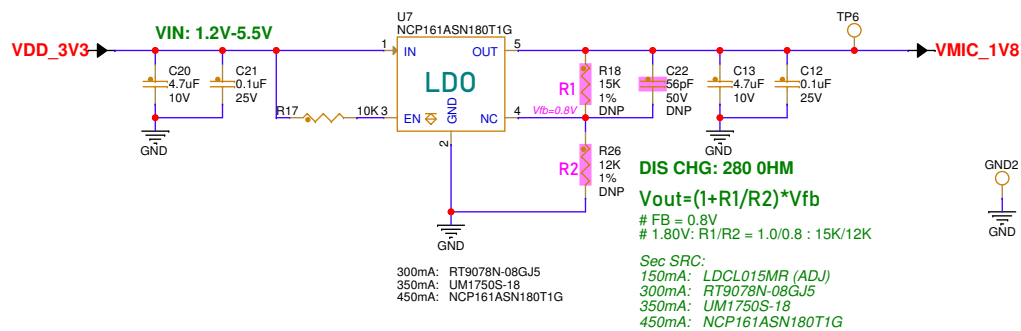
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Date:	Friday, May 09, 2025	Sheet 18 of 24	

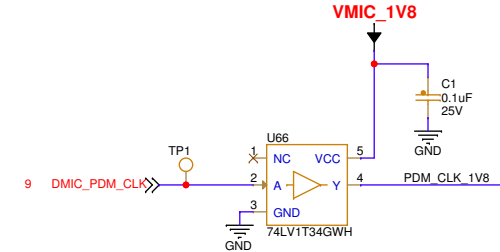
# PDM MIC




## LDO 1.8V for DMIC



## CLK Buffer

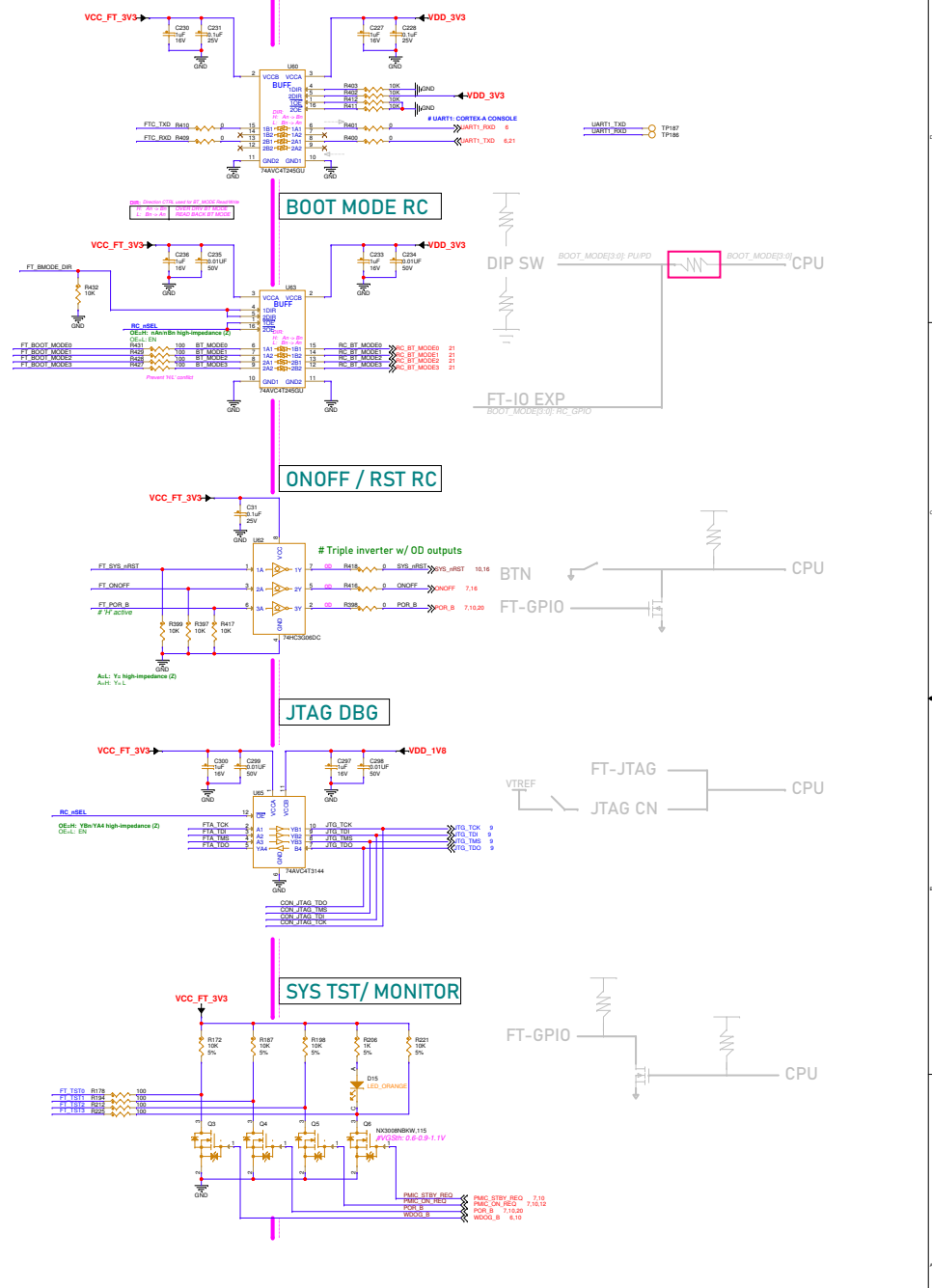
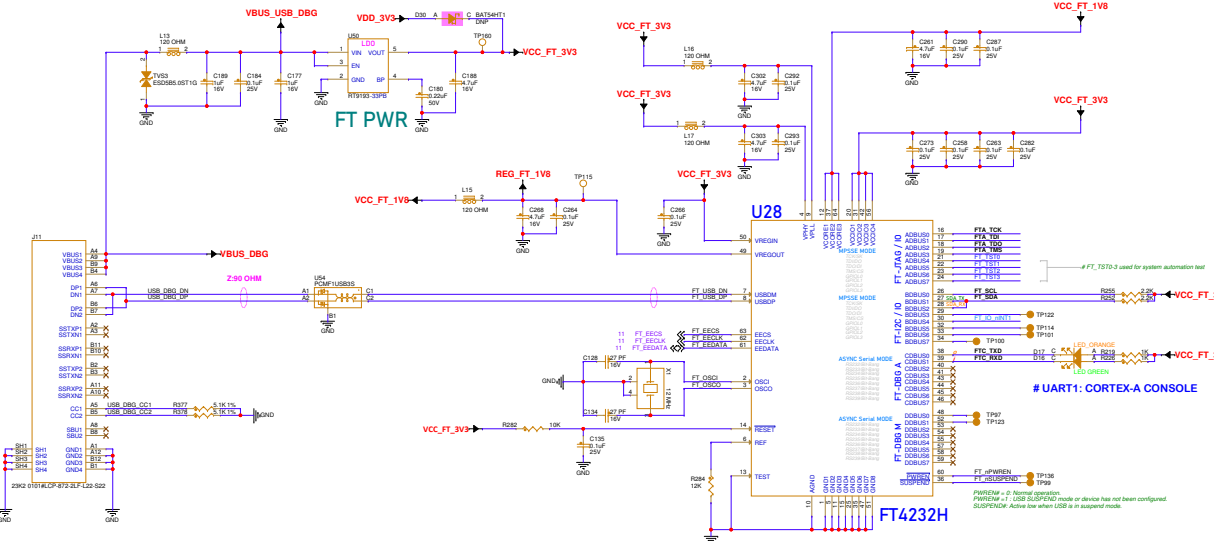


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REMOTE DEBUG

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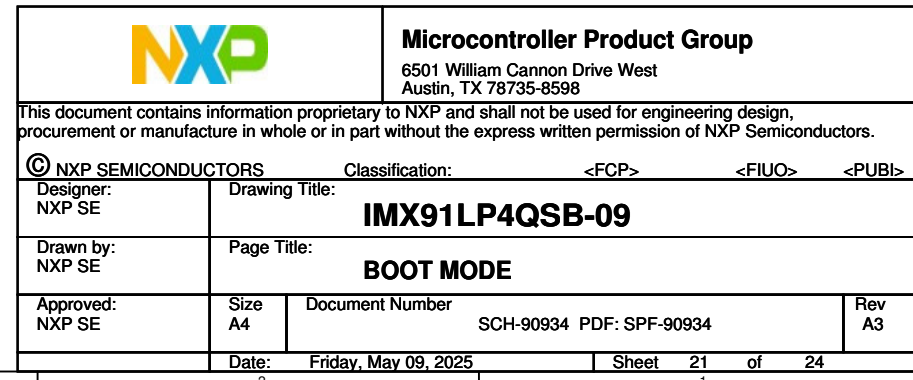
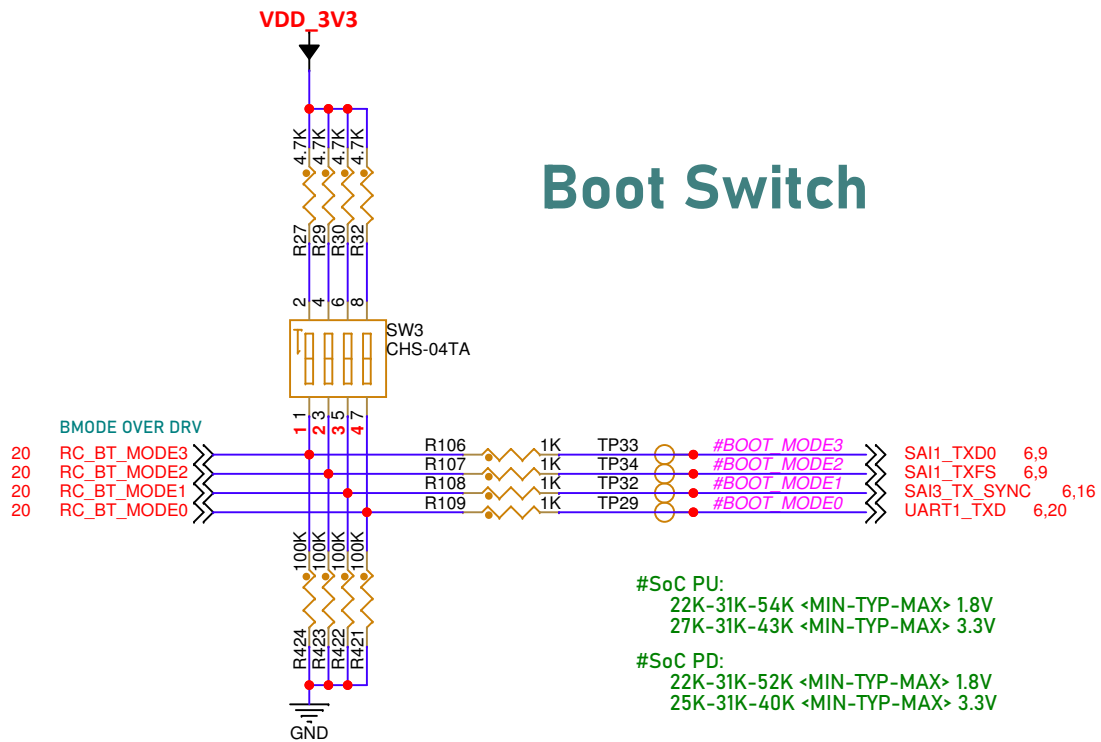
i.MX SoC RC I/F



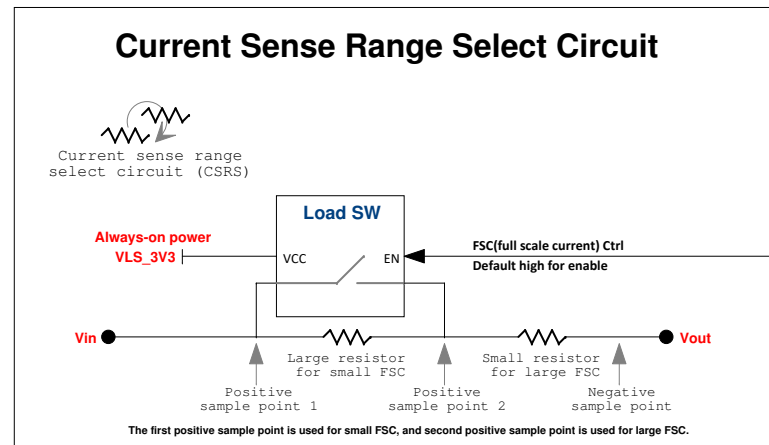
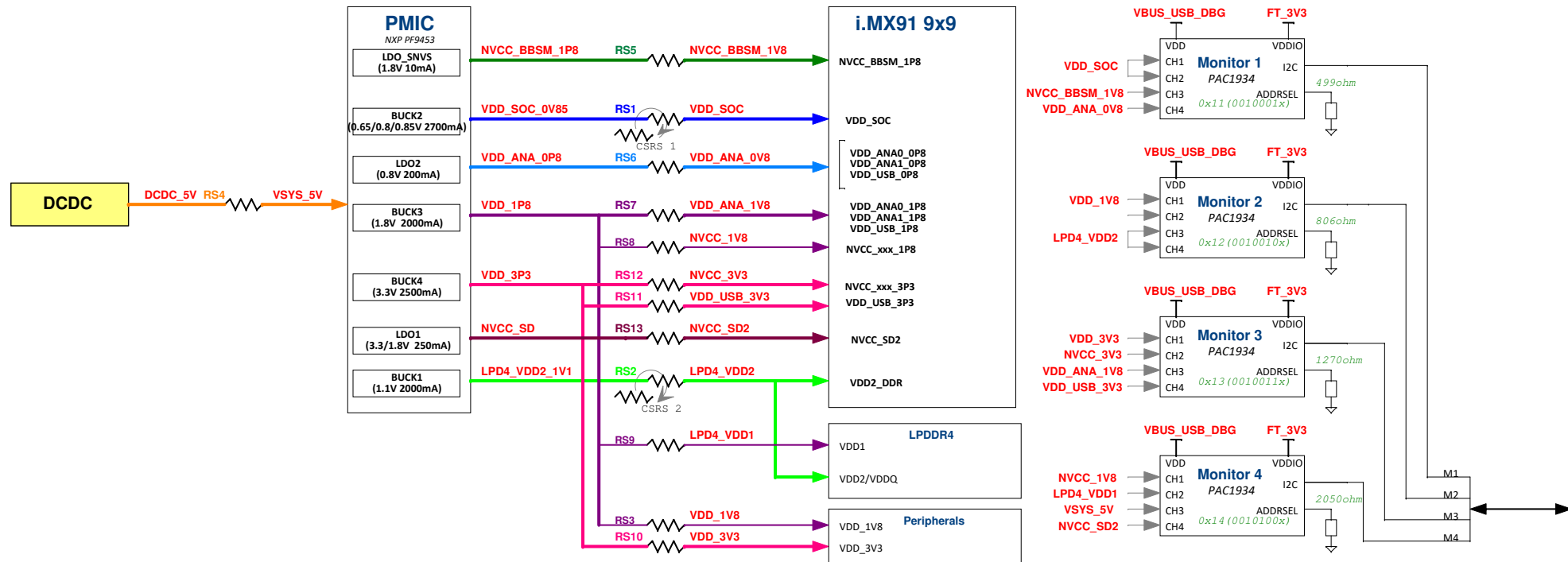
# BOOT MODE CFG

## i.MX91 BOOT MODE

BOOT_MODE[3:0] SW3[1:4]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	USB1
0001	Cortex-A55	Serial Downloader	
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	with SFDP (JESD-216) discoverable parameters
0011	Cortex-A55	USDHC2 4-bit SD3.0	
0100	Cortex-A55	FlexSPI Serial NOR	
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Reserved	
0111	Cortex-A55	Reserved	



# IMX91LP4QSB-09 Power Measurement Diagram



NOTE:

i.MX91 I2C DEV TABLE


PART	DEVICE	I2C ADDR	PORT	Max SPEED	VOL	DESCRIPTION
U15	PCAL6524HEAZ	0x22 (0b'0100010x)	MX-I2C2	1MHz Fm+	3.3V	IO EXP for IRQ/OUTPUT
U23	MPF9453AVMA1HN	0x32 (0b'0110010x)	MX-I2C2	1MHz Fm+	3.3V	PMIC
U49	PTN5110NHQZ	0x52 (0b'1010010x)	MX-I2C1	400KHz	3.3V	USB C PD
U48	PTN5110NHQZ	0x50 (0b'1010000x)	MX-I2C1	400KHz	3.3V	USB C USB1
U47	NX20P3483UK	0x71 (0b'1110010x)	MX-I2C1	400KHz	3.3V	USB Load Switch
J8	PCAL6408AEX1Z	0x20 (0b'0100000x)	MX-I2C1	400KHz	1.8V	M.2 / NGFF KEY-E
U11	P3T1085UK	0x48 (0b'1001000x)	MX-I2C1/I3C1	I3C-12.5MHz	3.3V	Temp Sensor (I3C support)
U12	PCF2131TF	0x53 (0b'1010011x)	MX-I2C1	400KHz	3.3V	Ext RTC

FT4232 I2C DEV TABLE

PART	DEVICE	I2C ADDR	PORT	Max SPEED	VOL	DESCRIPTION
U13	PCA9655EMTTXG	0x21 (0b'0100001x)	FTDI-I2C	1MHz Fm+	3.3V	IO EXP
U64	PAC1934T	0x11 (0b'0010001x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
U16	PAC1934T	0x12 (0b'0010010x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
U17	PAC1934T	0x13 (0b'0010011x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
U21	PAC1934T	0x14 (0b'0010100x)	FTDI-I2C	1MHz Fm+	3.3V	Power Monitor
U18	PCT2075	0x48 (0b'1001000x)	FTDI-I2C	1MHz Fm+	3.3V	Temp Sensor

## i.MX91 9x9 IOMUX:

[illegible]

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<b>Drawn by:</b> NXP SE		<b>IOMUX</b>	
<b>Approved:</b> NXP SE		Size Custom	Document Number SCH-90934 PDF: SPF-90934
		Date: <b>Saturday, February 08, 2025</b>	Sheet <b>24</b> of <b>24</b>