Quickstart Guide LPC1850 Board
LPC1850EVA-A4
Evaluation Board
Populated with LPC1850
or LPC4350

Document management

Document history

Version	Status	Date	Responsible	Reason for change
0.1	in progress	05.01.2011	Ma	New creation
0.2		27.04.2011	Ma	Changes to fit PCB Rev. –A2
1.0	Release	04.05.2011	Ma	Minor changes
1.01		15.09.2011	Ma	Minor changes
1.1	preliminary	20.09.2011	Gn	Update
1.2	RC	24.11.2011	Gn	Jumpers and Connectors, Tables, Graph
1.3	rework	12.01.2012	Ma	details
1.4	update	25.6.2012	Gn	Memories updated, power over USB

Purpose of the document

This document describes the jumpers and connectors on the NXP LPC1850EVA-A4 evaluation board developed by Hitex Development Tools GmbH.

Demonstrating the features of this LPC1850 evaluation board pre-settings are activated and configuration is made
To enable the user configuring normal modes and special features of the adequate settings are described

Authoring tools

MS-Word
Visio

Related documents and links

- Schematics SCM_LPC1850EVA-A4-2.pdf, 2011-12-22
- Assembly BPL_LPC1850EVA-A4-2.pdf, 2012-01-02
- LPC18xx http://www.hitex.com/LPC1800
- LPC1800 http://www.lpcware.com/gfiles/devper/lpc18xx
- LPC4300 http://www.lpcware.com/gfiles/devper/lpc43xx

Contents

Overview

The evaluation board has the following features:

- CPU: LPC1850 (ARM Cortex-M3) or LPC4350 (ARM Cortex-M4 with M0)
- Power-over-Ethernet
- Ready for energy consumption analysis with PowerScale of the complete board, the CPU-core and other peripherals
- SDRAM, SRAM, FLASH, qSPI flash
- Temperature sensor, SD card-connector
- CAN, UART, USART, Ethernet, USB (Host, Device, OTG)
- Debug with standard ARM JTAG and JTAG + Trace connector
- Ready for Jennic ZigBee module
- Small onboard display and NXP standard display / LCD/TFT interface
- HDMI interface
- Media connector to connect well known MP3-Player
- Push buttons, joystick and LEDs
- Wrap field with power and GND
- Audio IN and OUT, microphone IN, headphones OUT and a D-Class amplifier
- Motor Control interface for NXP inverter board
- VADC with OPAmp circuit

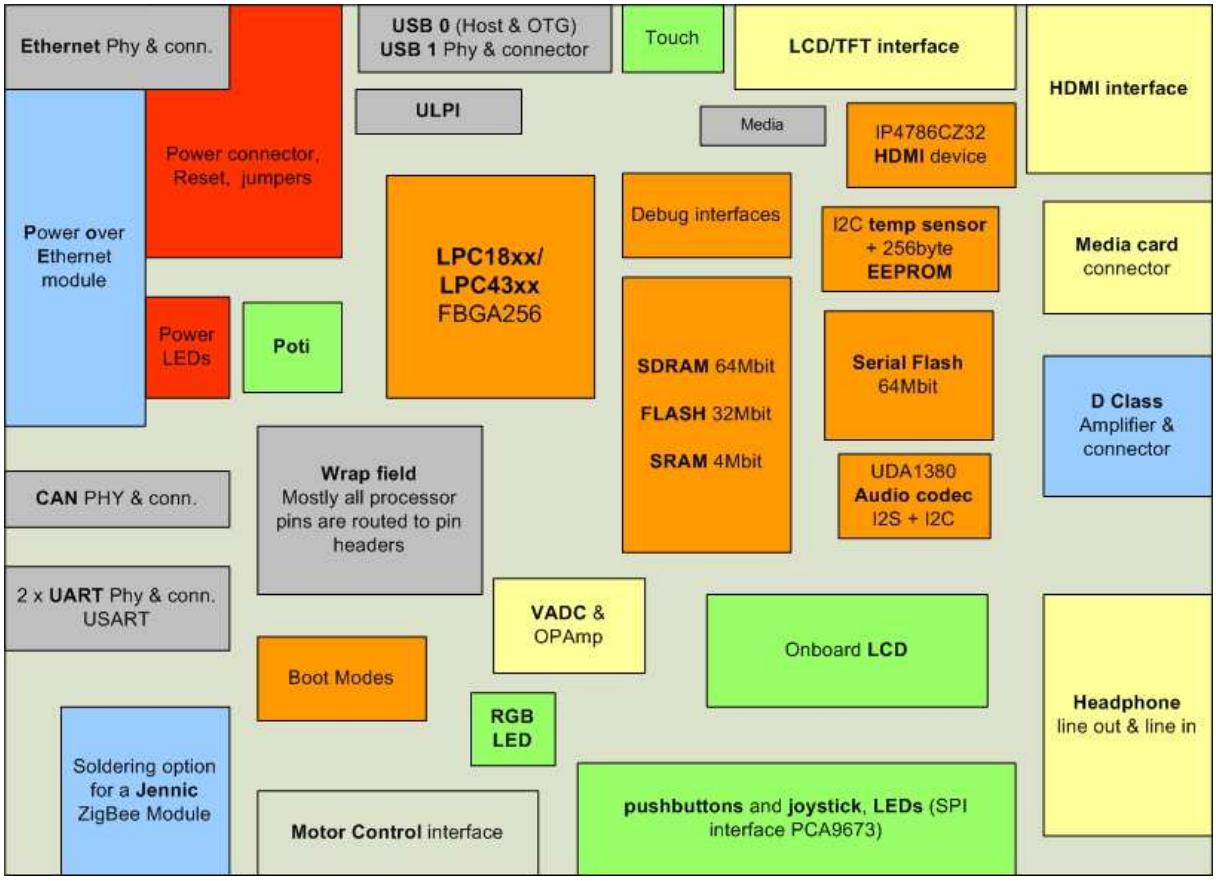


Figure 1 Block schematics

1 Image

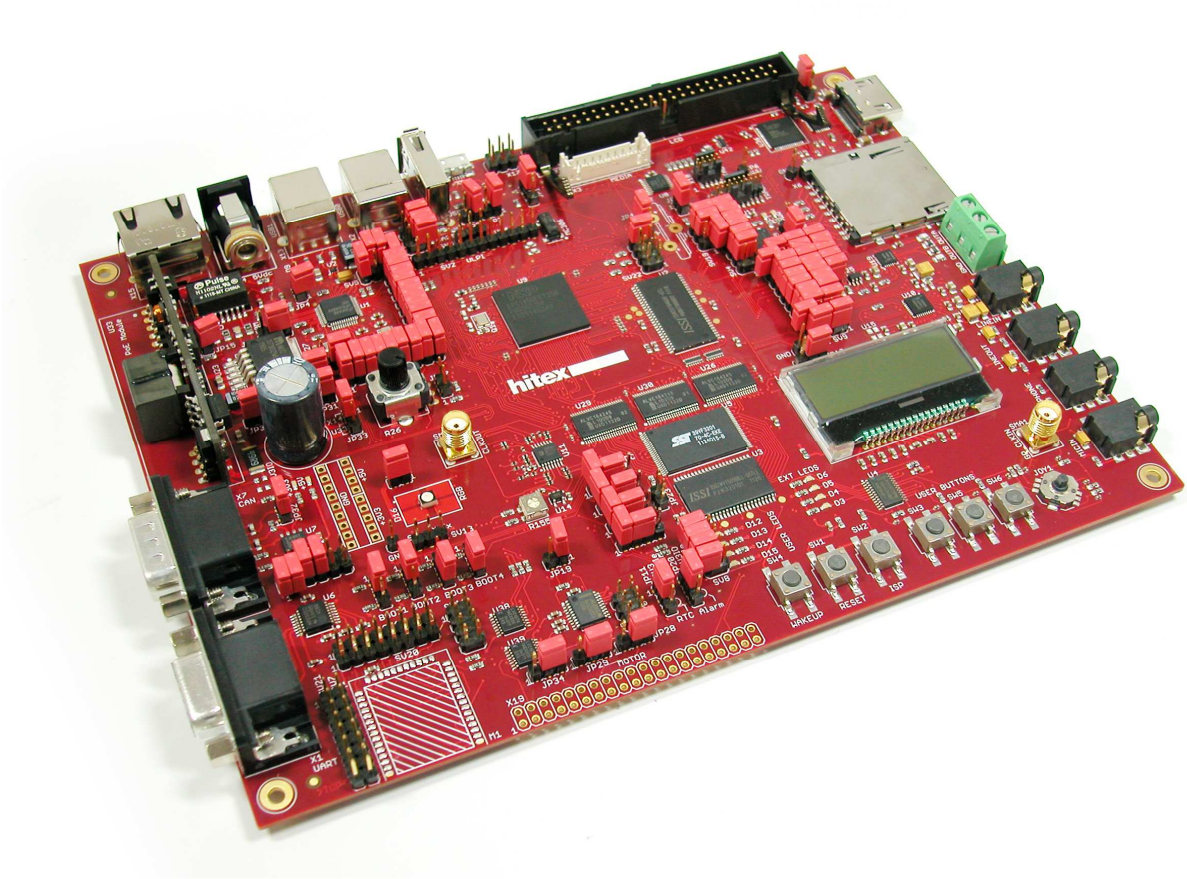
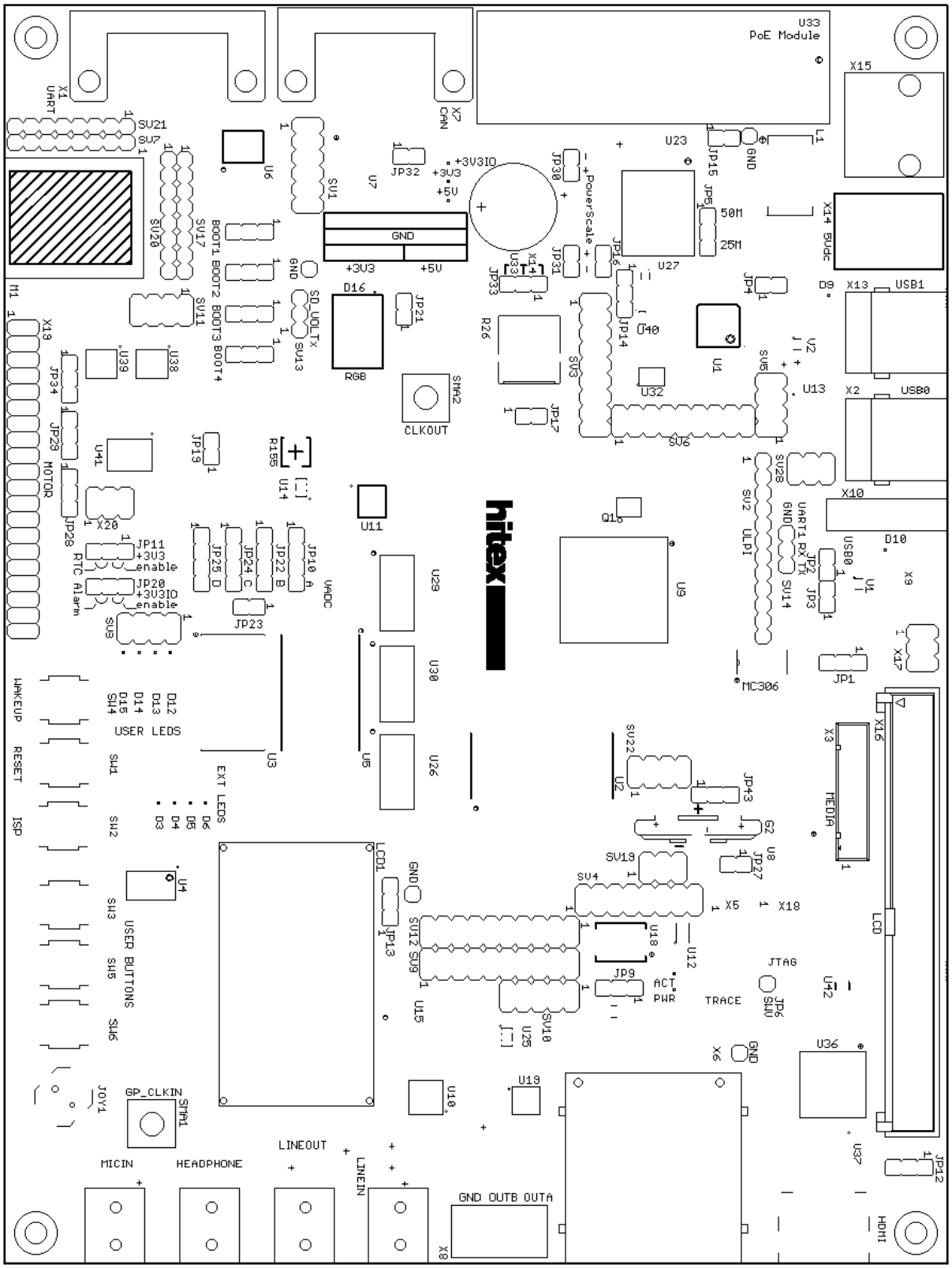


Figure 2 Real Image

2 Connectors

Designator	Function	Description
X1	UART	D-SUB9 female connector for UART
X2	USB0	USB-B (device) connector
X3	Media	This connector is to connect media devices like IPod and others with the Hitex Mediacable HK279. Please note: HK279 is not delivered within the LPC1850 evaluation board, but can be purchased separately at www.ehitex.de
X5	JTAG/Trace	Connector for attaching an ARM Cortex-Debug+Trace debugger (1.27mm pitch, 20 pins)
X6	SD Card	SD card connector
X7	CAN	D-SUB9 male connector with CANopen pinout
X8	D-Class amplifier	Screw connector for the D-Class amplifier output Pin 1: GND Pin 2: OUTB Pin 3: OUTA
X9	USB0	USB-microAB (OTG) connector
X10	USB0	USB-A (host) connector
HDMI	HDMI	HDMI interface
X13	USB1	USB-B (device) connector
X14	Power	A wall mount (or similar) AC/DC supply with **5V (DC)** output can be connected to X14. Inner plug is positive, outer shell is negative
X15	Ethernet/PoE	An Ethernet device for communication and/or a PSE device for powering the LPC1850 Evaluation Board can be connected to X15
X16	LCD	LCD connector for attaching an external LCD with NXP's standard LCD interface
X17	Touch	Touch pad interface for LCD touch devices
X18	JTAG	Shrouded connector for attaching a standard ARM Cortex debugger (1.27mm pitch, 10 pins)
X19	Motor Control	NXP Motor Control connector
X20	MISC	A UART (U41) and I2C1 are routed to this connector.
LINEIN	Line In	Connector to the input amplifier of U10 When no plug is connected, the signal is automatically routed to connector X3
LINEOUT	Line Out	Connector from the output amplifier of U10 When no plug is connected, the signal is automatically routed to connector X3
HEADPHONE	Headphone	Connector from the headphones output amplifier of U10
MICIN	Microphone	Connector to the microphone input amplifier of U10
SMA1	LCDDCLK	
SMA2	CLKOUT	From LPC1850
SW1	Reset	Global hardware reset
SW2	ISP	Switch to pull EXTBUS_A9 low
SW4	Wakeup	In combination with SV22 pins 7-8, pull WAKEUP0 low
SW3	Pushbutton 1	User Pushbutton 1. Connected to I2C-GPIO expander U4
SW5	Pushbutton 2	User Pushbutton 2. Connected to I2C-GPIO expander U4
SW6	Pushbutton 3	User Pushbutton 3. Connected to I2C-GPIO expander U4
JOY1	Joystick	User Joystick function. Connected to I2C-GPIO expander U4


U33
PoE Module
X15
X1
UART
X7
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SV7
SV20
SV17
SV11
BOOT1 BOOT2 BOOT3 BOOT4
U6
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+5V
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GND OUTB OUTA
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RGB
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SD_VOLTx
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CLKOUT
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R155
U14
MOTOR
JP34
JP28
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U38
X13
X20
JP11
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enable
JP20
+3V3IO
enable
RTC Alarm
SV8
JP23
JP25 D
JP24 C
JP22 B
JP10 A
VADC

3 Default settings

Jumper, Configurations and pinheaders

Jumper	Function	Description
SV1	CAN	Default: Pin 1-2 and 3-4 are open No CAN interface (mutual exclusive to input-data of U10 and U19)
	UART	Default: Pin 5-6 and 7-8 are closed UART is connected to UART0 interface of the CPU
	UART bootloader	Default: Pin 9-10 and 11-12 are open Do not use the external bus interface, while using the UART bootloader!
SV2	USB1 ULPI	USB1_ULPI signals are routed to this connector.
SV3 and SV6	Ethernet (MII/RMII)	SV3 and SV6 are completely closed (pin 1-2, 3-4, etc.) Ethernet is available in MII- and RMII-Mode. Ethernet MII is mutual exclusive to SD card. RMII is available.
SV4	SPI flash (qSPI)	SV4 is completely closed (pin 3-4, 5-6, 7-8, 9-10, 11-12, 13-14) Pin 9-10 is mutual exclusive to SV19 pin1-2 Pins 1, 2 are GND and pins 15, 16 are +3V3 This allows for attaching a users board to the pinheader.
SV5	USB power	SV5 is closed at pins 1-2 and 7-8. Pins 3-4 and 5-6 are open. Pins 3-4, 5-6 (part of USB1 powering) are mutual exclusive to Motor control and MII-Ethernet.
SV7	Jennic Module	
SV8	LED	4 colored user LED (default: all pins are open)
SV9	UDA_RST	Pin 1-2 is closed, Reset of U10
	Pin 3-4	Open, not connected
	I2S_TX*	Pins 5-6, 7-8, 9-10 are closed (mutual exclusive to CAN)
	I2S_RX*	Pins 11-12, 13-14, 15-16 are closed
	I2C0*	Pins 17-18, 19-20 are closed
SV10	I2C0*	Pins 1-2, 3-4 are closed
	I2S_TX*	Pins 5-6, 7-8, 9-10 are closed (mutual exclusive to CAN)
SV11	Jennic Module	
	UART1	TX, RX
SV12	SD card	SV12 is closed and is mutual exclusive to MII-Ethernet. Only pins 3-4 and 17-18 are left open.
SV13	SD_Volt	SDIO_VOLT0, 1, 2
SV14	UART1	Signals to UART1
SV17	Jennic Module	
SV19	I2C0*	Connect I2C0 to serial EEPROM, Pins 3-4, 5-6 are closed
	SPI_SIO3	EVENT# (output), pin 1-2 is open Mutual exclusive to SV4 9-10
SV20	Jennic Module	
SV21	Jennic Module	
SV22	WAKEUP	Pos 7-8 is closed Pos 1-2, 3-4, 5-6 are open
SV28	Media Connector USB	Pos 1-2, 3-4, 5-6 are open (jumpers only set to one pin). When closed USB1 signals and power are routed to Media Connector X3.

A picture of the default configuration can be downloaded at www.hitex.com/LPC1800

4 Jumpers

Jumper	Function	Description
BOOT1 – BOOT4	Bootloader	See chapter **Fehler! Verweisquelle konnte nicht gefunden werden.** Default: BOOT1 pos. 1-2, BOOT2 pos. 1-2, BOOT3 pos 2-3, BOOT4 pos 2-3
JP1	R42	Connects R42 to GND when set to position 1-2 Default: pos. 1-2
JP2	USB0_ID	Pulls USB0_ID permanently to GND Default: pos. 1 (open)
JP3	USB0_IND1	Connects USB0_IND1 to LED D10 Signal USB_IND1 is shared with MCIN1 (Motor control) Default: pos. 1 (open)
JP4	USB1_IND1	Connects USB1_IND1 to LED D9 Signal USB1_IND1 is shared with ENET_RXD2 and therefore mutual exclusive to MII-Ethernet. Default: pos. 1 (open)
JP5	Ethernet Phy Clock select	Clock selection for the Ethernet Phy device Clock selection for the Ethernet Phy device. (see also JP14) Pos. 1-2 50MHz, pos. 2-3 25MHz, Default: pos. 2-3 (25MHz)
JP6	TDO	
JP7, JP8, JP18, JP26	GND	
JP9	SD power	Switches power to the SD card either by CPU (signals SDIO_POW) (pos. 2-3) or permanently (pos. 1-2) Default: pos. 2-3
JP10	ADC4	Connect MADC4 (Motor control) to ADC4 or by VADC OpAmp circuit Default: pos 2-3, another jumper is set to pos 1-open
JP11	RTC	When set to pos. 1-2 the +3V3 regulator is enabled. With this jumper set to pos. 2-3, the CPU can set signal RTC_ALARM to power up or shut down its IO +3V3IO or the complete +3V3 power of the board Default: pos. 1-2
JP12	LCD	Switches either +3V3 (pos. 1-2) or signal CTOUT12/BL to the external LCD Interface (pos. 2-3). Default: pos. 1-2
JP13	Audio Codec Clock	Connects the SYSCLK Pin of the UDA1380 device to CLK3 (pos. 1-2) or LCDCLKIN (pos. 2-3). Alternatively a 24.576MHz 3,3V 3.2x2.5mm crystal oscillator can be assembled to supply U10 with a clock. Default: pos. 1-2
JP14	Ethernet TX Clock	Connects controller pin ENET_TX_CLK to Phy TX_CLK pin (pos. 2-3) or to the 50 MHz clock from oscillator (pos. 1-2) Default pos. 2-3
JP15	Ethernet RX_DV	If closed the signal RX_DV is pull up to 3V3 domain Default: pos 1 (open)
JP16	PowerScale	At this point a Hitex PowerScale probe can be connected for current sensing the +3V3C (CPU Core power) and +3V3IO (CPU IO power). If not used, keep this jumper closed! Default: pos. 1-2 (closed)

JP17	DBGEN	Connects the Pin DBGEN of the LPC1850 to GND Default: open / pull up
JP19	Max3222 Enable	Pulls the /EN pin of the MAX3222 device to GND and enables UART1 Default: pos 1 (open)
JP20	3V3IO	Enable the power domain 3V3IO by RTC_ALARM signal (pos. 2-3) or permanent (pos. 1-2) Default pos. 1-2
JP21	RGB-LED	Connect the common Anode of the RGB LED to +5V Default: pos 1-2 (closed)
JP22	ADC5	Connect MADC5 (Motor control) to ADC5 or by VADC OpAmp circuit Default: pos 2-3, another jumper is set to pos 1-open
JP23	Write protect	Write protect of parallel flash (U5). Close for write protect. Default: (open)
JP24	ADC6	Connect MADC6 (Motor control) to ADC6 or by VADC OpAmp circuit Default: pos 2-3, another jumper is set to pos 1-open
JP25	ADC7	Connect MADC7 (Motor control) to ADC7 or by VADC OpAmp circuit Default: pos 2-3, another jumper is set to pos 1-open
JP27	HDMI_INT	For calibration purposes this pin on the TDA19988 chip is an input for a clock signal. Default: pos 1-2 (closed)
JP28	MC	Connects either CTIN6 (pos 1-2) or MCIN0 (pos 2-3) to X19-pin13 Default: pos 2-3
JP29	MC	Connects either CTIN0 (pos 1-2) or MCIN0 (pos 2-3) to X19-pin11 Default: pos 2-3
JP30	PowerScale	At this point a Hitex PowerScale probe can be connected for current sensing of the whole board. If not used, keep this jumper closed! Default: pos. 1-2 (closed)
JP31	PowerScale	At this point a Hitex PowerScale probe can be connected for current sensing the +3V3 power. If not used, keep this jumper closed! Default: pos. 1-2 (closed)
JP32	CAN 120R	Connects a 120OHM termination resistor to the CANH/CANL lines Default: pos. 1-2 (closed)
JP33	Power Over Ethernet	Switches between Power-over-Ethernet or 5V (DC) wall plug for board supply. Default: pos. 1-2 (wall plug)
JP34	MC	Connects either CTIN1 (pos 1-2) or MCIN1/USB0_IND1 (pos 2-3) to X19-pin11 Default: pos 2-3
JP43	VBAT	Connects either a battery (not mounted) or +3V3C (Core power) to the VBAT pin of the CPU. Also hardware reset pullup R41 is connected to that power. Default: pos. 2-3 (+3V3C)

A picture of the default configuration can be downloaded at www.hitex.com/LPC1800

5 Features

5.1 Power

5.1.1 AC/DC Power Supply

A wall mount (or similar) AC/DC supply with 5V (DC) output can be connected to X14.
Inner plug is positive, outer shell is negative. Jumper JP33 has to be set to pos 1-2. Over all current consumption will be depending on the active elements on the board. But at least 280mA with LCD backlight are expected. …

5.1.2 USB

VBUS (+5V) can be supplied by either X13 or X2/X9. Please note that USB current is limited to 100mA. If the LPC1850 is running a program, which enumerates at the USB-Bus, the current limit can be set to 500mA (within that program) …

5.1.3 Power-over-Ethernet (PoE)

A Power-over-Ethernet module (U33) is populated on the evaluation board. Jumper JP33 has to be set to pos 2-3. Maximum output power of the module is 5V - 9W. …

5.1.4 Power LEDs

3 LEDs (D1, D2, and D11) are mounted to monitor the internal and external power domains near JP32.

5.1.5 PowerScale Connectors

Three connectors (JP16, JP30 and JP31) are allowing measuring the power consumption in current and voltage on different power domains on the board.

5.1.6 RTC Power Domain

The RTC of the LPC18xx chips ha a separate power domain. This power domain can be connected to the +3V3 domain of the controller (default) with JP43 pos 2-3 or to a battery which is not mounted on the original board with pos 1-2.

5.1.7 Memories

The board is populated with
Parallel Flash: SST39VF3201 (2M x 16 = 32Mbit)
Serial Flash: Spansion FL064P1F (64Mbit) or (older Versions : Winbond W25Q80BV (8Mbit))
Synchronous Dynamic RAM (SDRAM): IS42S16400D (1M x 16 bit x 4 banks = 64Mbit)
Static RAM (SRAM): IS62WV25616ALL (256k x 16 = 4Mbit)

5.2 Multimedia

5.2.1 Audio

Audio Codec and Class-D amplifier are populated on the board. To run the devices be sure connector SV 9 is set correctly.

5.2.2 HDMI Interface

From the 24bit RGB interface the HDMI interface is driven with video data. Test jumper must be fixed and the device need configuration by the CPU.

5.2.3 LDC/TFT Interface

The 24 bit RGB color TFT/LCD interface is available on the 50 pin standard header.

5.2.4 Media Connector

The LPC1850 board provides a media connector. This connector is to access media devices like IPod and others with the Hitex Mediacable HK279.
Please note: HK279 is not delivered within the LPC1850 evaluation board, but can be purchased separately at www.ehitex.de

5.3 User Interface

5.3.1 Potentiometer

A potentiometer (R26) is connected to pin PF.9 of the LPC1850.

5.3.2 LEDs, Push-Buttons and Joystick

LEDs, push-buttons and a joystick are available by using NXP's I2C-GPIO expander PCA9673 (U4). The I2C address is hex 0x48.

5.3.3 LCD

4 LEDs are accessible over I2C interface expander U4 (address 0x48) and 4 LEDs are directly connected to the CPU.

5.4 VADC with OPAmp circuit

Connect pins 2-3 of jumpers JP10, JP22, JP24 or JP25 when MADCx signals are within the voltage range of the VADC signals (limited by LPC1850). When connecting pins 1-2 and 3-4, the MADCx signals are routed to the OpAmp circuit for attenuation. Trimmer potentiometer R155 can be used to change the offset.

6 Mutual Exclusive Functions

In general, all signals with double names like “Ethernet/SD card” show that this signal is used in more than one function.

6.1 Ethernet, SD Card

The Ethernet (MII) is multiplexed with the SD card interface (SDIO).
Therefore jumper arrays SV3 and SV6 are used to connect ENET*-signals to the Ethernet PHY (U1) as well as jumper array SV12 connects SDIO*-signals to the SD card interface (X6).
In the schematic the double used pins can be identified by their double name ENET_*/SDIO_*.

Please note: It is possible to use RMII and SD-Card.

6.2 CAN Interface, I2S (Audio)

The CAN interface is multiplexed with some I2S functionality. The audio outputs can’t be used when the CAN interface is used.
Jumper array SV9 routes the I2S signals to the Audio-Codec UDA1380 (U10) and SV10 routes them to the D-Class amplifier (U19).
Jumper array SV1 pins 1-2 and 3-4 connect the CAN transceiver (U7) to the signals.

In the schematic the double used pins can be identified by their double name CAN1_TD/I2S_TX_SDA and CAN1_RD/I2S_TX_WS.

6.3 UART, Memories and UART-Bootloader, USART

The UART bootloader pins at the CPU are multiplexed with the external bus interface and so with all onboard memories.
At jumper array SV1 the user can set the jumpers to pins 5-6 and 7-8 for normal UART operation. If set to pins 9-10 and 11-12 the UART transceiver will be connected to signals EXTBUS_A13 and EXTBUS_A12. To avoid short circuit and damage< to the CPU and UART transceiver, the user should not use the external bus interface while using UART bootloader on those pins.

6.4 Ext. LCD and ULPI

The ULPI (USB1) interface is brought out to a pin-header for easier access. User should take care not to use these signals in parallel with the external LCD.

6.5 HDMI interface

The HDMI interface uses the same signals, which are also used for external LCD/ULPI.

6.6 USB0

The USB0 functionality is brought out to a HOST (X10), a DEVICE (X2) and an OTG (X9) connector. Use only one connector at a time.

6.7 USB1

The USB1 functionality is brought out to a DEVICE (X13) connector. Also there is the option to connect the media connector X3 (USB lines) to the bus by closing jumper array SV28.
USB1 power signals MCOB1/USB1_PWR_FAULT, ENET_TXD3/USB1_VBUS and ENET_TXD2/USB1_IND1 are multiplexed with Ethernet or motor control functions.

6.8 Media Connector and Audio

If no 3,5mm audio plug is inserted into Audio IN (LINEIN) or Audio OUT (LINEOUT), the corresponding signals of the audio codec (U10) will automatically connect to the media connector (X3).

6.9 SPI

Signal SPI_SIO3 is connected to the qSPI device (U18) and to the I2C-EEPROM (U12).
Use SV19 pins 1-2 or SV4 pins 9-10 to connect either to U12 or U18.

6.10 Power Supply

Power the board only by one power source at the same time. Use either

X14	Wall mount AC/DC	5V (DC)
X15	PoE	5V (DC) by onboard PoE-converter
X2/X9	USB0	5V (DC)
X13	USB1	5V (DC)

6.11 Motor Control Connector

NXP's Motor control connector X19 uses some signals that are multiplexed with other functions on the board. Analog switches U38 and U39 can switch some of these signals. The switches are controlled by the LPC1850's signal MC_SEL.

X19	MC_SEL	Signal
Pin 3	L	CTOUT2
	H	ENET_RXD2/USB1_IND1
Pin 4	L	CTOUT3
	H	ENET_TXD2
Pin 5	L	CTOUT4
	H	ENET_TXD3/USB1_VBUS_EN
Pin 6	L	CTOUT5
	H	MCOB1/USB1_PWR_FAULT
Pin 7	L	CTOUT6
	H	ENET_RX_ERR
Pin 8	L	CTOUT7
	H	ENET_RXD3

Except ENET_RX_ERR all other Ethernet signals are not used in RMII-Mode.

X19	Jumper Block				Signal
Pin 11	JP29	1	2	3	CTIN0 (also routed to pin 1)
		1	2	3	MCIN2

X19	Jumper Block				Signal
Pin 12	JP34	1	2	3	CTIN1 (also routed to pin 2)
		1	2	3	MCIN1/USB0_IND1

X19	Jumper Block				Signal
Pin 13	JP28	1	2	3	CTIN6 (also routed to pin 21)
		1	2	3	MCIN0

X19 Pin 20 is TRACEDATA[3]/CTIN2.
X19 Pin 31 is CTOUT12/BL.
X19 Pin 32 is ADC1_0/SDIO_VOLT1.

7 Special setup configurations

7.1 Boot options

Mode	Boot[4:1]				Environment
USART0	low	low	low	low	Boot from device connected to USART0 using pins P2_0 and P2_1
SPIFI	low	low	low	high	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8
EMC 8-bit [1]	low	low	high	low	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus
EMC 16-bit	low	low	high	high	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus
EMC 32-bit [1]	low	high	low	low	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus
USB0	low	high	low	high	Boot from USB0
USB1	low	high	high	low	Boot from USB1
SPI (SSP)	low	high	high	high	Boot from SPI flash connected to the SSP0 interface on P3_3 (SSP0_SCK), P3_6 (SSP0_MISO), P3_7 (SSP0_MOSI), and P3_8 (SSP0_SSEL)
USART3 [1]	high	low	low	low	Boot from device connected to USART3 using pins P2_3 and P2_4

[1] Not supported on LPC1850/LPC4350 Evalboard

7.2 USART0 Bootloader

Function	Jumper Block			BootModes					Environment
Invoke Bootloader on USART0	SV1	1	2	Boot1	1	**2**	**3**		115200,8,N,1
		3	4						Send: 0x3F
		5	6	Boot2	1	**2**	**3**		Replies: „OK“
		7	8						
		9	**10**	Boot3	1	**2**	**3**		
		11	**12**						
				Boot4	1	**2**	**3**		

7.3 RTC Power Domain

Function	Jumper Block				Power Domain
Power Domain on RTC	JP43	1	**2**	**3**	3V3C
		1	**2**	3	Battery

7.4 Ethernet Phy Clock Selection

Function	Jumper Block				Clock
Ethernet Phy clock	JP5	1	2	3	50 MHz
		1	2	3	25 MHz

7.5 TXCLK selection

Function	Jumper Block				ENET_TX_CLK
Ethernet Phy clock	JP14	1	2	3	CLK50
		1	2	3	Phy TX_CLK

7.6 Power Over Ethernet (PoE)

Function	Jumper Block				ENET_TX_CLK
Power Source	JP33	1	2	3	X14 (Power Jack)
		1	2	3	POE module

7.7 SD_Card Power

Function	Jumper Block				FET for VDD
SD-Card Pow	JP9	1	2	3	Gnd (enabled)
		1	2	3	SDIO_POW

7.8 X3 Media Connector

Function	Jumper Block				FET for VDD
X3 Media Connector	JP1	1	2	3	500k to GND
		1	2	3	open

7.9 LCD Pin50

Function	Jumper Block				LCD Pin 50
LCD Pin50	JP12	1	2	3	3V3
		1	2	3	CTOUT12/BL

7.10 RTC Alarm

Function	Jumper Block				RTC_ALARM Pin
RTC Alarm	JP11	1	2	3	enable 3V3IO
		1	2	3	pull up

7.11 ADC4, ADC5 ADC6, ADC7 input selection

Function	**Jumper Block**					**ADC4**
ADC4	JP10	1	2	3	4	1-2 OpAmp to ADC4, 3-4 MADC4 to VADC_A
		1	2	3	3	MADC4 to ADC4

Function	**Jumper Block**					**ADC5**
ADC5	JP22	1	2	3	4	1-2 OpAmp to ADC5, 3-4 MADC5 to VADC_B
		1	2	3	4	MADC5 to ADC5

Function	**Jumper Block**					**ADC6**
ADC6	JP24	1	2	3	4	1-2 OpAmp to ADC6, 3-4 MADC6 to VADC_C
		1	2	3	4	MADC6 to ADC6

Function	**Jumper Block**					**ADC7**
ADC7	JP25	1	2	3	4	1-2 OpAmp to ADC7, 3-4 MADC7 to VADC_D
		1	2	3	4	MADC7 to ADC7

8 Programming the parallel flash on Hitex LPC1850EVA-A4

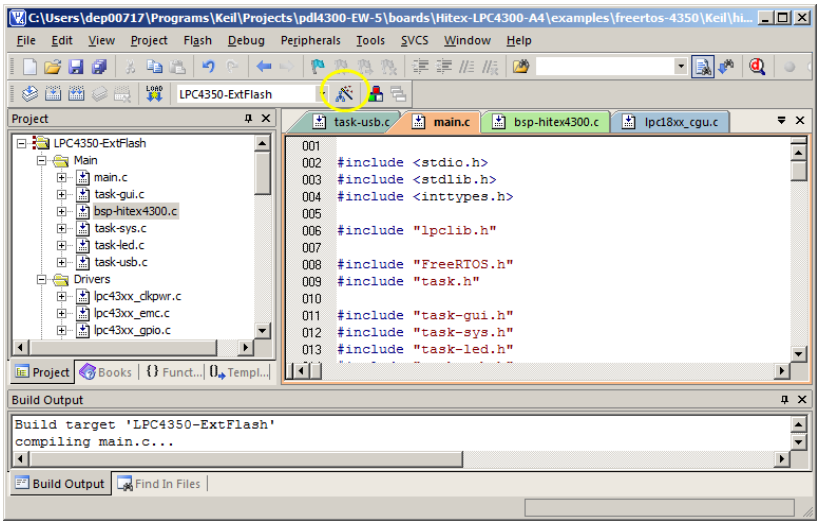
Device types on the Rev. A4 board:

- SST39VF3201 or SST39VF3201B (16-bit bus, 4 MByte)
- Spansion S25SL129 serial NOR flash (quad SPI)

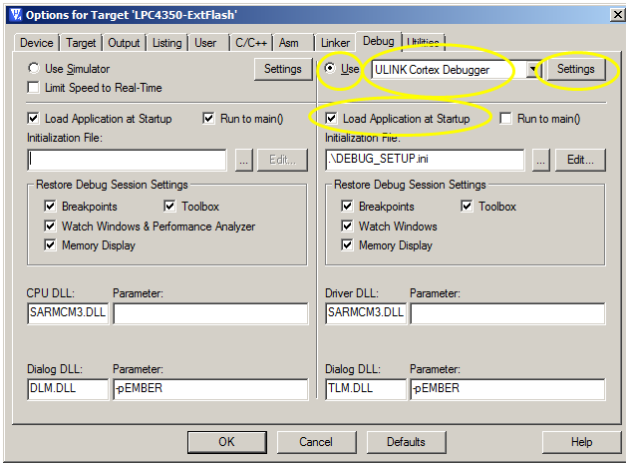
The parallel flash can be programmed with the flash utility inside KEIL µVision 4. The JTAG connection between the µVision debugger and the LPC1850/4350 is used to download and program data into the external flash device. For each flash type you need a specific flash algorithm.
The algorithm for the SST39VF3201/3201B can be found in the folder .\software_design\µVision4 of the CDROM (SST39VF3201x_Hitex.FLM)
Please put this file into the following folder of you KEIL µVision installation: .\KEIL\ARM\Flash
The source project of the flash algorithm is also on the CDROM, to recompile it you need a licensed version of µVision, because the creation of position independent target code does not work with the evaluation version.
The INI file LPC18xx_43xx_ExtFlashProg.ini needs to be in a convenient place on your computer, e.g. copy it into the folder of your own µVision project

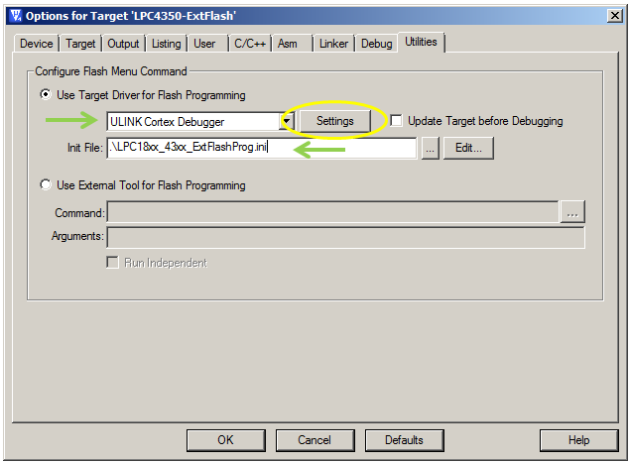
If you have a project for the LPC1850 or LPC4350 which should run from external flash you need to do the following things in µVision:

1. Enter the configuration settings for your project:



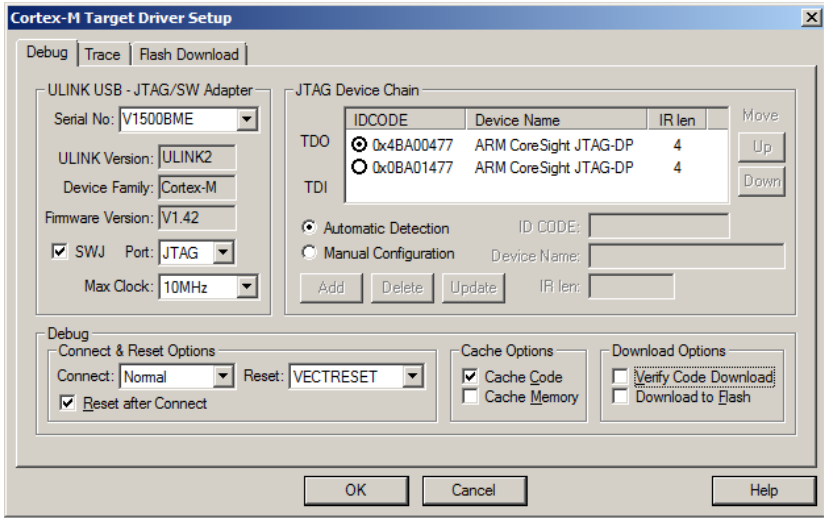
2. Select the correct debugger hardware and the INI file:
   Working debuggers are e.g. ULINK2, ULINK Pro, J-Link



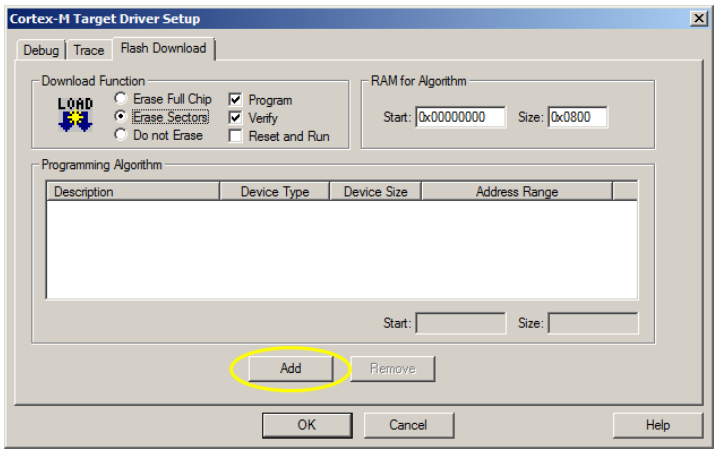


3. Enter the Settings for Debug and set the parameters as shown in the screenshot:

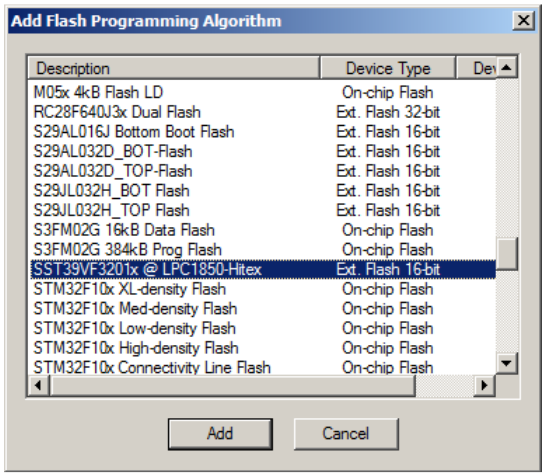
   In case of the LPC4350 the first ARM core is the Cortex-M4, the second is the Cortex-M0. With the LPC1850 you will see only one core, the Cortex-M3.



4. Enter the Settings for Flash programming:

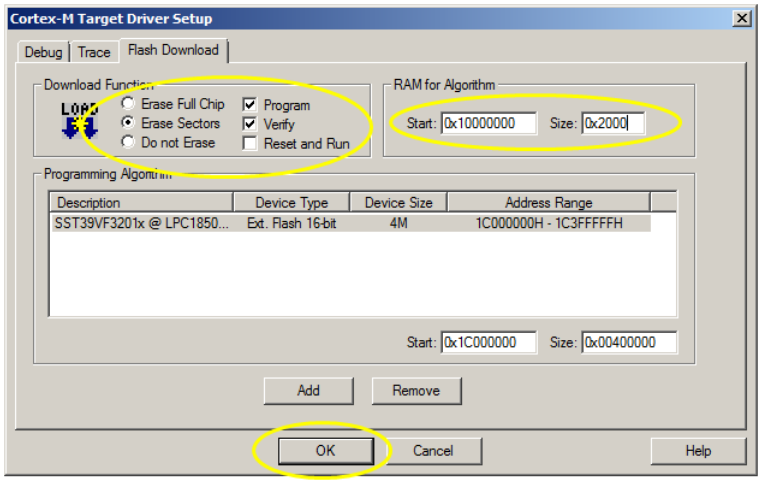


5. Click on Add and select the SST39VF3201x device for the Hitex board, then finish with a click on Add

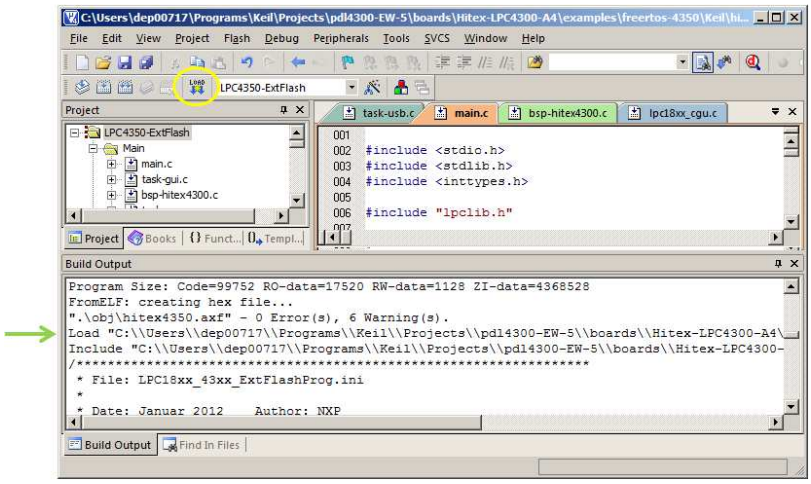


6. Fill in the correct parameters for the “RAM for Algorithm” settings:
   - Start = 0x10000000
   - Size = 0x2000

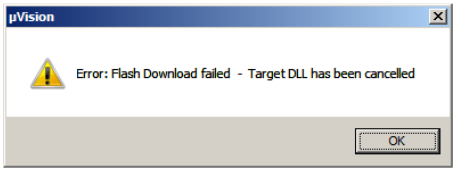
   Choose the appropriate Download Functions and then confirm with OK.



7. With a click on the Load icon a correctly compiled project is now downloaded to the flash memory.



8.1 Troubleshooting:

1. 

That's the most common problem and can have a lot of root causes:

- Wrong settings in the Debug mask (see step 2 above)
- Memory access to the target failed. Check if you provided the correct start address for the flash algorithm (see step 2 above)
- Debugger does not get access to the target because of a problem on the target board.
  1) Check the physical connection.
  2) Choose another bootmode on the Hitex board.
  (see below at 3).

2. 

The value for the size of the RAM for the flash algorithm is too low. Please choose 0x2000 (see step 6 above)

3. The debugger connection to the LPC1850/4350 can be a problem in case the ARM core(s) are already executing code from the boot flash with interrupts and/or high speed. Then it helps to select a boot mode which does not start any code, but remains in the bootmode.
Change one of the jumpers Boot1/Boot2/Boot3/Boot 4 to another position and then try to flash again.

9 Notes

9.1 Parallel Flash (U5)

As parallel flash an SST39VF3201-70-4C-EKE from SST is used. However due to availability of this flash device, also an SST39VF3201**B**-70-4C-EKE from SST can be populated. These devices are electrically fully compatible but they do have different IDs that can be read back from the device. Also the flash algorithm has to be slightly changed.
For the flash algorithm this means the following:

- Read the flash ID: 0x235B for the SST39VF3201 and 0x235D for the SST39VF3201**B**
- Adapt the flash commands. Mostly it's just sending 0x555 (3201**B**) instead of 0x5555 (3201) and 0x2AA (3201**B)** instead of 0x2AAA (3201)

9.2 Jennic ZigBee

Optionally a Jennic ZigBee module can be populated. The board is prepared with the standard layout and connectors.

9.3 Powering over USB while debugging

Powering the board over USB connector from a USB host should not a problem while the current is not exceeding 50 mA. Taking more power from a USB host requires a sufficient USB device enumeration requesting the power from the host. Only if this power is granted by the host the device is allowed to take more than 50mA. Especially external display devices are able to exceed the 500 mA overall maximum power which can be taken from a USB 2.0 host. (background illumination)
Working without that limitation is possible if the USB device plug can be used to connect to a USB hub which is tolerant to the power consumption or a special USB power connector.