

# AUD-EXP-42448

## Table of Content

Page 1	COVER
Page 2	BLOCK DIAGRAM
Page 3	POWER&INTERFACE
Page 4	AUDIO CODEC
Page 5	AUDIO INPUT
Page 6	AUDIO OUTPUT
Page 7	
Page 8	
Page 9	
Page 10	
Page 11	
Page 12	
Page 13	
Page 14	
Page 15	
Page 16	
Page 17	
Page 18	
Page 19	
Page 20	
Page 21	
Page 22	
Page 23	
Page 24	
Page 25	
Page 26	
Page 26	
Page 27	
Page 28	

## Revision History

Rev. Code	Date	By	Description
A	2021-01-06	Shawn Shi	Initial Release
B	2021-03-26	Shawn Shi	1. Add R83(DNP) for 3V3 power option 2. Add P1/P2, R84/R85 for MIC input 3. Populate R82, DNP R28 for DGND/AGND connection

1. Unless Otherwise Specified:
- All resistors are in ohms, 1/16 Watt,0402  
All capacitors are in uF,0402  
All voltages are DC  
All polarized capacitors are aluminum electrolytic
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:  
\_B Denotes - Active-Low Signal  
<> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



Microcontroller Product Group  
6501 William Cannon Drive West  
Austin, TX 78755-8500

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

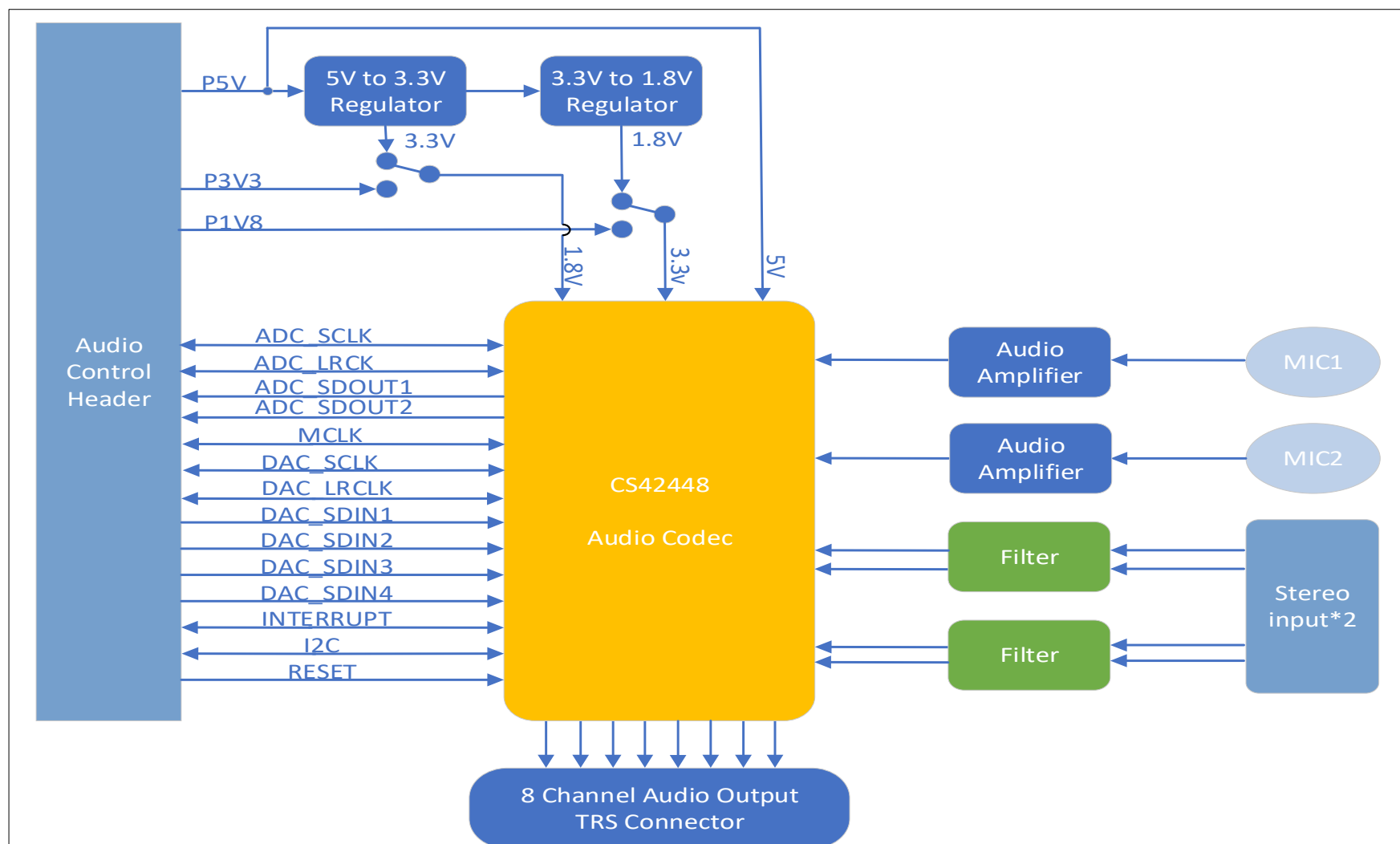
ICAP Classification:CP: IUC: PUBI:

Designer:Shawn ShiDrawing Title:**AUD-EXP-42448**

Drawn by:Shawn ShiPage Title:**COVER**

Approved:YesSize CDocument NumberSCH-48012, PDF: SPF-48012Rev B

Date:Friday, March 26, 2021Sheet 1 of 8



[illegible]

### 5V Control

The 5V Control circuit diagram shows a power switch controlled by a microcontroller pin (DC\_GPIO1). The input signal is connected to the base of a PNP transistor (Q2, PN7002BKW) through a 100K resistor (R7). The emitter of Q2 is connected to the positive terminal of a 5V battery (P5V). The collector of Q2 is connected to the gate of an N-channel MOSFET (Q1, IRLML6401) through a 47K resistor (R2). The MOSFET's source is connected to ground, and its drain is connected to the positive terminal of a 5V battery (P5V\_S) through a 100K resistor (R5). The MOSFET's gate is also connected to ground through a 2200PF capacitor (C13). The MOSFET's drain is connected to the positive terminal of a 5V battery (P5V\_S) through a 10V capacitor (C7). The MOSFET's drain is also connected to the positive terminal of a 5V battery (P5V\_S) through a 10V capacitor (C8).

1-->>Enable  
0-->>Disable

### 3V3 LDO

The 3V3 LDO circuit diagram shows a 3.3V LDO regulator (U1, MAX350mA) connected to a 5V input (P5V\_S). The input is connected to the IN pin of the LDO through a 10V capacitor (C9). The LDO's output is connected to the positive terminal of a 3.3V battery (P3V3\_S) through a 4.7uF capacitor (C11). The LDO's output is also connected to the positive terminal of a 3.3V battery (P3V3\_S) through a 10V capacitor (C12). The LDO's output is also connected to the positive terminal of a 3.3V battery (P3V3\_S) through a 10V capacitor (C10). The LDO's output is also connected to the positive terminal of a 3.3V battery (P3V3\_S) through a 10V capacitor (C10).

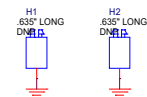
### 1V8 LDO

The 1V8 LDO circuit diagram shows a 1.8V LDO regulator (U2, MAX250mA) connected to a 3.3V input (P3V3\_S). The input is connected to the VIN pin of the LDO through a 4.7uF capacitor (C14). The LDO's output is connected to the positive terminal of a 1.8V battery (P1V8\_S) through a 4.7uF capacitor (C16). The LDO's output is also connected to the positive terminal of a 1.8V battery (P1V8\_S) through a 10V capacitor (C17). The LDO's output is also connected to the positive terminal of a 1.8V battery (P1V8\_S) through a 10V capacitor (C17).

### Power Options

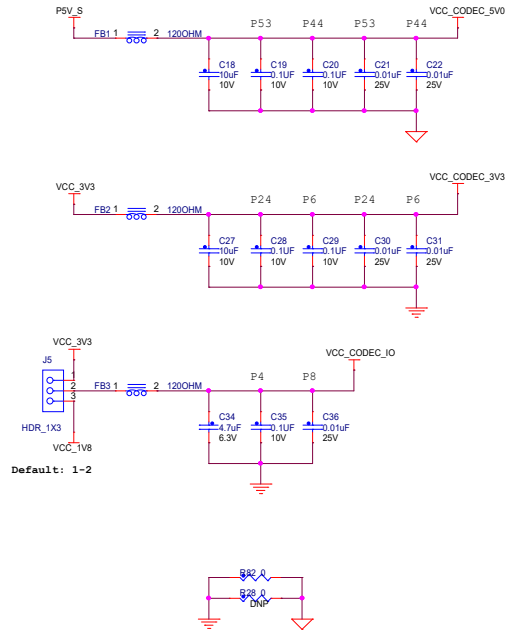
The Power Options circuit diagram shows two power switches controlled by microcontroller pins (VCC\_3V3 and VCC\_1V8). The VCC\_3V3 pin is connected to the base of a PNP transistor (Q3, PN7002BKW) through a 100K resistor (R8). The emitter of Q3 is connected to the positive terminal of a 3.3V battery (P3V3). The collector of Q3 is connected to the positive terminal of a 3.3V battery (P3V3\_S) through a 10V capacitor (C18). The VCC\_1V8 pin is connected to the base of a PNP transistor (Q4, PN7002BKW) through a 100K resistor (R9). The emitter of Q4 is connected to the positive terminal of a 1.8V battery (P1V8). The collector of Q4 is connected to the positive terminal of a 1.8V battery (P1V8\_S) through a 10V capacitor (C19).

## Power Options

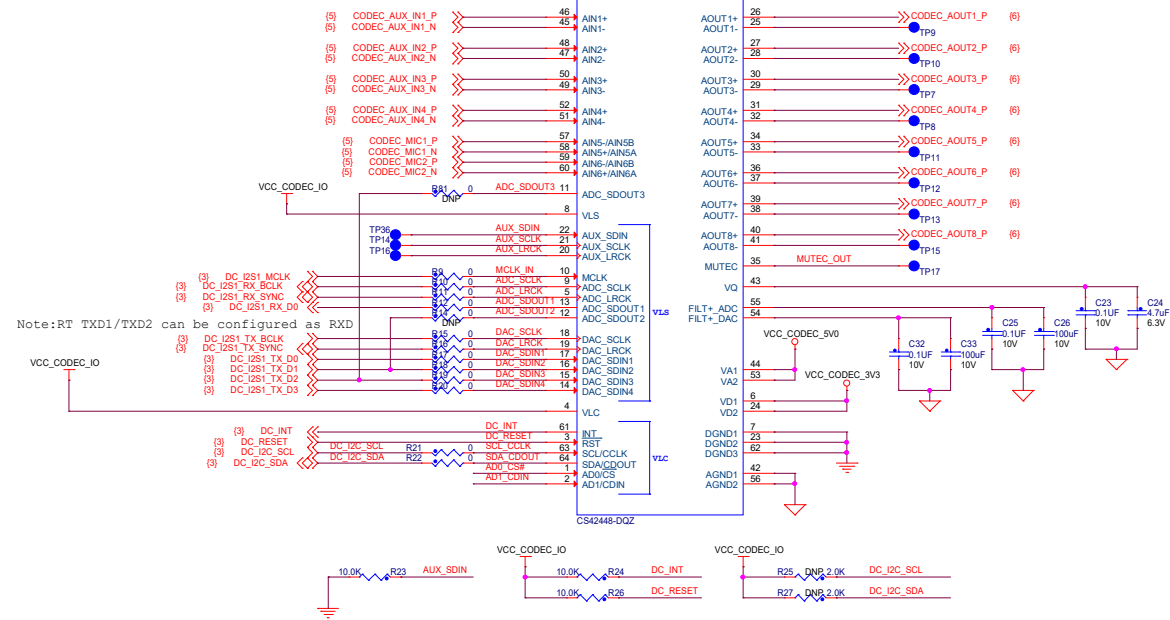


ICAP Classification:		CP:	IUC: X	PUBI:
Drawing Title:				
<b>AUD-EXP-42448</b>				
Page Title:				
<b>POWER&amp;INTERFACE</b>				
Size C	Document Number			
	SCH-48012, PDF: SPF-48012			
Date:	Friday, March 26, 2021		Sheet	3 of 6

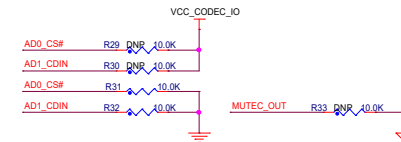
## Audio Codec Power&GND



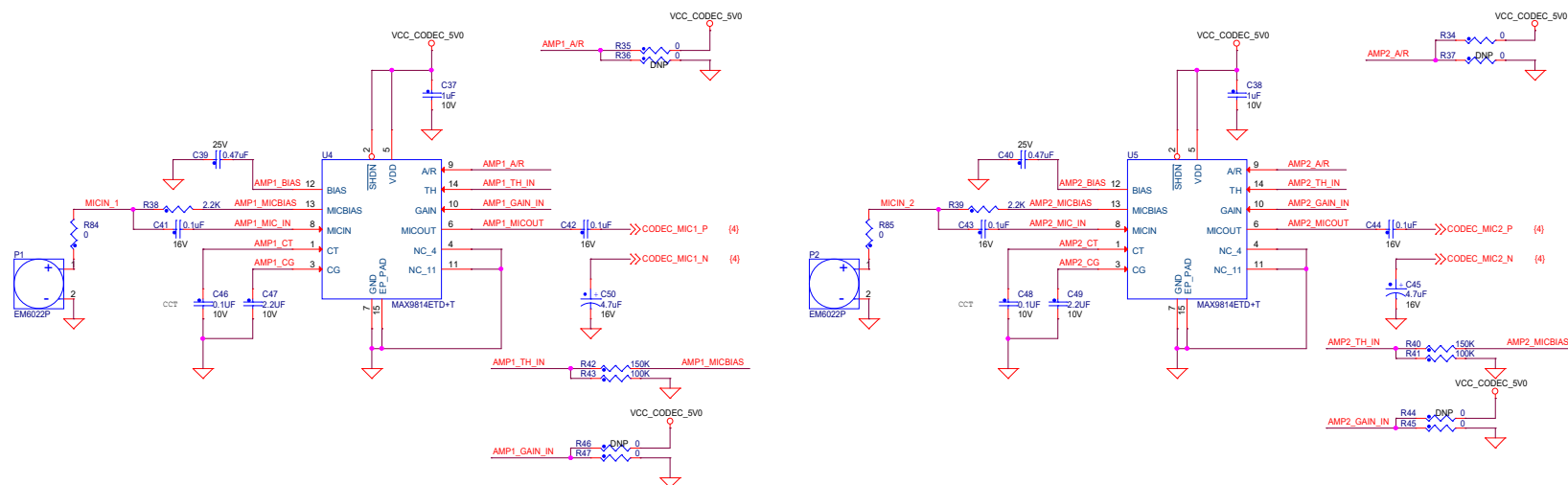
## Audio Codec



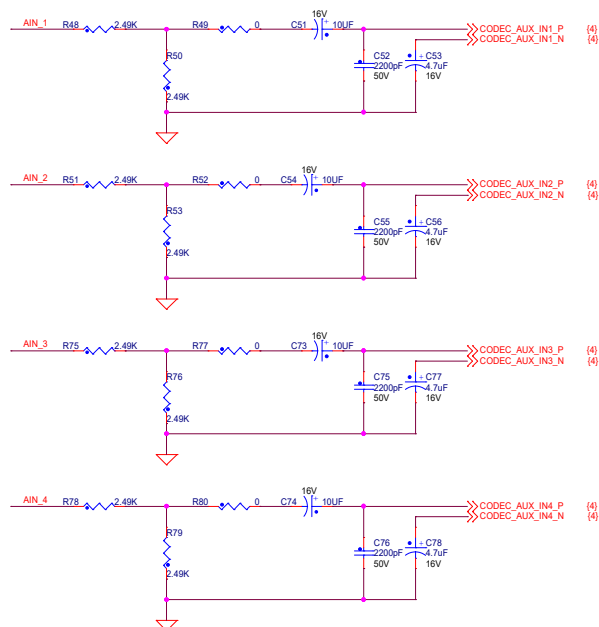
## I2C Address Config



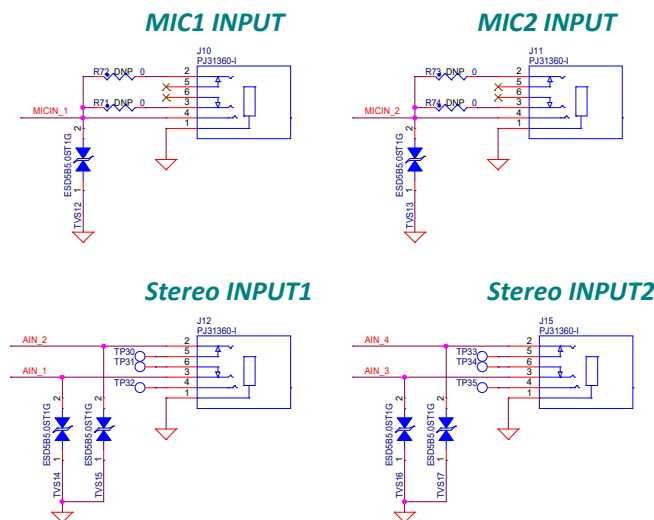
# Audio Input Amplifiers



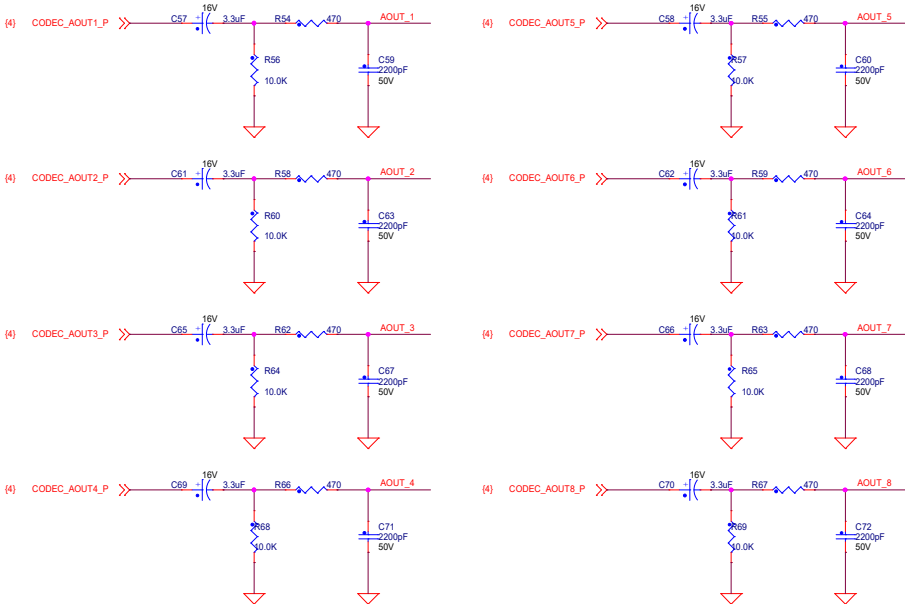
# Auxiliary Audio Input Filter



# Input TRS Connectors



# Audio Output Filters



# Output TRS Connectors

