

# S32K148EVBQ144/Q176

## C U S T O M E R   E V B

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Revisions				
Rev	Description	Designer	Date	Approved
X4	Schematic	J.Sanchez		
A	Prototype			
B	First Release			

### CAUTION :

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3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

 TPV?

 TPH5

 TP?


### Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

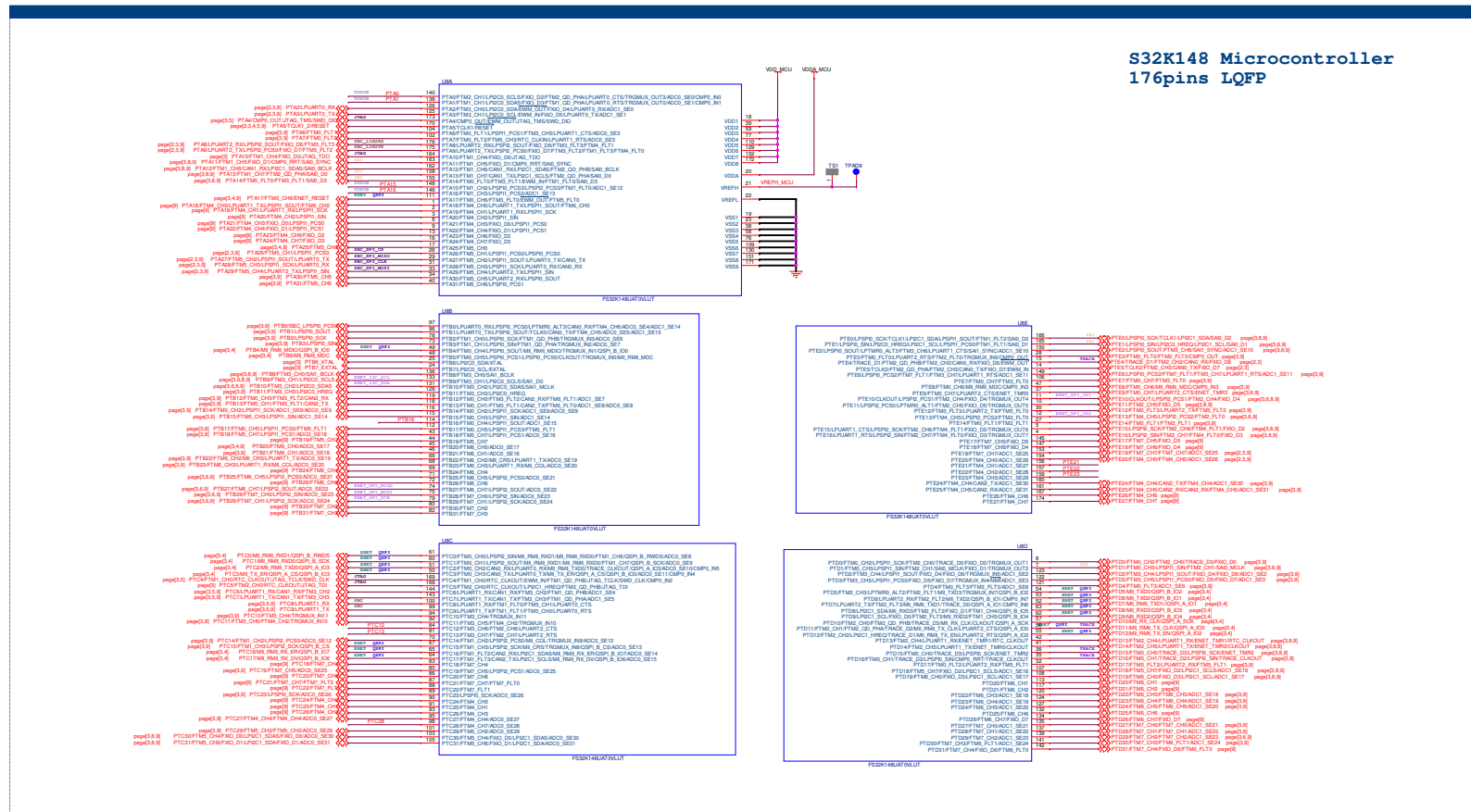
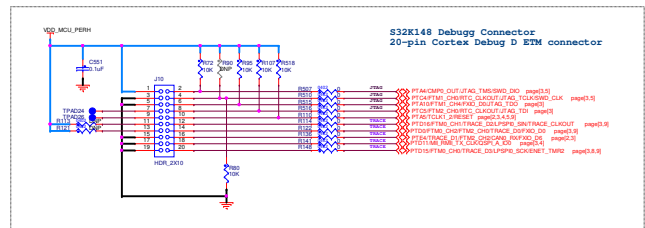
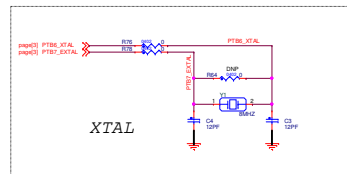
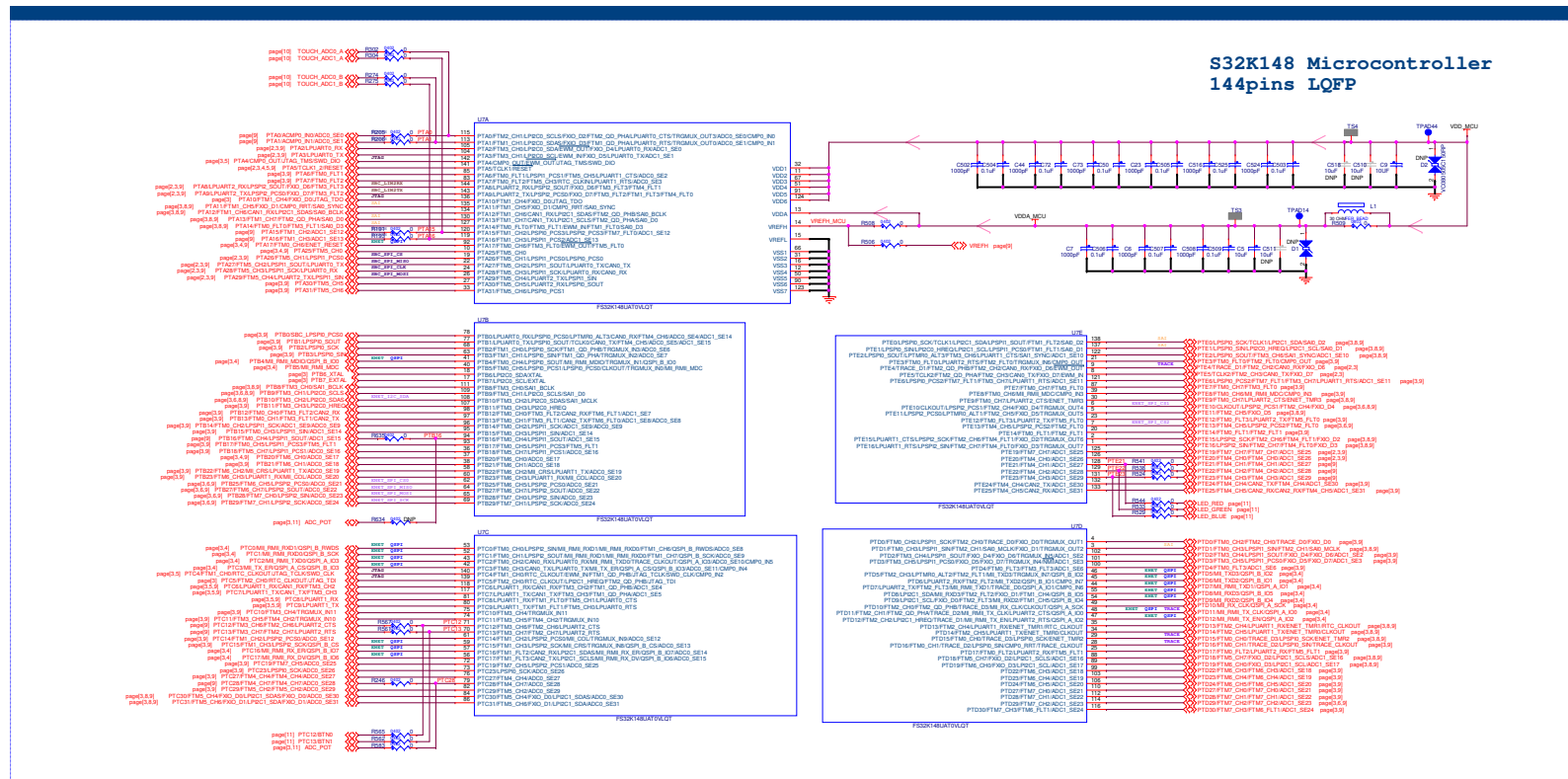
Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

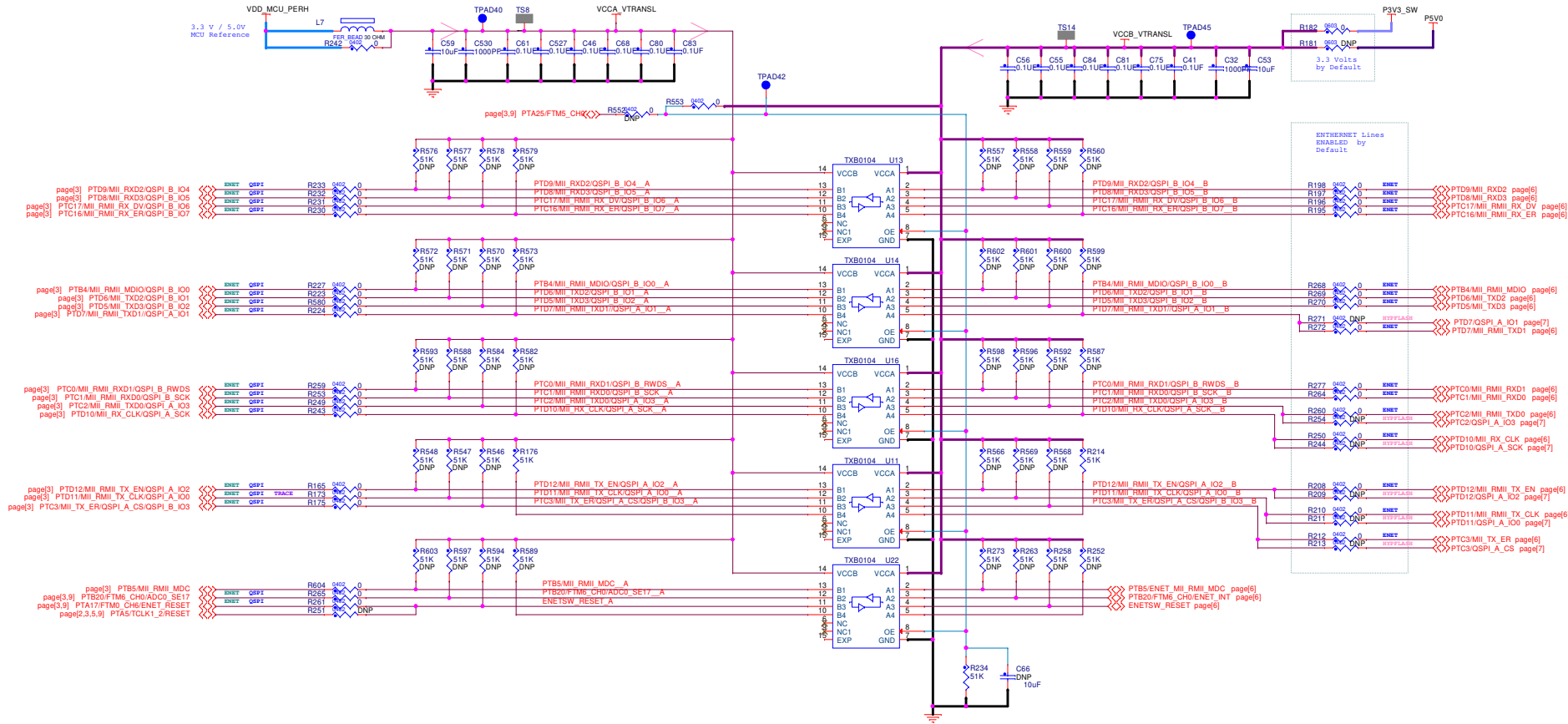
Specific PCB LAYOUT notes are detailed in ITALICS

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Drawn by: Jesus Sanchez		Page Title: <b>TITLE</b>		
Approved: Juan Romero	Size B	Document Number SCH-29642 PDF: SPF-29642		Rev B
Date:    Friday, February 02, 2018		Sheet    1    of    11		






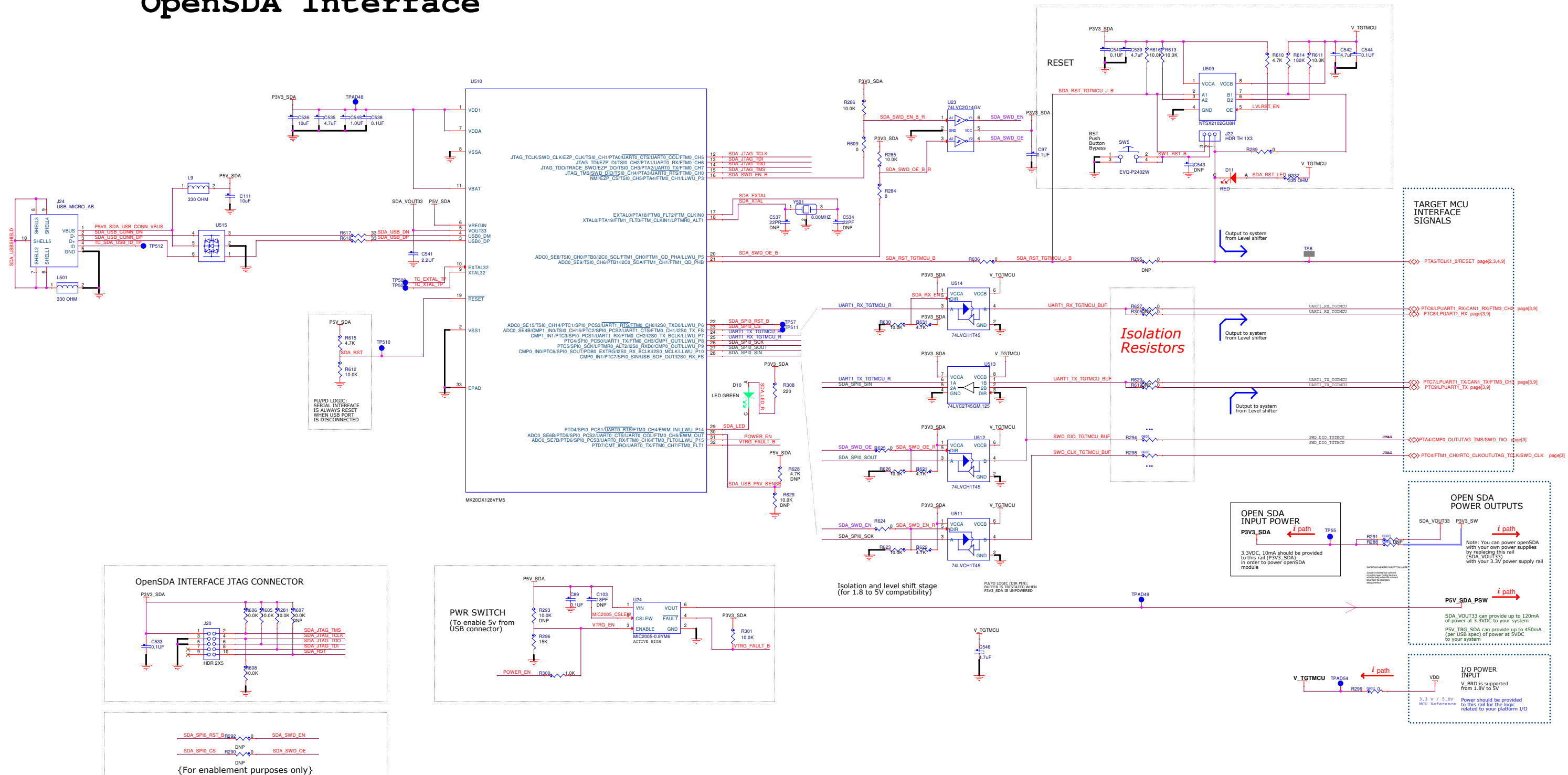
S32K148  
MCU SIGNALS



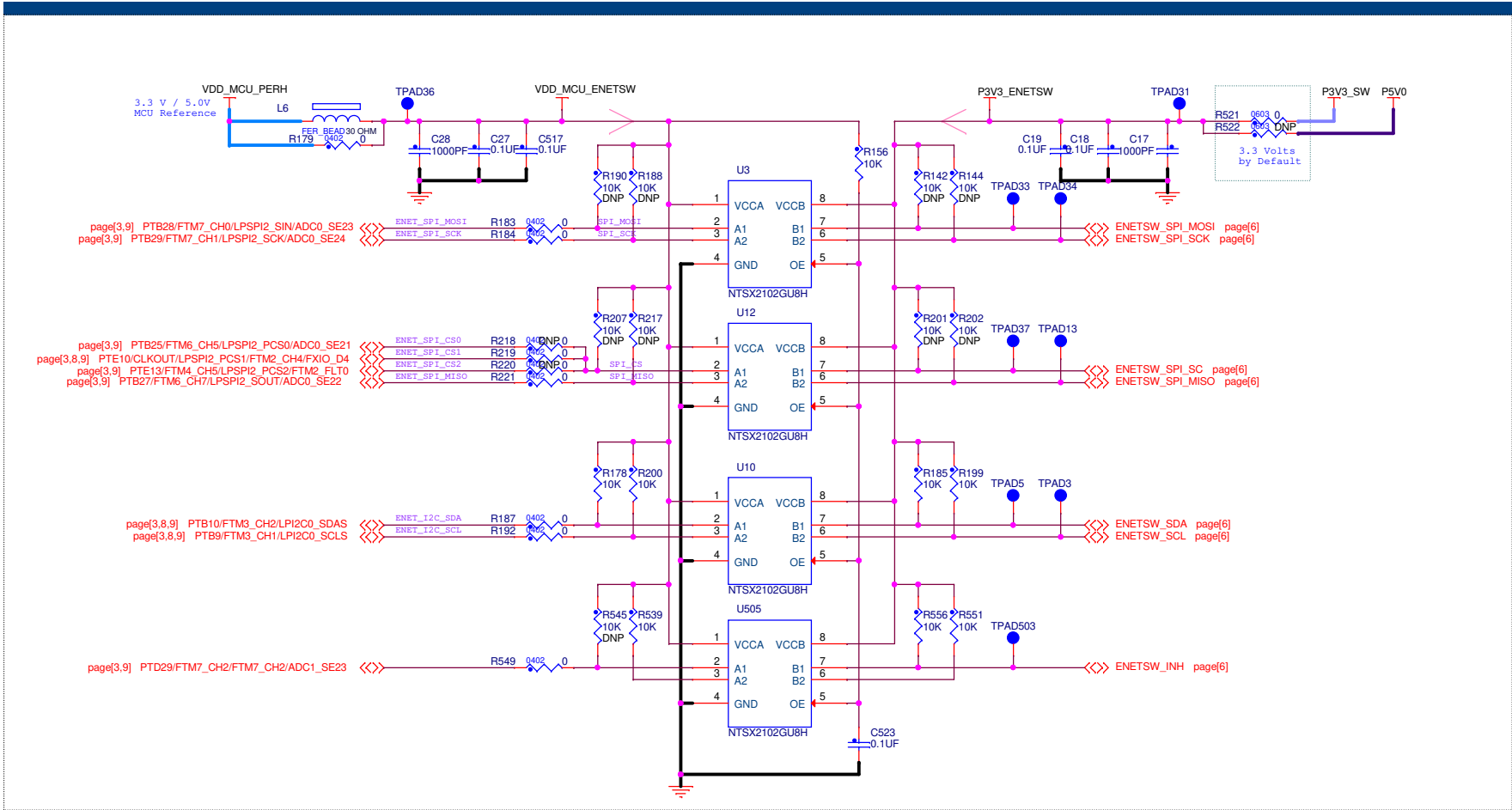
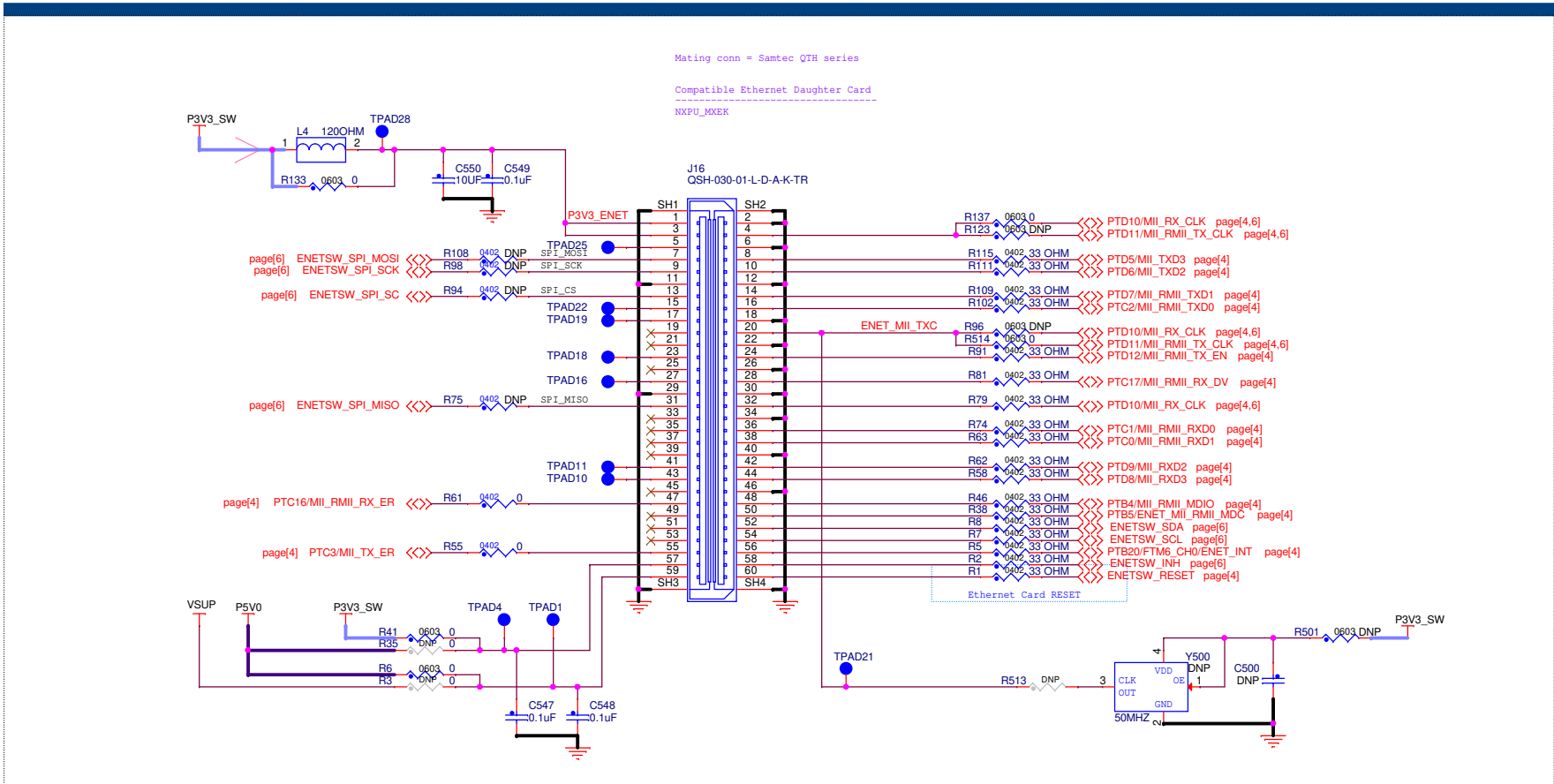
HyperFLASH &  
Ethernet Connector


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## OpenSDA Interface

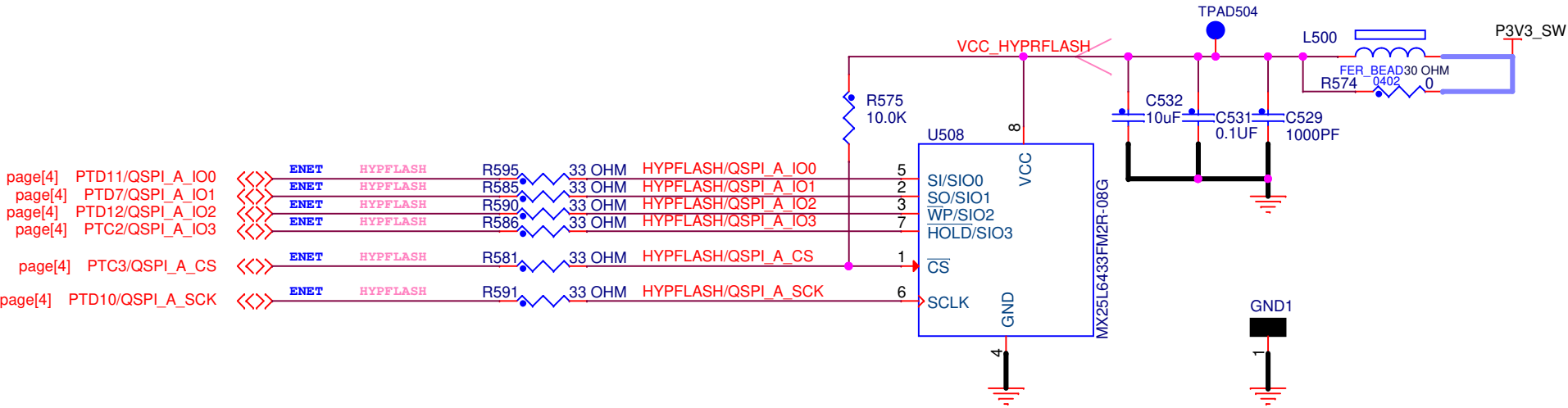







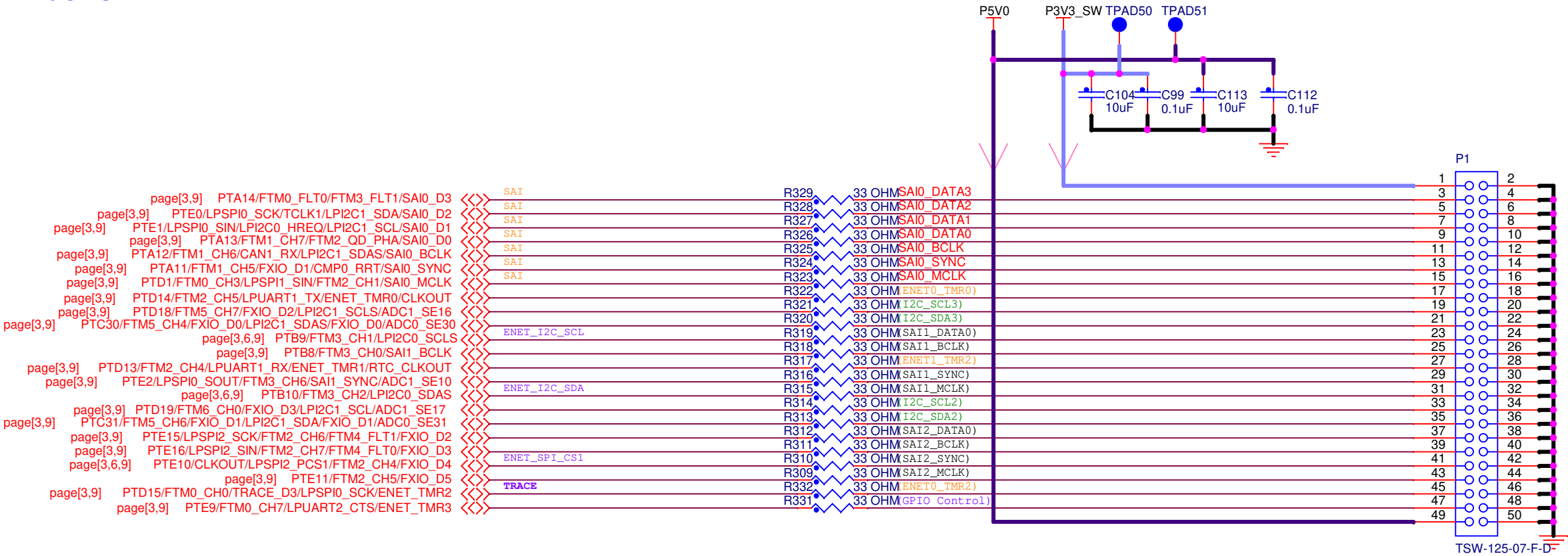
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CMOS FLASH Memory 64M-BIT



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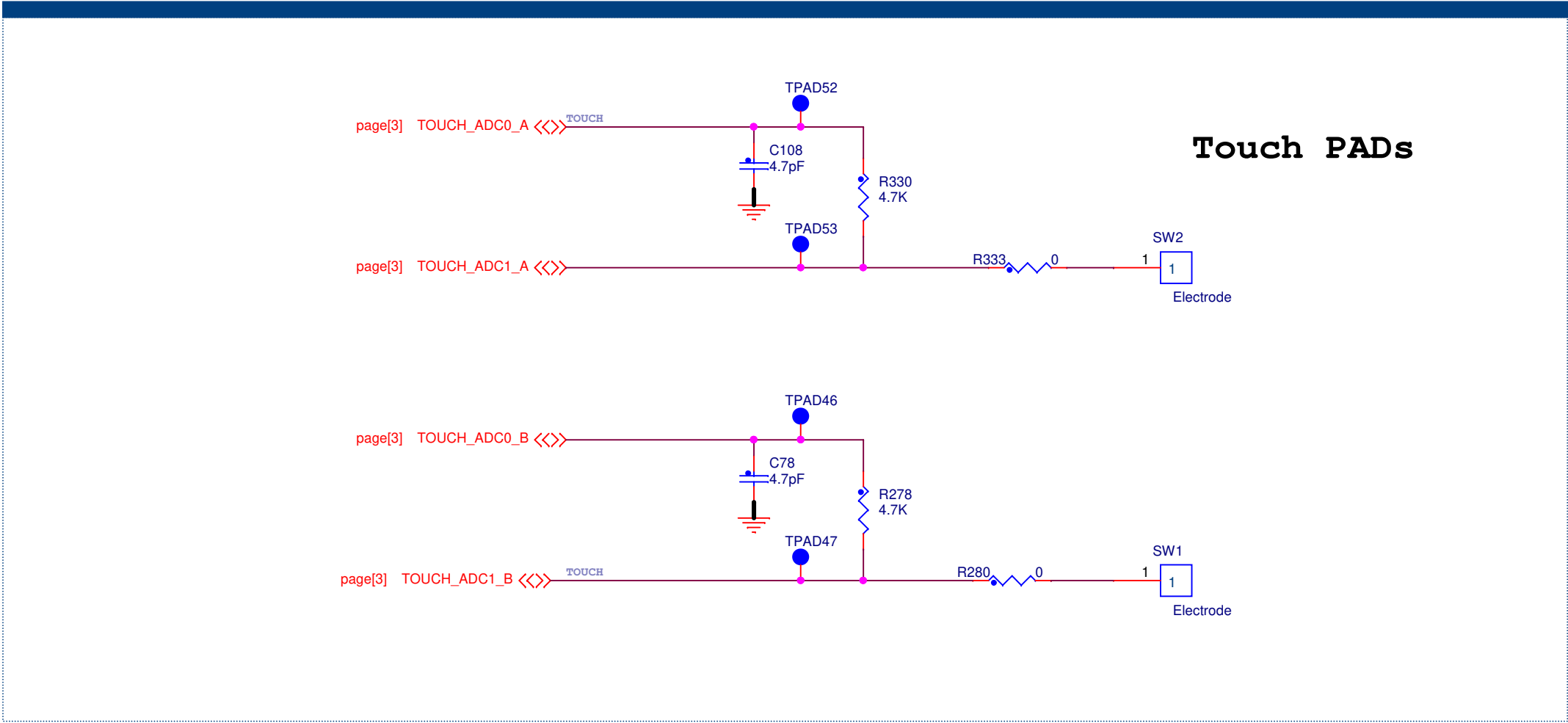
SAI Audio




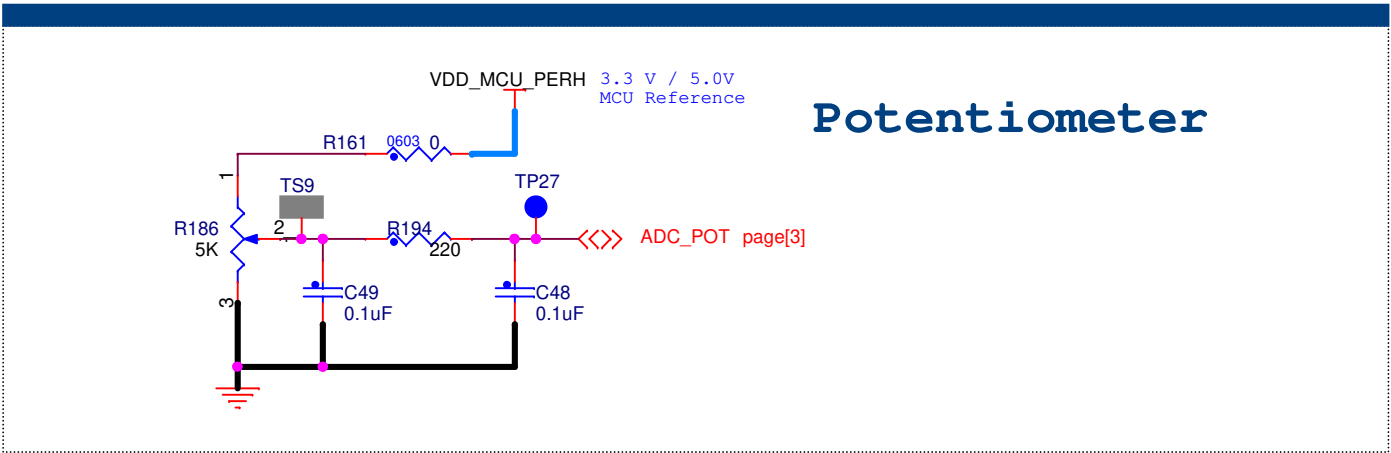
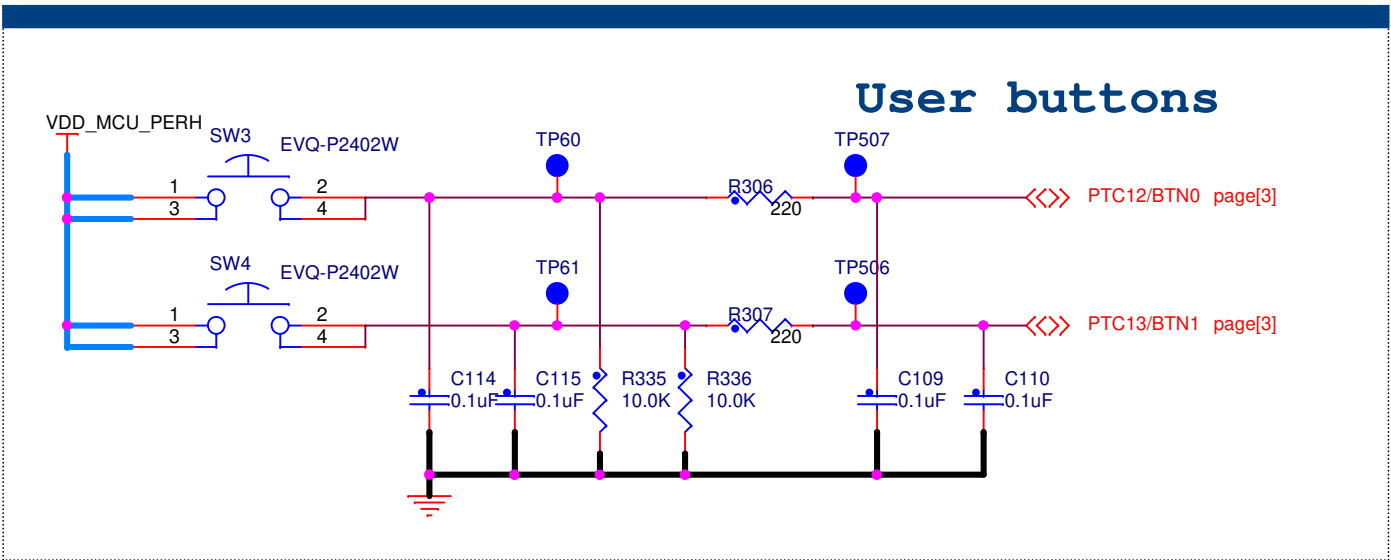
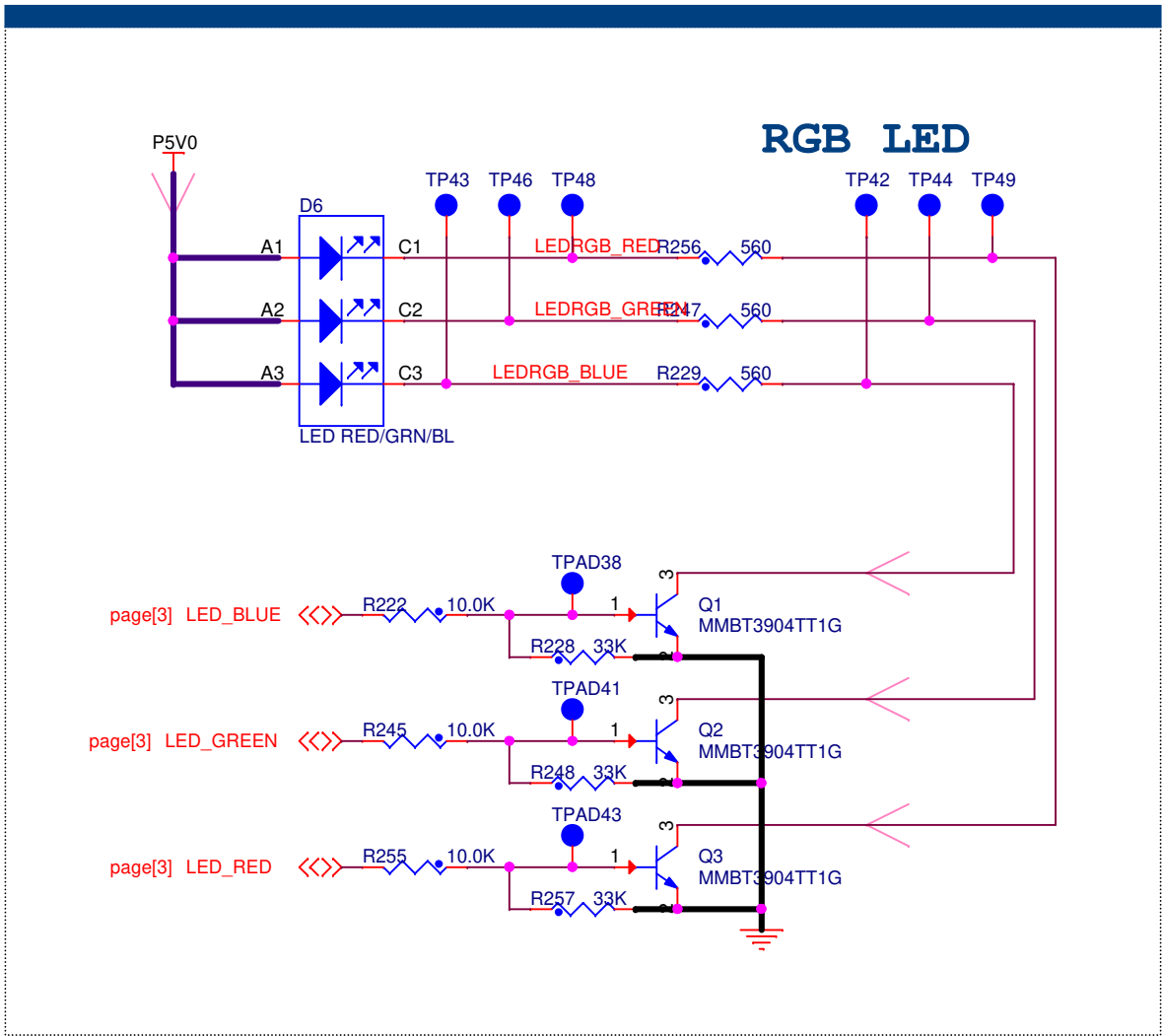
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