AN14509

如何在MCX MCU上用SmartMDA实现MDIO从接口

第1.0版—2024年11月29日 **应用笔记**

文档信息

信息	内容
关键词	AN14509、MDIO、SmartDMA、MCX N947
摘要	本应用笔记介绍了在MCX系列MCU上使用SmartDMA实现MDIO从接口的方法。

1 介绍

本应用笔记介绍了如何在MCX系列MCU上用SmartDMA来实现MDIO从接口。

本文包括MDIO接口的简介、一些相关功能与API例程的介绍，以及一个演示工程。在MCX N947中，配备了一个称为SmartDMA的协处理器，可用于实现MDIO从接口的功能。

性能如下：

SmartDMA可以使用高达150MHz的MCU系统时钟作为其时钟源。

1. 例如，当生成2kHz的PWM波形时，每周期的分辨率可达到16位。
2. 如果生成周期为40微秒的250kHz PWM波形，分辨率可达600个点（即40微秒除以150MHz的倒数），大约相当于全范围调谐的9位分辨率。

2 MDIO接口

管理数据输入/输出（Management Data Input/Output, MDIO）是IEEE 802.3以太网标准中为媒体独立接口（MII）定义的串行总线协议。MII将媒体访问控制（MAC）设备连接到以太网物理层（PHY）电路。MDIO 总线有两条信号线：管理数据时钟信号（MDC）和管理数据输入/输出信号（MDIO）。MDIO最初是在 IEEE 802.3 标准第22条中定义的。

以下是相关时序的介绍。

2.1 管理帧结构

MII接口上传输的管理帧具有表1所示的帧结构。位传输顺序必须从左到右。

表1. 管理帧格式

	管理帧字段							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDD DDDDDD DDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDD DDDDDD DDDD	Z

2.1.1 PRE（前导码）

MDIO的IDLE状态是一种高阻态，此时所有三个状态驱动器均需禁用，PHY 的上拉电阻会将MDIO线路拉至逻辑1。在每次传输开始时，主设备会在MDIO上发送32个连续的逻辑1比特，并在MDC上对应32个时钟周期，以便为PHY提供一个建立同步所需的模式。在响应任何传输之前，PHY需检测到MDIO上的32个连续的逻辑1比特及其在MDC上相应的32个时钟周期。

如果主设备（STA）判定连接到MDIO信号的所有PHY均能接受不带前导码模式的管理帧，则STA可以抑制前导码生成的模式，并直接以ST（帧起始）模式启动管理帧。

2.1.2 ST（帧起始）

帧起始由<01>模式表示。该模式确保从默认的逻辑1状态转变为0，然后再返回至逻辑1。

2.1.3 OP（操作码）

读取事务的操作码为<10>，写入事务的操作码为<01>。

2.1.4 PHYAD（PHY地址）

PHY地址为一个5比特字段，可支持最多32个唯一的PHY地址。传输和接收的第一个PHY地址位是地址的MSB。通过第22.6条定义的接口连接到主设备的PHY，会响应寻址到PHY地址零（<00000>）的事务。对于连接到多个PHY的情况，主设备需要预先知道每个PHY的具体地址。

2.1.5 REGAD（寄存器地址）

读传输的操作代码是<10>，而写传输的操作代码是<01>。寄存器地址为一个5比特的字段，在每个PHY内部可寻址最多32个寄存器。发送和接收的第一个寄存器地址位为该地址的MSB。

2.1.6 TA（转换时间）

每个帧的开始由<01>码型标识。该码型通过从默认的逻辑1状态切换到零状态，再返回逻辑1状态来保证发生变化。此转换时间是管理帧中的寄存器地址字段和数据字段之间的2位间隔，以避免在读传输期间发生竞争。对于读传输，STA和PHY在转换的第一个比特位时间内都处于高阻态，而在第二个比特位的时间里，PHY会输出一个0信号。对于写传输，STA在转换的第一个比特位时间输出1，在第二个比特位时间输出0。

2.1.7 DATA（数据）

数据字段的长度为16位，发送和接收的第一个数据位必须为所寻址寄存器的第15位。

2.2 第45条

为了满足10千兆以太网设备日益增长的需求，802.3ae规范引入了第45条。第45条增加了对低至1.2V的低压设备的支持，并扩展了帧格式，以提供对更多设备和寄存器的访问功能。

表2列出了时序方面的差异。

表2. 时序差异

条款	ST（帧开始）	OP代码	16位ADDRESS/DATA
第22条	第22条为0b01	0b01：写 0b10：读	写：写入数据 读：读取数据
第45条	第45条为0b00	0b00：读写地址 0b01：写 0b11：读	地址：寄存器地址 写：写入数据 读：读取数据

表2. 时序差异（续）

条款	ST（帧开始）	OP代码	16位ADDRESS/DATA
		0b10：读取增量	读：增加读取数据

图1所示为帧结构（OP为读写地址）。

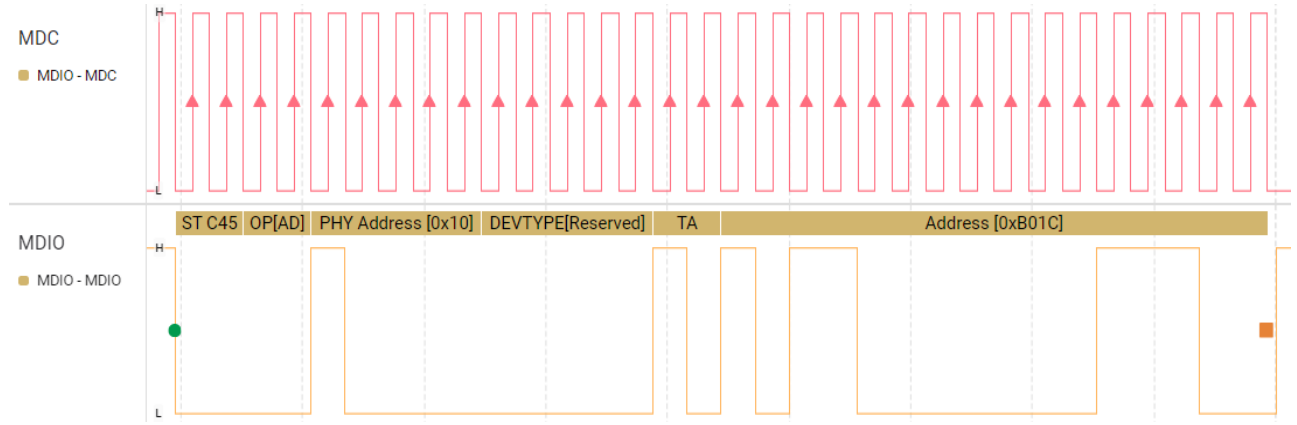

图1. 帧结构

3 将SmartDMA用于MDIO

SmartDMA是MCX MCU中的一个协处理器单元，它能够执行精简指令集。它可以在单个时钟周期内访问GPIO，并能够将GPIO输入信号作为触发源。当MDC时钟信号上升时，SmartDMA能够同步捕获MDIO数据信号的值；当MDC时钟信号下降时，SmartDMA可以传输MDIO数据的信号电平。此外，SmartDMA还可以设置内部超时信号，以防止出现总线挂起的问题。

3.1 SmartDMA的配置

与其他外设一样，SmartDMA还具备复位、时钟和中断等功能。在`SMARTDMA_InitWithoutFirmware()`函数中启用SmartDMA的时钟。

为了便于用户更方便地使用SmartDMA函数，本应用将SmartDMA代码封装到一个数组中，并提供一些可供用户直接调用的API函数。

SmartDMA代码封装后需要在地址为`0x4000000`的SRAMX处运行。因此，在运行SmartDMA代码之前，用户必须首先使用`SMARTDMA_InstallFirmware()`函数将数组传输到`0x4000000`地址处。SmartDMA支持中断功能，当中断发生时会执行回调函数。用户可以使用`SMARTDMA_InstallCallback()`函数设置回调函数。此外，用户还可以使用`EnableIRQWithPriority()`函数启用SmartDMA中断并设置中断优先级。`SMARTDMA_Boot()`函数是SmartDMA的启动函数，用户可通过设置smartdmaParam来传递参数。

3.2 SmartDMA参数的设置

参数包括两部分内容：SmartDMA操作所用的堆栈和MDIO寄存器的设置。表3列出了MDIO寄存器的具体设置。

设置MDIO寄存器的目的是：

- 获取总线上的信息，包括操作码、PHY地址、DEV地址、数据以及内存地址。

- 用户可以设置MDIO的PHY地址和DEV地址，并启用相关中断，如帧完成中断。

表3. MDIO寄存器的设置

偏移值	寄存器	功能	偏移值	寄存器	功能
0x0	RXOPCODE	接收操作码	0x40	MEM0ADDR	存储器0地址
0x4	RXPHYADD	接收PHY地址	0x44	MEM1ADDR	存储器1地址
0x8	RXDEVADD	接收DEV地址	0x48	MEM2ADDR	存储器2地址
0xc	RXDAT	接收数据	0x4c	MEM3ADDR	存储器3地址
0x10	RXMEMADD	接收内存地址	0x50	MEM4ADDR	存储器4地址
0x14	ADDINC	地址增加	0x54	MEM0SIZE	存储器0大小
0x18	SETPHYADD	待设置的PHY地址	0x58	MEM1SIZE	存储器1大小
0x1c	SETDEVADD	待设置的DEV地址	0x5c	MEM2SIZE	存储器2大小
0x20	STA	状态	0x60	MEM3SIZE	存储器3大小
0x24	INTEN	启用中断	0x64	MEM4SIZE	存储器4大小
0x28	TIMERADDR	超时定时器	0x68	MEM0ZONE	存储器0区域
0x2c	MDIODEBUG	调试缓冲区	0x6c	MEM1ZONE	存储器1区域
0x30	RESERVED	已保留	0x70	MEM2ZONE	存储器2区域
0x34	RESERVED	已保留	0x74	MEM3ZONE	存储器3区域
0x38	RESERVED	已保留	0x78	MEM4ZONE	存储器4区域
0x3c	RESERVED	已保留	0x7c	RESERVED	已保留

3.3 结构框图

图2所示为MCXN947中实现的MDIO模块框图。SmartDMA执行SRAMX中的代码，操作GPIO，并将MDIO数据从RAM发送至主设备。如果主设备执行的是读操作，SmartDMA可将数据发送出去。

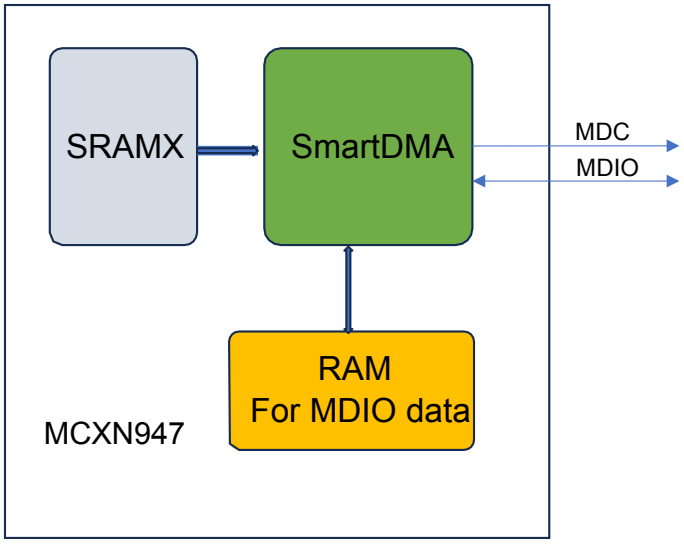

图2. 结构框图

3.4 特性

在本应用中，SmartDMA实现了MDIO从设备的功能，它具有以下特性：

- 用户可以配置PHY地址、设备地址和内存块的定义。
- 用户可以接收当前帧的操作码、PHY地址和设备地址。
- 用户可以启用帧完成中断。
- 从设备可接收高达4MHz的MDC时钟数据。
- 数据的接收与发送完全不需要Arm内核的参与。

4 演示

此演示使用两块FRDM-MCXN947开发板实现MDIO通信。

4.1 MDIO主设备代码

MCX N947的以太网接口具备MDIO主设备功能。用户可通过相应SDK中名为“txrx_rxpoll”的示例程序来演示MDIO主设备功能。示例代码路径为*SDK_2_16_000_FRDM-MCXN947\boards\frdmmcxn947\driver_examples\enet\txrx_rxpoll*。

部分重要的代码例程如下：

```
static void MDIO_Init(void)
{
    (void)CLOCK_EnableClock(s_enetClock[ENET_GetInstance(EXAMPLE_ENET_BASE)]);
    EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS = ENET_MAC_MDIO_ADDRESS_CR(0);
}

static status_t MDIO_Write(uint8_t phyAddr, uint8_t devAddr,uint16_t regAddra,
 uint16_t data)
{
    uint32_t reg = EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS &
 ENET_MAC_MDIO_ADDRESS_CR_MASK;

    /* Build MII write command. */
    EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS =
        reg | ENET_MAC_MDIO_ADDRESS_GOC_0(1) | ENET_MAC_MDIO_ADDRESS_PA(phyAddr)
 | ENET_MAC_MDIO_ADDRESS_RDA(devAddr)| ENET_MAC_MDIO_ADDRESS_C45E(1);
    EXAMPLE_ENET_BASE->MAC_MDIO_DATA =  (regAddra << 16) | data;
    EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS |= ENET_MAC_MDIO_ADDRESS_GB_MASK;


    while (((EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS &
 ENET_MAC_MDIO_ADDRESS_GB_MASK) != 0U))
    {
    }

}

static status_t MDIO_Read(uint8_t phyAddr, uint8_t devAddr, uint16_t regAddr,
 uint16_t *pData)
{
    uint32_t reg = EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS &
 ENET_MAC_MDIO_ADDRESS_CR_MASK;

    /* Build MII read command. */
```

```
    EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS = reg | ENET_MAC_MDIO_ADDRESS_GOC_0(1) |
 ENET_MAC_MDIO_ADDRESS_GOC_1(1) |
                              ENET_MAC_MDIO_ADDRESS_PA(phyAddr) |
 ENET_MAC_MDIO_ADDRESS_RDA(devAddr)| ENET_MAC_MDIO_ADDRESS_C45E(1);
    EXAMPLE_ENET_BASE->MAC_MDIO_DATA =  (regAddr << 16);

    EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS |= ENET_MAC_MDIO_ADDRESS_GB_MASK;
    while (((EXAMPLE_ENET_BASE->MAC_MDIO_ADDRESS &
 ENET_MAC_MDIO_ADDRESS_GB_MASK) != 0U))
    {
    }

    *pData = (EXAMPLE_ENET_BASE->MAC_MDIO_DATA & ENET_MAC_MDIO_DATA_GD_MASK);

}
```

执行示例代码如下所示：

```
MDIO_Init();
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
  MDIO_Write(0x10, 0x20, 0x8000+i, i);
  SDK_DelayAtLeastUs(10, SystemCoreClock);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
  MDIO_Write(0x10, 0x20, 0x9000+i, i+0x100);
  SDK_DelayAtLeastUs(10, SystemCoreClock);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
  MDIO_Write(0x10, 0x20, 0xa000+i, i+0x200);
  SDK_DelayAtLeastUs(10, SystemCoreClock);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
  MDIO_Write(0x10, 0x20, 0xb000+i, i+0x300);
  SDK_DelayAtLeastUs(10, SystemCoreClock);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
        MDIO_Read(0x10, 0x20,  0x8000+i, &g_rec_data);
        PRINTF("addr:0x%4x,RxD:0x%4x.\r\n",0x8000+i,g_rec_data);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
        MDIO_Read(0x10, 0x20,  0x9000+i, &g_rec_data);
        PRINTF("addr:0x%4x,RxD:0x%4x.\r\n",0x9000+i,g_rec_data);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
        MDIO_Read(0x10, 0x20,  0xa000+i, &g_rec_data);
        PRINTF("addr:0x%4x,RxD:0x%4x.\r\n",0xa000+i,g_rec_data);
    }
    for(uint32_t i = 0; i < 8*4; i = i+4)
    {
        MDIO_Read(0x10, 0x20,  0xb000+i, &g_rec_data);
        PRINTF("addr:0x%4x,RxD:0x%4x.\r\n",0xb000+i,g_rec_data);
    }
```

4.2 MDIO从设备代码

对于MDIO从设备，其主要功能由SmartDMA实现。用户主要的工作是提供寄存器配置参数，正确启动SmartDMA，处理引脚初始化和做好中断处理。

重要的例程如下：

```
   INPUTMUX_Init(INPUTMUX0);
    /* CTIMER4_CH3 is selected for SMARTDMA arch B 0 */
    INPUTMUX_AttachSignal(INPUTMUX0, 0U, kINPUTMUX_Ctimer4M3ToSmartDma);

    PRINTF("MCXN947 SmartDMA MDIO Demo.\r\n");
    memset((void *)&g_mdio_registers, 0, sizeof(g_mdio_registers));
    memset((void *)g_mdio_mem0, 0x0, sizeof(g_mdio_mem0));
    memset((void *)g_mdio_mem1, 0x0, sizeof(g_mdio_mem1));
    memset((void *)g_mdio_mem2, 0x0, sizeof(g_mdio_mem2));
    memset((void *)g_mdio_mem3, 0x0, sizeof(g_mdio_mem3));
    g_mdio_registers.SETPHYADD = 0x10;
    g_mdio_registers.SETDEVADD = 0x0;
    g_mdio_registers.TIMERADDR  =(uint32_t)&CTIMER4_PERIPHERAL->TCR;
    g_mdio_registers.MDIODEBUG = (uint32_t)g_mdio_debug;
    g_mdio_registers.MEM0ADDR =(uint32_t)g_mdio_mem0;
    g_mdio_registers.MEM0SIZE = MEM0_SIZE;
    g_mdio_registers.MEM0ZONE = MEM0_ZONE;
    g_mdio_registers.MEM1ADDR =(uint32_t)g_mdio_mem1;
    g_mdio_registers.MEM1SIZE = MEM1_SIZE;
    g_mdio_registers.MEM1ZONE = MEM1_ZONE;
    g_mdio_registers.MEM2ADDR =(uint32_t)g_mdio_mem2;
    g_mdio_registers.MEM2SIZE = MEM2_SIZE;
    g_mdio_registers.MEM2ZONE = MEM2_ZONE;
    g_mdio_registers.MEM3ADDR =(uint32_t)g_mdio_mem3;
    g_mdio_registers.MEM3SIZE = MEM3_SIZE;
    g_mdio_registers.MEM3ZONE = MEM3_ZONE;
    g_mdio_registers.INTEN   = (1<<0);
    PRINTF("g_mdio_registers.MEM0ADDR:0x%8x\r\n", g_mdio_registers.MEM0ADDR);
    PRINTF("g_mdio_registers.MEM1ADDR:0x%8x\r\n", g_mdio_registers.MEM1ADDR);
    PRINTF("g_mdio_registers.MEM2ADDR:0x%8x\r\n", g_mdio_registers.MEM2ADDR);
    PRINTF("g_mdio_registers.MEM3ADDR:0x%8x\r\n", g_mdio_registers.MEM3ADDR);

    /* Initialize components */
    SMARTDMA_InitWithoutFirmware();
    SMARTDMA_InstallFirmware(SMARTDMA_MDIO_MEM_ADDR,s_smartdmaMDIOFirmware,
SMARTDMA_MDIO_FIRMWARE_SIZE);
    SMARTDMA_InstallCallback((smartdma_callback_t)SMARTDMA_Callbck, NULL);
    EnableIRQWithPriority(SMARTDMA_IRQn, 3);
    smartdmaParam.smartdma_stack = (uint32_t*)g_samrtdma_stack;
    smartdmaParam.p_registers_base_address = (uint32_t *)&g_mdio_registers;
    SMARTDMA_Boot(kSmartDMA_MDIO_Slave, &smartdmaParam, 0x2);
```

4.3 硬件准备工作

本应用需要两块FRDM-MCXN947开发板来实现MDIO通信，其中一块作为MDIO主设备，另一块作为MDIO从设备。两块开发板通过两个引脚和地接线进行连接。表4列出了硬件连接方式。

表4. 硬件连接

功能	MDIO主设备在FRDM-MCXN947开发板上的位置	MDIO从设备在FRDM-MCXN947开发板上的位置
MDIO	J1-1 (P3_16)	J1-1 (P3_16)
MDC	R191的Pad 1 (删除R191) (P1_20)	J8-10 (P1_0)
GND	J5-8 (GND)	J5-8 (GND)

图3是硬件连接的物理图。逻辑设备可以捕捉MDIO波形并分析数据格式。

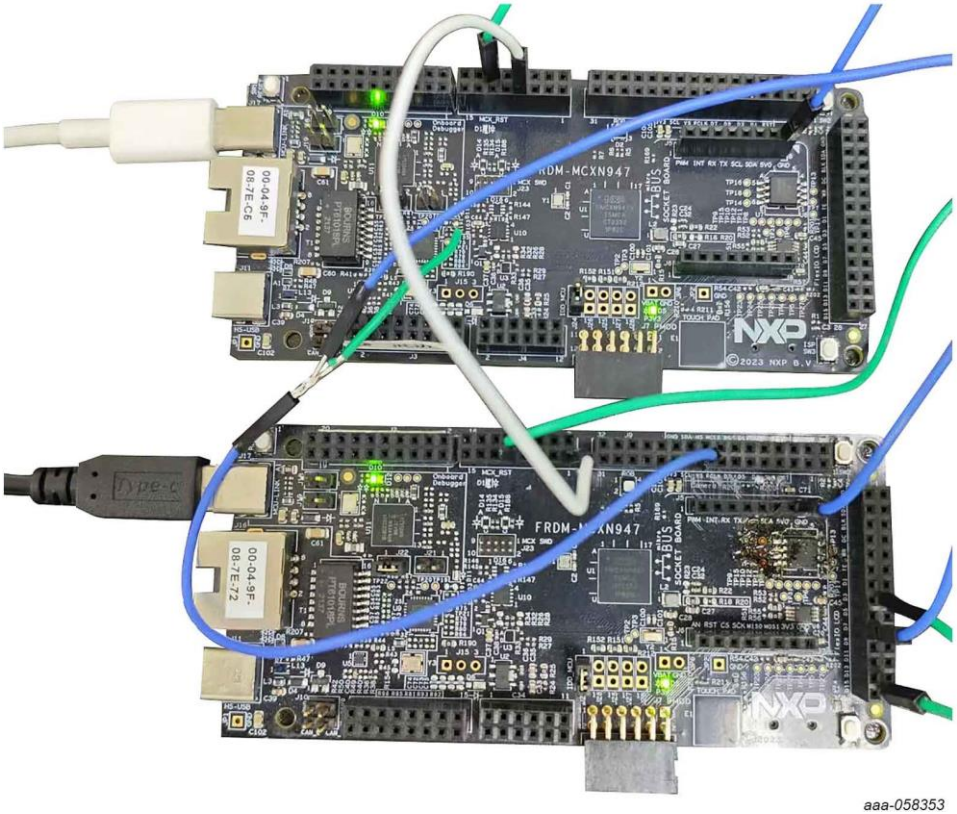

图3. 硬件连接的物理示意图

开发板：FRDM-MCXN947

逻辑设备：Saleae logic pro16

1. 采用USB线缆将逻辑分析仪连接到个人电脑，并将逻辑分析仪的引脚连接到MDIO信号线上。
2. 采用USB Type-C数据线将FRDM-MCXN947开发板连接到个人电脑。
3. 连接两块FRDM-MCXN947开发板的信号引脚。

4.4 软件准备工作

按照以下步骤导入MDIO主设备代码SDK示例`txrx_rxpoll`，并将固件下载到主板。解压附件中的MDIO从设备的代码工程，并用MCUXpresso IDE打开。

1. 在IDE中导入工程。
2. 编译工程代码。

3. 下载固件。

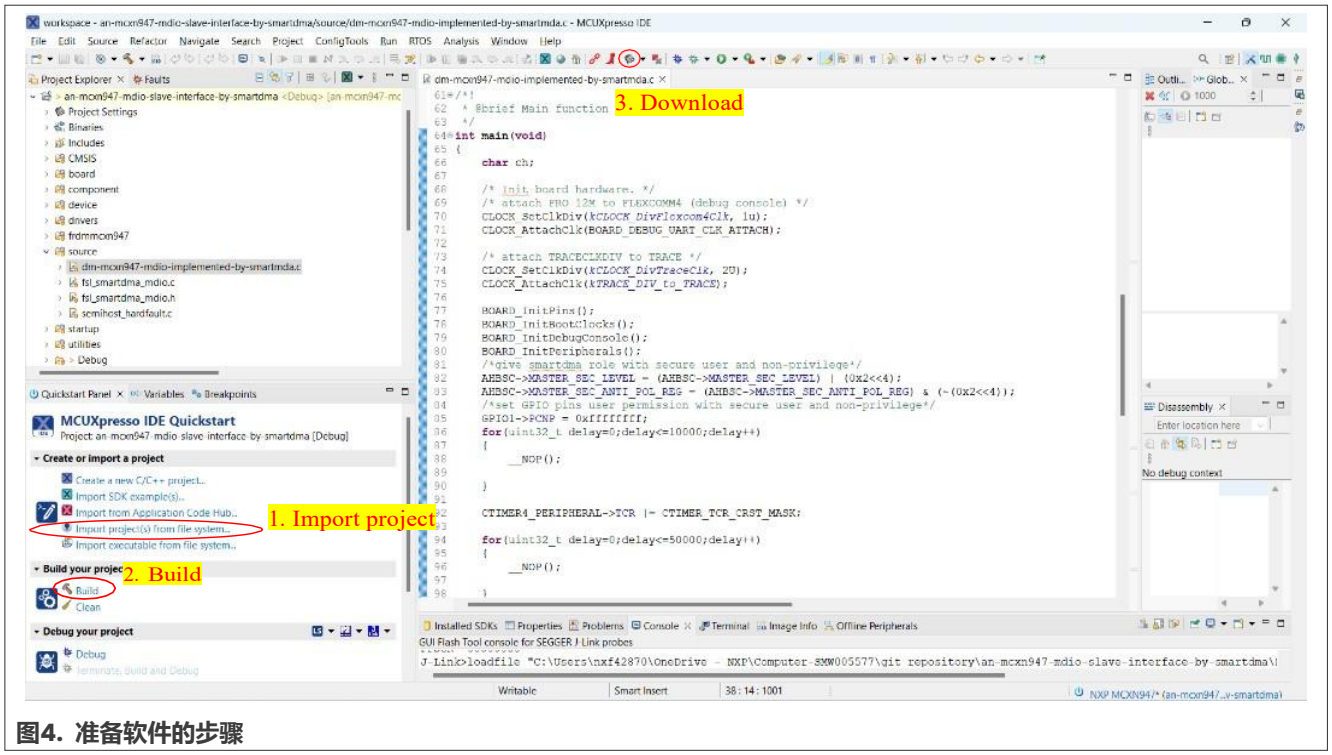

图4. 准备软件的步骤

4.5 结果

1. 打开连接至MDIO主设备串口的PC主机串口软件，然后复位开发板。
2. 启动逻辑分析仪软件工具。
3. 按以下顺序复位演示板：首先复位MDIO从设备板，然后复位MDIO主设备板。
4. 此时，可以查看MDIO主板打印出以下串行日志内容：
   - addr:0x8000,RxD:0x 0.
   - addr:0x8004,RxD:0x 4.
   - addr:0x8008,RxD:0x 8.
   - addr:0x800c,RxD:0x c.
   - addr:0x8010,RxD:0x c.
   - addr:0x8014,RxD:0x c.
   - addr:0x8018,RxD:0x c.
   - addr:0x801c,RxD:0x 1c.
   - addr:0x9000,RxD:0x 1c.
   - addr:0x9004,RxD:0x 1c.
   - addr:0x9008,RxD:0x 108.
   - addr:0x900c,RxD:0x 10c.
   - addr:0x9010,RxD:0x 110.
   - addr:0x9014,RxD:0x 114.
   - addr:0x9018,RxD:0x 118.
   - addr:0x901c,RxD:0x 11c.
   - addr:0xa000,RxD:0x 200.
   - addr:0xa004,RxD:0x 204.

- addr:0xa008,RxD:0x 208.
- addr:0xa00c,RxD:0x 20c.
- addr:0xa010,RxD:0x 210.
- addr:0xa014,RxD:0x 214.
- addr:0xa018,RxD:0x 218.
- addr:0xa01c,RxD:0x 21c.
- addr:0xb000,RxD:0x 300.
- addr:0xb004,RxD:0x 304.
- addr:0xb008,RxD:0x 308.
- addr:0xb00c,RxD:0x 30c.
- addr:0xb010,RxD:0x 310.
- addr:0xb014,RxD:0x 314.
- addr:0xb018,RxD:0x 318.
- addr:0xb01c,RxD:0x 31c.

5. 可在逻辑分析仪软件工具上观察MDIO波形，如图5图6所示：

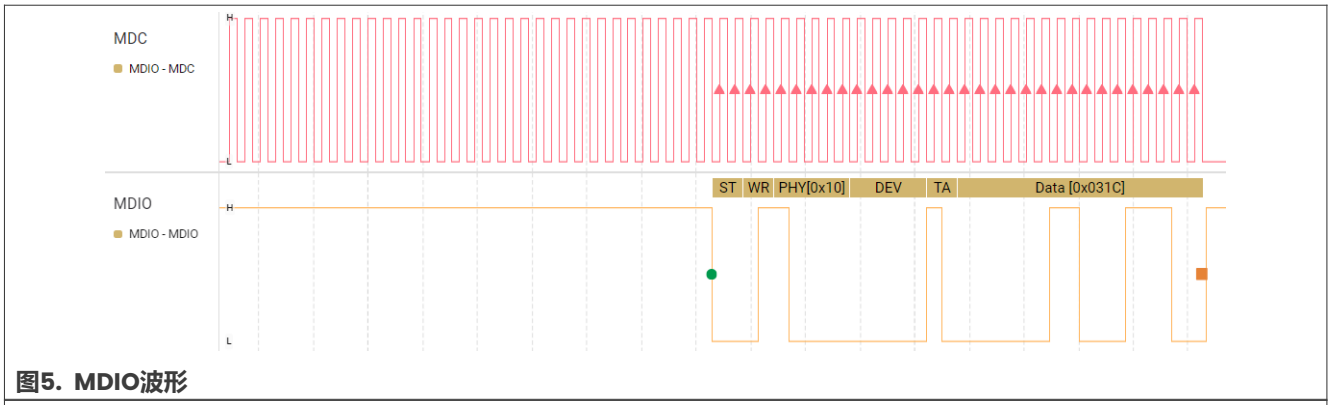

图5. MDIO波形

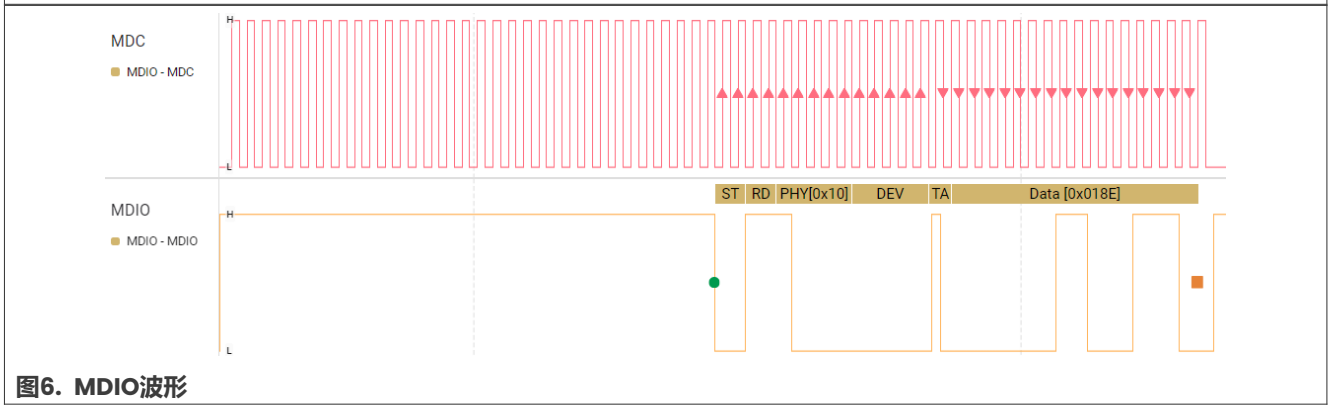

图6. MDIO波形

5 参考资料

- IEEE以太网标准（IEEE Std 802.3™-2018）
- CFP MSA管理接口规范v2.0
- CFP MSA硬件规范v1.4

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7 修订历史

表5汇总了本文档的修订情况。

表5. 修订历史

文档编号	发布日期	说明
AN14509 v.1.0	2024年11月29日	首次公开发布

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