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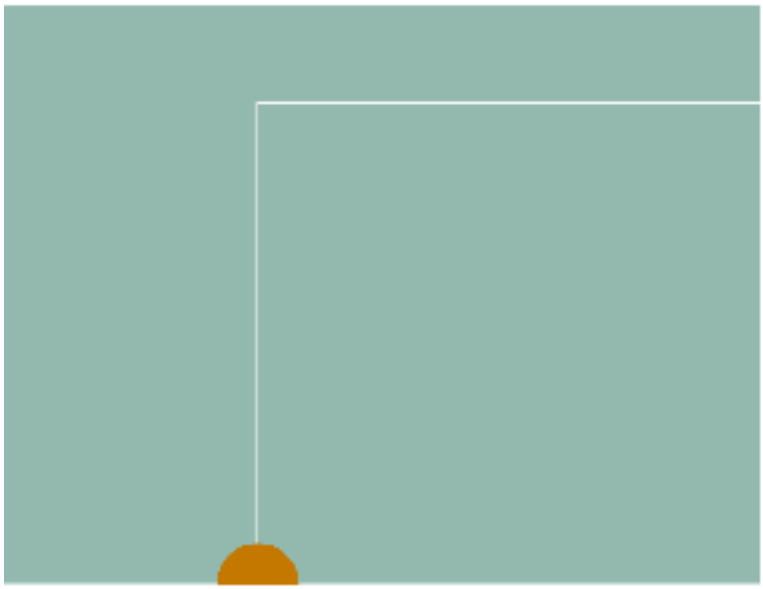
ADDRESSING MULTISERVICE ACCESS PLATFORM DESIGN ISSUES WITH NETWORK PROCESSORS



WHITE PAPER

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Network Processors

ABSTRACT

The past two years have been challenging for the multiservice switch market. Switch sales have dropped 23% from 2000 to 2002 (Cahners In-Stat/MDR - IN020214WN) due to service provider financial woes. During the late 1990s and early 2000, service provider networks were built out to accommodate the insatiable future demand of bandwidth. With the economy slow-down over the past two years, service providers began curbing their capital expenditures and only purchasing limited equipment to handle growth in traffic and customers, usually adding line cards to the existing network platforms versus adding new shelves or platforms. Their strategy was to leverage the existing network infrastructure as much as possible to maximize return on investment (ROI). The dilemma that service providers face now is how to add revenue-generating services and continue to add customers while keeping costs under control.

In addition to facing a challenging economic environment, the multiservice switch market has its own technological challenges. The market is diverse with single multiservice platforms accommodating a mixture of ATM, Frame Relay, IP, Multi-protocol Label Switching (MPLS), Packet over SONET (PoS), and Gigabit Ethernet. Interface speeds range from subT1/E1 to OC-3 to full-duplex OC-48c/STM-16 links. The multiservice switch must also be able to adapt to emerging applications such as packetized voice (VoIP) and 2.5G/3G wireless backbone networks. In addition, with converging applications (data/voice/video) come more extensive requirements for Quality of Service (QoS).

To address the economic realities and technical challenges network equipment manufacturers are seeking multiservice switch design solutions that answer these questions:

- How can I integrate with today's dominant technologies, such as ATM and Frame Relay, yet support the all IP contingency and whatever future technologies arise?
- How can I increase port density per-line card while maintaining power, space, and cost budgets?
- How can I implement fine-grained Quality of Service (QoS) to support greater service differentiation?
- How can I maximize hardware and software reuse to save development costs?
- How can I provide a smooth upgrade path for my customers to new services, higher bandwidths, greater port density, and continued technology integration?

One technology that is being used by network equipment manufacturers to help address the issues of multiservice switch design is the network processor. Network processors provide a programmable solution for the forwarding plane, enabling more flexible and scalable implementations. In addition, development time and costs are generally less as compared to the more traditional ASIC-based designs. It is helpful to review the evolution of the multiservice switch architecture to understand how network processors can play an important role in next-generation designs.

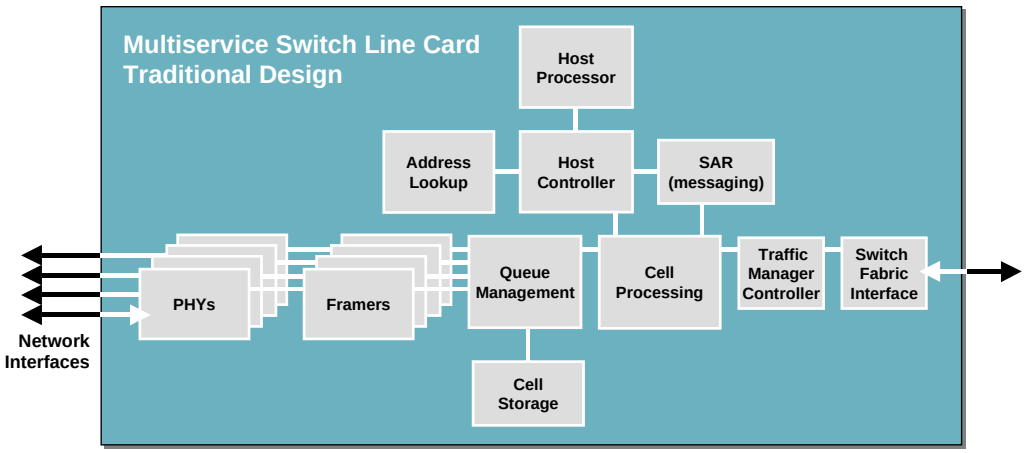
MULTISERVICE SWITCH ARCHITECTURE EVOLUTION

A multiservice switch is generally defined as a platform that can handle more than one protocol (usually ATM and Frame Relay, along with other protocols including IP, MPLS, PoS, Gigabit Ethernet, TDM, and legacy data) and can provide aggregation and bandwidth-efficient uplink capabilities. The traditional architecture of a multiservice switch is a rack or shelf with multiple flavors of line cards and one or more control processor cards — all connecting through a backplane interconnect or fabric. These line cards are usually dedicated to a specific service such as ATM, Frame Relay, TDM, or IP. Routing within the shelf across the system backplane or switch fabric provides interworking among the cards.

There are two general categories of processor cards: control processor cards and functional processor or line cards. The control processor card manages and controls applications supporting both system and networking functions. It provides shelf management functions, such as monitoring and alarm processing, and it connects to a network management system. The control processor card also interacts with the line cards, providing common services. Redundancy is implemented by adding another control processor card. Line cards are responsible for terminating the physical connections and for processing the specific Layer 2 and higher protocols, including ATM, MPLS, PoS, Frame Relay, and IP. Inter-working among protocols is achieved by routing traffic to other protocol-specific line cards as needed, thereby allowing the architecture to be multi-service at the system level. Other items included on a typical line card include LIU/Framers to transmit and receive data, host processor, and a backplane or switch fabric interface logic/chip.

Some architectures may also use TDM and packet/cell switch fabric line cards. Fabric solutions usually include one or more fabric chips that reside on one or more central switch fabric cards. Additional fabric interface chips generally reside on the line cards, bridging traffic from an ASIC or ASSPs to the fabric itself. Ranges of speed for switch fabrics vary from 20 Gbps to Terabits per second. Another approach to switch fabrics is a mesh backplane. A mesh is an open architecture, distributed fabric where each node has both a 1 by N switch to transmit traffic to other nodes and N-1 point-to-point connections to every other node for receiving traffic. For switches not requiring massive backplane speeds, mesh fabrics provide a very cost-effective solution.

Figure 1: Traditional, Single-Protocol Multiservice Switch Line Card — Functional Blocks



Traditional multiservice platforms typically use line cards based on in-house ASIC development or application-specific silicon. These line cards are usually dedicated to a single service (such as ATM or Frame Relay) and have a set number of interfaces that they can support. Space and cost become an issue when service providers are faced with adding another chassis or platform to accommodate expansion.

To maximize ROI for network equipment manufacturers and service providers, consolidation of multiservice switch technologies is becoming key. Merging interfaces and protocols and adding greater density per line card — all while reducing board components, power consumption, and costs — is a tough challenge with traditional ASIC-based or ASSP designs. In addition, new and evolving services must be provided to keep pace with end-user demands. One of the greatest challenges is to be able to scale the platform to adapt to changing requirements and standards over time without major disruption to the service provider network.

Increasing interface density and bandwidth has been an ongoing challenge for network equipment manufacturers. It is not uncommon today to see systems providing up to 32 ports of T1/E1, where two years ago the standard was four or eight ports per line card. Likewise, bandwidth capacity of these systems has seen a steady increase. Two years ago, the most common range of speed interfaces was from T1/E1 to OC-3 (maximum). Today, these systems must support speeds from channelized DS0 to OC-48c — and even OC-192 in some cases (although numbers of shipments are low for this speed). The Dell'Oro Group calculated that DS3 and OC-12, particularly the channelized versions, will be the primary bandwidths for connecting enterprises to the service provider networks, while OC-48 and above will be limited to 3% of total ports shipped in 2006 (Dell'Oro Group 01/28/02 Switches & Routers Report). Bottom line: the challenge is to provide scalable line cards that offer a range of speeds and provide the necessary interface density to address the multiservice switch market space.

The traditional design of a single protocol line card is also being challenged in today's environment. Again, more and more vendors are delivering multi-protocol capabilities on a single line card. Popular examples include ATM/IP and IP/PoS on a single line card. In addition, adaptability is key in keeping up with evolving standards and market requirements. Examples of evolving protocols and standards include RFC 2684 (describing AAL-5 encapsulation methods) replacing RFC 1483, and the migration from IPv4 to IPv6. Furthermore, once the design is released to market, the limited flexibility of hardware-based product designs severely restricts the ability to adjust or add product functionality.

Designers also need to continue to be sensitive to power and cost budgets for line cards. Additional components often needed to implement additional interfaces and functionality — such as MACs/Framers, ASSPs, ASICs, coprocessors, and memories — lead to higher power requirements along with added costs. The challenge is to provide more functionality with less components to meet power budget and reduce overall system costs.

As networks evolve, there is an ever-increasing requirement for complex multi-protocol processing and intelligence at the access and edge of the networks. Scalability, adaptability and flexibility are required in order to address these requirements. The challenge for network equipment manufacturers is to facilitate these requirements in a dynamic environment while ultimately providing improved ROI and cost efficiency.

DESIGNING IN FLEXIBLE INTERFACES AND PROTOCOLS

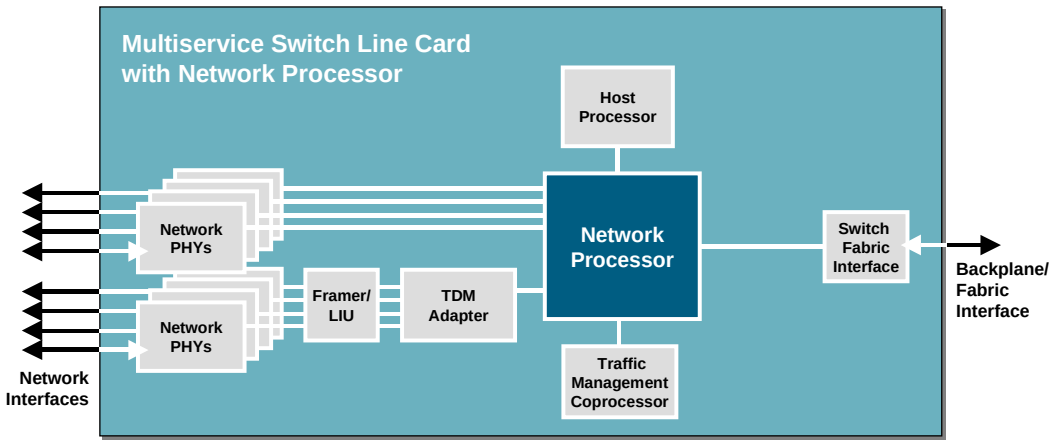
To meet the challenges of multiservice switch design, while leveraging the investment in existing multiservice switch architectures, network equipment manufacturers can benefit by integrating network processor (NPU) technology into their platforms. NPUs provide the flexibility and performance to enable network equipment manufacturers to consolidate multiple protocols on a single line card and even increase port density on that line card. NPUs are fully programmable devices optimized for fast path processing of packet and/or cell streams. Consequently, instead of investing in costly, long ASIC development cycles, vendors using NPUs can invest in less costly and shorter software development cycles — and be able to reprogram systems in the field as required. In addition, many NPUs typically require less supporting silicon on a board because of the high-level of functional integration on chip.

One line card using an NPU can displace previous solutions consisting of two or more cards — at a lower cost then the previous line cards. Multiple protocols can be combined on a single line card along with increased port density if needed. With an NPU implementation, you are able to eliminate extra logic (such

as ASICs, ASSPs, SARs, Framers, and FPGAs) resulting in significant savings per line card. Note that the level of integrated functions on the NPUs reduces part count, which in turn means less power, space and bus interconnects. For example, Motorola's NPUs have built-in Ethernet MACs, SONET Framers, SARing capabilities, classification, buffer management, fabric control, and host control.

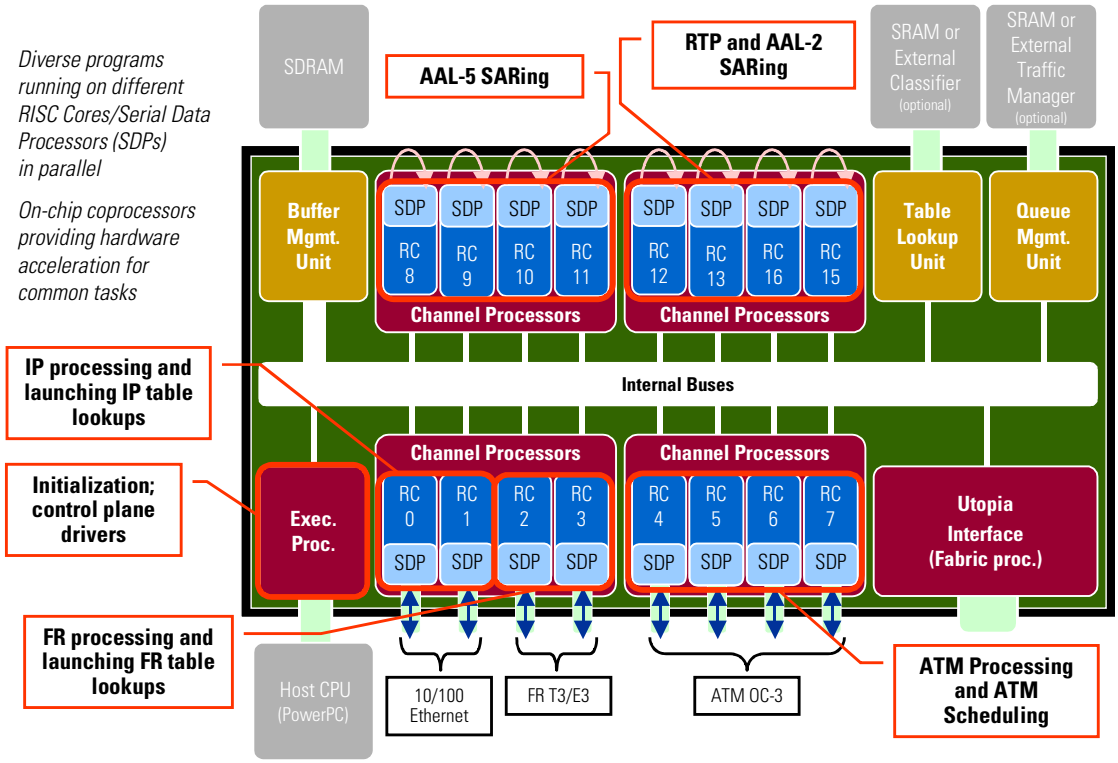
Not only do NPUs enhance a multiservice switch line card design by their high-level of functional integration, but they also provide greater bandwidths, higher densities, and more flexibility than traditional solutions, enabling greater system scalability. For example, with Motorola's C-5e NPU, 16 interfaces can be programmed on a single piece of logic, with each port capable of handling up to an OC-3c's worth of bandwidth (therefore a maximum of 16 ports of OC-3c per NPU). These interfaces can be programmed to support a mixture of protocols. For example, you could have OC-3/ATM running on one interface and another interface running Ethernet/IP. Increasing granularity can easily be accomplished with the addition of framers. The C-5e NPU can support up to 64 ports on T1/E1 with quad framers fronting the 16 external ports. By adding Motorola's TDM channel adapters to a design, a single C-5e NP can support even higher densities up to hundreds of T1/E1s. Motorola also offers an OC-12 class of NPU with eight external interfaces called the C-3e NPU, which has the same interface extension capabilities.

Figure 1: High-Density Multiservice Switch Line Card — Network Processor Design



Because the NPU is a programmable device optimized for fast path processing of packet and cell streams, it is possible to implement complex interworking applications in a fairly streamlined manner. The following diagram shows how an NPU might be programmed to handle protocol interworking within a single chip. The Motorola C-3e NPU is used in this example. In this application two T3/E3 interfaces are programmed for Frame Relay, two ports for Ethernet (10/100 Mbps), and four ports for ATM OC-3c with SARing (Segmentation and Reassembly) implemented on separate internal processing clusters. Layer 3 IP packets, traversing from Ethernet or Frame Relay, are AAL-5 encapsulated in the SAR cluster. Similarly, cells traversing from ATM to Ethernet or Frame Relay are reassembled into packets. If the data is traversing from one ATM interface to another ATM interface, the incoming cells are reassembled in the SAR cluster; the encapsulated IP packet is examined and again the packet is chopped into cells. These cells are then sent to the outgoing ATM interface. This application alone can replace up to three line cards (one each for Frame Relay, Ethernet, and ATM) in traditional multiservice switch designs.

Figure 3: Multi-Protocol Multiservice Switch Application on One Network Processor — Motorola C-3e NPU



Another advantage of NPUs is that they can aid in developer productivity through the development tools and reference applications provided. For example, the SwitchRouter application, provided with Motorola's C-Ware Software Toolset (CST), provides interworking of three applications: Frame Relay, Ethernet, and ATM, including AAL-5 SARing. This enables developers to get a jump start on their application with similar features.

DESIGNING IN VALUE-ADDED SERVICES

NPUs offer a high degree of flexibility in adding services to multiservice switch line cards. Inherent in most NPUs are functions such as classification, SARing, and traffic management. However, NPUs may differ architecturally in how they handle these functions. One model is the processor+coprocessor model wherein processors handle much of the services processing, but hardware acceleration is provided for computationally intensive functions through integrated coprocessors. Other models offer micro-engine farms that may be programmed for all functions or in some cases require the use of external coprocessors.

Motorola's NPUs are an example of the processor+coprocessor model in that they provide C-programmable RISC Cores to handle functions such as SARing, but for functions such as classification and traffic management, they have integrated coprocessing elements that off load processing from the RISC Cores. One such hardware accelerator in the C-5e NPU is the TLU (Table Lookup Unit). The TLU enables a wide range of traffic classification functions and support for a variety of exact match and longer prefix match algorithms, eliminating the requirement for an external classification engine.

QoS is a key mechanism in multiservice applications where the convergence of services requires appropriate levels of transmission quality for various types of applications such as VoIP, streaming video, Web casting, or data transfer. Technologies such as ATM, IP DiffServ (Differentiated Services), and MPLS have been developed in order to facilitate the deployment of QoS across networks by providing sufficient QoS differentiation and ease of management and provisioning while maximizing overall network utilization. These QoS technologies may be supported to some degree on the NPU (called soft queuing) or they may require an external traffic management coprocessor (TMC) to off load the complex algorithms and buffering mechanisms involved in fine-grained QoS.

Key requirements of TMCs in supporting multiservice applications include multi-protocol support (standard and non-standard), micro-level QoS controls, flexible scheduling hierarchy, buffer management, fully configurable service level agreements (SLAs), and high-level APIs for ease of programming and investment protection. These requirements can be addressed in a product such as Motorola's Q-5 TMC, designed as look-aside traffic manager to the Motorola NPUs. The Q-5 TMC offers 5 Gbps of multi-protocol support for virtually any protocol, including ATM TM 4.x, IP DiffServ, IntServ, MPLS, Ethernet, PoS, and Frame Relay.

The benefits of using NPUs (and when necessary their supporting coprocessors) for implementing QoS is that it is possible to dynamically adjust QoS configurations to meet the growing and changing needs of the multiservice network.

SUMMARY

Service providers are challenged more than ever to provide improved financial returns. They want to leverage their network build-outs of the past several years through increasing the density and protocol capabilities of line cards in existing platforms — and at the same time provide new revenue-generating services to their customers. An NPU-based solution can deliver a new generation of high-performance, cost-efficient, hybrid multiservice switch line cards that incorporate multi-protocol capabilities, evolving standards, and higher densities — and can be easily integrated into existing and new multiservice switches.

In cases in which additional logic is required (such as intensive classification applications or VPN/IPSec applications running at multiple gigabits per second), adherence to industry specifications, such as Network Processing Forum (NPF), can ensure interoperability with 3rd party equipment. This applies not only to hardware elements, but also to software applications and protocols. The NPF encourages the growth and effective use of network processing technologies through specifications, benchmarks, interoperability, and education initiatives.

By adding network processors to multiservice switch designs, you get the flexibility and adaptability to add new services to meet market requirements for today and the future.

REFERENCES

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