The Development of Component-level Thermal Compact Models of a C4/CBGA Interconnect Technology: The Motorola PowerPC 603™ and PowerPC 604™ RISC Microprocessors

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ABSTRACT

Thermal resistance networks or "compact" models of the PowerPC 603 and PowerPC 604 microprocessors in controlled-collapsed-chip-connection / ceramic-ball-grid-array (C4/CBGA) single-chip package are derived from "detailed" three-dimensional conduction models of the parts by both analytical and data fitting techniques.

The behavioral correctness of these models is assessed by comparing the die-junction temperatures predicted for the compact model with the detailed model results for a range of boundary conditions applied at the surfaces of the package. The performance of these models is then verified by comparing the detailed and compact models in an application-specific environment (a wind tunnel) using a computational-fluid dynamics program. The interaction between the package and its environment is also discussed.

The work reported here forms part of a long term European research program to create and validate generic thermal models of a range of electronic parts.

NOMENCLATURE

Qj   =   die power, W
QiC   =   heat flux through node "i" in the compact model
QiD   =   heat flux through surface in detailed model corresponding to node "i" in the compact model
Rjc   =   die-junction-to-case resistance, °C/W
Rjl   =   die-junction-to-lead (i.e.,ball) resistance, °C/W
Rja   =   die-junction-to-ambient resistance, °C/W
Tj   =   die-junction temperature, °C
TjC   =   die-junction temperature in compact model, °C
TjD   =   die-junction temperature in detailed model, °C
Ta   =   ambient (inlet) temperature of cooling fluid, °C
Tc   =   package case temperature, °C
Tl   =   package lead temperature, °C
CostQ =   measure of error in surface heat flux prediction
CostT =   measure of error in die-junction temperature prediction

INTRODUCTION

PowerPC 603 and PowerPC 604 RISC Microprocessors

The scaleable PowerPC™ microprocessor family (Figure 1), jointly developed by Apple, IBM, and Motorola, is being designed into high-performance cost-effective computers (including notebooks, desktops, workstations, and servers). The PowerPC microprocessor family ranges from the PowerPC 601™ to the PowerPC 620™. The PowerPC 603 microprocessor is a low-power implementation of the PowerPC Reduced-Instruction-Set-Computer (RISC) architecture. The PowerPC 604 microprocessor is a 32-bit implementation of the PowerPC architecture, and is software and bus compatible with the PowerPC 601 and PowerPC 603 microprocessors. Both the Motorola PowerPC 603 and PowerPC 604 microprocessors are available in a 21mm controlled-collapsed-chip-connection / ceramic-ball-grid-array single-chip package (C4/CBGA) (Figures 2, 3; Table 7) [1-5].
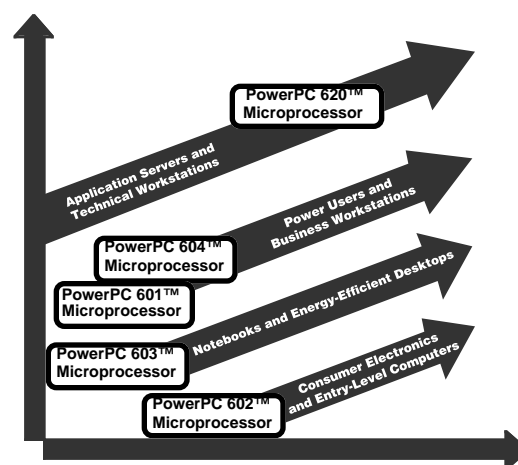

Figure 1. The PowerPC Microprocessor Family.

Thermal control of these microelectronic devices is required for proper operation and acceptable reliability. Thermal control is becoming an increasingly critical part of the design of microelectronic systems. Increases in the number of transistors per chip, chip area, and device clock frequency have resulted in increased heat production at the package
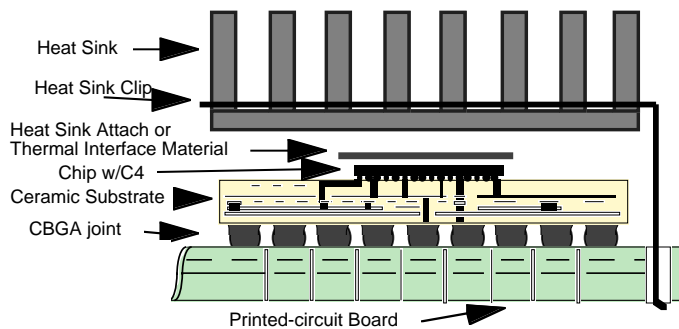
Figure 2. C4-Ceramic-Ball-Grid Array: Exploded Cross-sectional View with Optional Heat Sink (not to scale).

level. Together with the increasing use of surface mount technology these trends have resulted in higher power dissipations at the board and cabinet level. Reliable thermal models of components are now required to reduce prototyping, as companies strive to reduce design-cycle time and to design their products "right the first time".

C4-Ceramic-Ball-Grid Array Package
The use of C4 die on a CBGA interconnect technology offers significant reduction in both the signal delay and the microelectronic packaging volume [14-19]. Figure 2 shows the salient features of the C4/CBGA interconnect technology, with an optional heat sink; while, Figure 3 is a photo of the PowerPC 604 microprocessor showing the exposed die on the left and the ball array on the right. The C4 interconnection provides both the electrical and the mechanical connections for the die to the ceramic substrate. After the C4 solder bump is reflowed, epoxy (encapsulant) is under-filled between the die and the substrate. Under-fill material is commonly used on large high-power die; however, this is not a requirement of the C4 technology. The package substrate is a 21mm multi-layer co-fired ceramic. The package-to-board interconnection is by an array of orthogonal 90/10 (lead/tin) solder balls on a 1.27 mm pitch. During assembly of the C4/CBGA package to the board, the high-melt balls do not collapse [3].

C4/CBGA requires less board routing space than a wire-bond ceramic-quad-flat-pack (WB/CQFP). Therefore, the C4/CBGA offers the same connections in a significantly smaller board area than a comparable WB/CQFP (Figure 4). This area reduction results in an approximate four-fold increase in package-level thermal flux density.

For most single-chip packaging technologies the method of connection for the power, ground, and signals to the next-level interconnect (e.g., printed-circuit board, PCB) often presents another challenge for adequate heat removal. That is, a conflict often exists between needs for electrical interconnect and the needs to design an adequate heat conduction path to minimize the package thermal resistance. However, the C4/CBGA technology is unique in that it allows electrical interconnect on the ball-array side, while the back of the die is exposed for thermal management.
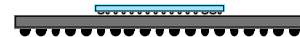

Figure 3. Photo of the PowerPC 604 Microprocessor in the C4/CBGA Package (die side on left, ball array on right).
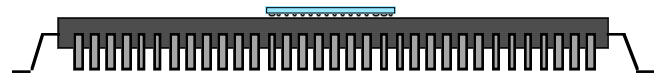

Figure 4. Size Comparison: 21 mm C4-Ceramic-ball-grid array versus a 40 mm Ceramic-quad-flat package (relative scale).

OBJECTIVE

The motivation behind the current work is to examine the behavior of compact models generated by different methods, for two packages of the same generic design, and then compare the performance of these models in a test application using a system-level thermal design tool.

This paper presents the development of three-dimensional computational-fluid dynamics (CFD) models for the first two C4/CBGA PowerPC RISC microprocessors that have been introduced by Motorola: that is, the PowerPC 603 and PowerPC 604 microprocessor in a 21mm C4/CBGA package. To improve computational efficiency for board- and system-level analysis, it is desirable to reduce the detailed model into an equivalent model. This equivalent compact or "behavioral" model could then be used in the design of electronic systems, where the boundary conditions experienced by the part will depend on the cooling strategy employed.

The objective of this paper is to describe the development of compact thermal models from a detailed model, to include a description of:

- the detailed three-dimensional CFD models
- the methods used to generate the compact models

• the representation of the n-resistor compact models within the system-level thermal design tool, and
• the wind tunnel simulations used to test the steady-state compact model behavior vs. that of the detailed model

BACKGROUND

The work forms a part of a three-year European Union funded ESPRIT project named DELPHI which seeks to address the fact that the accurate prediction of die-junction temperatures at the component-, board- and system-level is seriously hampered by the lack of reliable standardized input data. The electronic parts studied include a variety of chip packaging styles, heat sinks, fans, baffles and interfacing materials. A comprehensive account of this project is given by Rosten [6].

The overall aim of DELPHI is to show that accurate predictions can be made using compact models and to encourage package vendors to provide such models of their packages. The inspiration for this approach was drawn from the following quote from Bar-Cohen, Elperin and Eliasi [7]:

"The thermal precision required in the development of a competitive packaging design could best be served by vendor delivery of a validated numerical model ... for each chip package in its inventory"

This approach has been demonstrated by Rosten and Viswanath [8] for a Ceramic Pin Grid Array (CPGA) and Rosten et. al. for a Plastic Quad Flat Pack (PQFP) [9].

Computer system performance has dramatically improved over the past three decades. Much of this improvement is a result of increased integration of components at the semiconductor level, made possible by reduced feature sizes. These reduced feature sizes have resulted in several semiconductor integrated-circuit (IC) trends, all of which are increasing: gate count, chip inputs/outputs, chip size, operating frequency, and power consumption. These trends have placed an increased emphasis on microelectronics packaging design.

Use and Limitations of Traditional Thermal Package Metrics

Common figures-of-merit used for comparing designs of microelectronic packaging are the die junction-to-ambient, die junction-to-case, and die junction-to-lead thermal resistances:

$$Rja = (Tj - Ta)/Qj \qquad (1)$$
$$Rjc = (Tj - Tc)/Qj \qquad (2)$$
$$Rjl = (Tj - Tl)/Qj \qquad (3)$$

These metrics are determined under idealized conditions, that is, a single component is empirically characterized on a low conductivity printed-circuit board, according to international standards. Kromann [4] showed the effect of board-level thermal flux for the PowerPC 603 microprocessor when powered at 3 watts with no heat sink. When only a single component was powered (similar to these standards) the temperature rise was 50°C; however, when 9 components were powered the temperature rise increased to 140 °C. Thus, if one used the traditional Rja metrics to predict the die-

junction operating temperatures for the populated-board case, the error would be approximately 300%. The suitability of these traditional thermal metrics (eqn. 1, 2, 3) for design calculations is described in the following quote:

"The intent of Rja measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment" [10]

No single parameter can adequately describe three-dimensional heat flow, which is a function of many parameters, such as: geometry, heat source and placement, package orientation, next-level package attachment, heat sink efficiency, and method of chip connection. Many references in the literature discuss both the use and the limitations of these metrics [7,11,12,13].

C4-Ceramic-Ball-Grid Array Package: Heat Transfer Paths

To increase the thermal dissipation capability of this technology, a heat sink may be mated to the silicon die (i.e., as this technology is exposed die, the package case is the top of the die). Several commercially-available active and passive heat sink products are available: 1) several pin-fins; 2) bi-directional; 3) stamped; and 4) a pin-fin heat sink with an attached cooling fan. The integral fan heat sink promotes local convection cooling, at an approximate 1 watt power draw.

Due to the fragility of the silicon die, any heat sink attach material must be structurally compliant. Two heat sink attach options exist: 1) thermal pastes with a mechanical attach to the board, or 2) compliant adhesives (e.g., low shear stress epoxy, or silicone). An alternate implementation of the C4/CBGA incorporates an aluminum cap with thermal paste internally sealed [14].

For cases with an attached heat sink, the primary heat transfer path is as follows. Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material and finally to the heat sink where it is removed by natural or forced-air convection.

As the PowerPC 603 microprocessor is a low-power implementation of the RISC architecture, the use of a heat sink may not be necessary. Heat conducted through the silicon may be convectively removed to the ambient air. In addition, a second parallel heat flow path exists by conduction, through the C4 bumps and the epoxy under-fill, to the ceramic substrate for further convection cooling off the edges. From the ceramic substrate heat is also conducted via the leads/balls to the next-level interconnect; whereupon the primary mode of heat transfer is by convection and/or radiation. This path alone may be adequate for low-power chips; however, it is a function of the board population and the system-level conditions.

PACKAGE MODEL DEVELOPMENT: DETAILED MODEL

The detailed model of the package was constructed in a commercial finite-volume based computational-fluid

dynamics (CFD) tool, FLOTHERM® [20]. The same tool was used to solve the steady-state conjugate heat transfer present in the wind tunnel calculations used to analyze the performance of the models.

The detailed package models were constructed from conducting cuboid blocks representing the die, C4/underfill, co-fired ceramic substrate, and the ball array. The dimensions and thermal conductivities of these blocks are given in Table 1.

The effective thermal conductivity for heat flow through the block representing the C4/underfill was calculated from data on the size and number of the C4 solder bumps, and the thermal conductivities of the solder and the underfill epoxy. Similarly, the conductivity for heat flow through the package solder balls was calculated from the solder ball geometry and the conductivities of the solder and the surrounding air.

PACKAGE MODEL DEVELOPMENT: COMPACT MODELS

The detailed models were used to generate a number of thermally-equivalent compact thermal resistance network models. In previous studies, considerable effort has been spent validating the detailed modeling methodology and verifying the correctness of the data used [8,9]. Validation of the detailed models in the present study is not an issue. This work is only concerned with a performance comparison between the detailed and compact models.

Three methods of generating compact models are investigated in this study. Methods I and II generate star-shaped networks, in which the thermal resistors provide connections between the die junction and the surfaces of the package. Method III extends the technique used in Method II to models that include "shunt" resistances connecting the surface nodes to each other.

Each of the three methods involve running the detailed model for a set of boundary conditions imposed at the surfaces of the package that correspond to surface nodes in the chosen resistance network. All other surfaces are treated as adiabatic. Grid independence of the die-junction temperatures predicted for the detailed model was achieved for the set of boundary conditions imposed.

Method I: Surface Temperature Perturbation Method
This method has been described by Rosten [6]. The technique applies to star-shaped networks, where surface nodes connect to the die junction, but not to each other. The limitations of this type of network when highly non-uniform boundary conditions are imposed has already been discussed by Lasance et. al. [21].

Methods II & III: Linear Least Squares Data Fitting Method
This technique involves solving the detailed model with all surfaces representing nodes in the compact model connected to the ambient temperature, Ta. The connection is made by setting a heat transfer coefficient at each surface. In this

study, the set of 38 boundary conditions suggested by Lasance et. al. [21] were used, the purpose of which is to represent the full range of boundary condition combinations the part might experience in practice. The data fitting technique used to determine the values of the selected set of resistances minimizes the cost function:

$$CostQ = \sum_{1}^{38} \sum_{i=1}^{i=N} \left[\frac{QiC - QiD}{QiD} \right]^2$$

where i represents one of the N surface nodes in the network.

Table 1. Dimensions and Thermal Conductivities Used in Detailed Models.

Block in Model	Conduct-ivity (W/mK)	PowerPC603 Microprocessor: Model Dimensions (mm)	PowerPC604 Microprocessor: Model Dimensions (mm)
Die	108	7.5 x 11.5 x 0.61	12.4 x 15.8 x 0.61
C4/under-fill	0.8	7.5 x 11.5 x 0.102	12.4 x 15.8 x 0.102
Ceramic substrate	16.5	21 x 21 x 1.02	21 x 21 x 1.02
BGA array	17.6	21 x 21 x 0.94	21 x 21 x 0.94

Network Quality
The quality of the models generated by all the above methods are assessed by comparing the die-junction temperatures they produce for the 38 boundary conditions with the die-junction temperatures originally obtained for the detailed model, expressed as an average temperature over the die junction surface.

Measures of the quality of the resulting network presented here are the value of the cost function:

$$CostT = \sum_{1}^{38} \left[\frac{(TjC - TjD)}{(TjD - Ta)} \right]^2$$

and the minimum and maximum values of the percentage relative error in die-junction temperature, defined as:

$$\%Tj\_error = 100 \times \frac{(TjC - TjD)}{(TjD - Ta)}$$

These measures of quality for the PowerPC 603 and PowerPC 604 microprocessor are respectively shown in Tables 3 and 4.

Package Interconnection
In the present study, the package interconnection ball array was included in the compact model for simplicity. The ball array represents a uniform resistance over the bottom of the package as the array is fully populated, except for one ball in

Table 2. Resistance Network Maps for Fully Connected 4 and 5 Node Models

Topology:	Node:	Die-junction	top inner	top outer
4 Node Network	top inner	R12	-	-
	top outer	R13	R23	-
	BGA	R14	R24	R34

Topology:	Node:	Die-junction	top inner	top outer	BGA inner
5 Node Network	top inner	R12	-	-	-
	top outer	R13	R23	-	-
	BGA inner	R14	R24	R34	-
	BGA outer	R15	R25	R35	R45

Table 3. Resistance Values for the PowerPC 603 Microprocessor Compact Models

Method:	Method I		Method II		Method III	
Model:	C1	C2	C3	C4	C5	C6
Resistance	4 node	5 node	4 node	5 node	4 node	5 node
R12	5.8E-2	5.8E-2	5.8E-2	5.8E-2	5.8E-2	5.8E-2
R13	8.1	8.1	22.3	22.3	∞	12.5
R14	3.5	4.1	4.3	7.9	3.3	3.8
R15	-	23.4	-	6.9	-	37.1
R23	-	-	-	-	∞	∞
R24	-	-	-	-	4.3E+3	∞
R25	-	-	-	-	-	8.4E+3
R34	-	-	-	-	9.5E-1	13.7
R35	-	-	-	-	-	3.2E-1
R45	-	-	-	-	-	8.2
CostT	3.7E-1	4.1	1.2	7.1E-1	1.4E-1	1.6E-2
Max % Tj error	19.1	63.7	45.9	43.5	14.3	5.1
Min % Tj error	-19.1	-1.1	-1.5	-0.5	-5.2	-0.5

the corner of the package. As such, the resistance this represents adds to the values of the die-junction-to-BGA resistances.

COMPACT MODEL REPRESENTATION

FLOTHERM® Version 1.4 supports star-shaped network models via thermal resistances applied to the surface of cuboid blocks, to give a mathematically equivalent representation of the resistance network.

Details Of Compact Models Generated

Schematic diagrams of the resistances present in each of the models created in this study are shown in Figure 5. Resistance network maps showing the resistances present in fully connected 4 and 5 node compact models are given in Table 2. Tables 3 and 4 give the resistance values for the PowerPC 603 and PowerPC 604 microprocessor compact models.

DISCUSSION OF MODELS

The detailed models represent thermal test parts in which the thermal test die provides a uniform heat source over almost all of the active side of the die, so that the die junction is isothermal. If all the package surfaces are held isothermal the

resulting Rjc value is determined under conditions where the analogy between thermal resistance and electrical resistance holds true. Heat leaves one isothermal surface to arrive at the other, with no losses.

Heat loss from the sides of the die are ignored in the compact models, causing one-dimensional heat flow through the die, so the die-junction-to-top inner resistance, R12 is also obtained under conditions where the analogy holds true. In the present study, the term "thermal resistance" is also used when the package surface is not isothermal. As such the resistances presented here can include a contribution due to heat spreading within the package.

The parallel resistance sum of the R14 and R15 resistances in the C2 model is 3.5°C/W. This is the same as the R14 value in the C1 model. Note that Method I requires that the isothermal case Rjc described above is the parallel resistance sum of the die-junction-to-surface resistances. For the C1 model this gives:

$$1/Rjc = 1/R12 + 1/R13 + 1/R14$$

This is not the case for the C3 and C4 models generated by Method II. Rjc values of 0.057°C/W and 0.025°C/W respectively are obtained for the PowerPC 603 and PowerPC 604 microprocessor, by solution of the detailed model with all package surfaces held isothermal. Interestingly, the 5

Table 4.   Resistance Values for the PowerPC 604 Microprocessor Compact models

Method:	Method I		Method II		Method III	
Model:	C7	C8	C9	C10	C11	C12
Resistance	4 node	5 node	4 node	5 node	4 node	5 node
R12	2.5E-2	2.5E-2	2.5E-2	2.5E-2	2.5E-2	2.5E-2
R13	5.2	5.2	14.4	14.4	∞	8.3
R14	1.4	1.6	1.6	2.2	1.4	1.5
R15	-	15.1	-	4.3	-	22.2
R23	-	-	-	-	∞	∞
R24	-	-	-	-	2.3E+3	4.4E+3
R25	-	-	-	-	-	∞
R34	-			-	1.3	6.8
R35	-	-	-	-	-	4.8E-1
R45	-	-	-	-	-	5.1
CostT	1.0E-1	1.2	4.4E-1	2.4E-1	4.1E-2	4.2E-3
Max % Tj error	10.8	32.9	26.9	27.0	7.7	2.6
Min % Tj error	-9.9	-0.6	-0.9	-0.4	-2.7	-0.2

node C2 model is generally inferior to 4 node C1 as seen from the higher CostT and high maximum percentage Tj error in Table 3. This is counter-intuitive, as one would naturally expect the more intricate representation would give the best results.

For the C2 model the R15 resistance (23.4°C/W) is quite large compared with R14 (4.1°C/W), forcing the heat to enter the PCB under the center of the package. This is what would happen if the board were isothermal. If all surfaces were isothermal the C2 model would exactly predict the detailed model die-junction temperature, as this is the condition under which the detailed model was used to determine the compact model resistances.

In practice, the board is hottest under the center of the package. This non-uniform boundary condition causes greater heat spreading within the package, so less heat enters the board under the center of the package. If the R14 and R15 resistors in the compact model are determined by a fit to a range of boundary conditions, as they are in the C4 model, a higher R14 resistance, and a lower R15 resistance should therefore result. Also, as more heat spreading occurs within the package, the parallel resistance sum of the R14 and R15 values should be higher. The values in Table 3 support this. The R14 value in the C3 model (4.3°C/W) is higher than the value in the C1 model (3.5°C/W). For the C4 model the parallel sum of R14 and R15 (3.7°C/W) is higher than that of the C2 model (3.5°C/W).

In the C3 and C4 models where the resistances are determined by a fit of the data, the additional node produces a more reliable model over the 38 boundary conditions [21], as shown by the slightly lower cost in Table 3. However, adding more resistances between the die-junction and points on the package surface has limited benefit when the heat flux lines within the package are strongly curved, for example when the external thermal resistance at one of the package surfaces is high, forcing heat to leave through the other surfaces. For the model to accommodate such circumstances heat flow paths between the nodes are required.
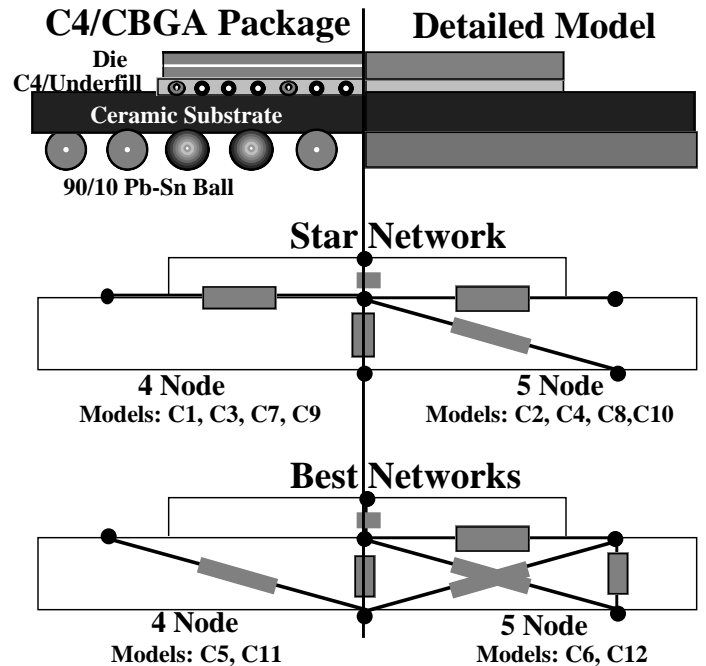

Figure 5.   Resistance Network Diagrams of the C4/CBGA Package.

The C5 and C6 models respectively have the same surface nodes as the C3 and C4 models, and are determined by fitting to the same detailed model data using the same technique. Additional connectivity between the nodes is considered in these models, and the method is used to determine the network which gives the lowest CostT for the set of 38 boundary conditions.

There should be no direct connection between the top inner node and any of the other surface nodes as the heat which passes through the top inner node must also go through the die junction in this package design. Observe that when these resistances (i.e., R23, R24 and R25) are included in the
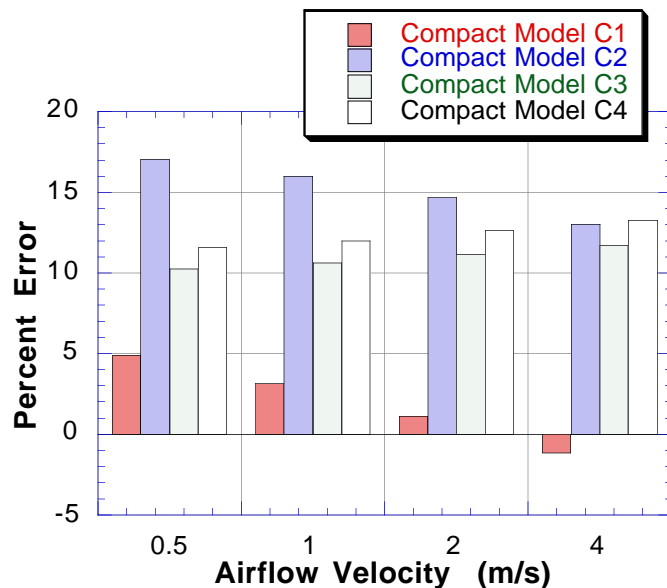
Figure 6. PowerPC 603 Microprocessor with a Printed-Circuit Board Conductivity of 0.4 W/mK: Compact Model Die-junction Temperature Error vs. Flowrate.

model, they are predicted as either infinite or effectively infinite (>2,000 °C/W).

The C7 to C12 models of the PowerPC 604 microprocessor are all equivalent to their PowerPC 603 microprocessor counterparts. The lower CostT values in Table 4 show that in all cases the fit over the 38 boundary conditions is better than that of the corresponding PowerPC 603 microprocessor model. This is presumably due to the larger die in the same size package resulting in heat flows that are less three-dimensional in the PowerPC 604 microprocessor, which also produces smaller die-junction-to-surface resistances.

DESCRIPTION OF WIND TUNNEL CALCULATIONS

To examine the suitability of the compact models for design purposes, their behavior was compared with the detailed model in a wind tunnel environment. It should be stressed here that the details of the wind tunnel calculations are unimportant to the results and conclusions of this study. The intent is to provide a thermal environment that is the same for both the detailed and compact models. The flow conditions remain constant, so that the differences observed are due to differences in the models and the effect the models have on their own environment.

The environment considered is a wind tunnel of 30.5 cm square test section in which the parts are centrally placed. The parts are assembled onto 7.62 cm square test boards. Two board conductivities are considered, 0.4 W/mK and 20.0 W/mK. The air flow was turbulent in all cases and an algebraic turbulence model was used. An ambient temperature of 25°C was assumed.
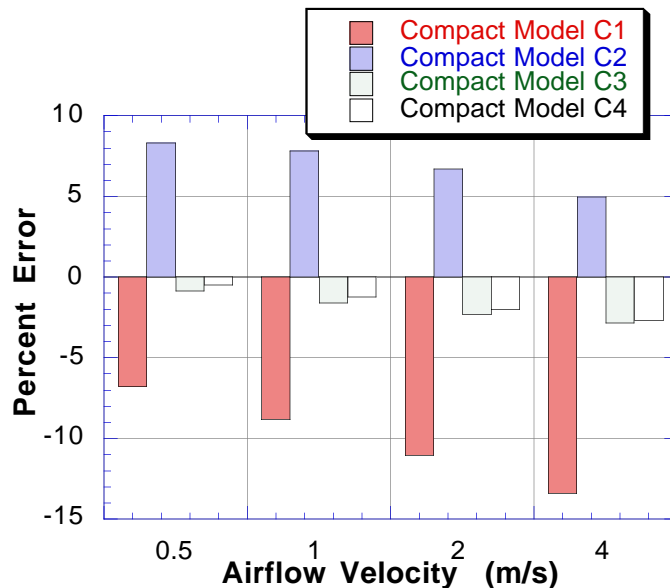

Figure 7. PowerPC 603 Microprocessor with a Printed-Circuit Board Conductivity of 20 W/mK: Compact Model Die-junction Temperature Error vs. Flowrate.

Table 5. PowerPC 603 Microprocessor Detailed Model Die-junction Temperature Rise Above Ambient vs. Flowrate (Tj-Ta vs. flowrate).

PCB Conductivity (W/mK)	Temperature Rise (Tj-Ta,°C) at Flowrate (m/s)			
	0.5	1.0	2.0	4.0
0.4	123.8	94.2	71.1	54.3
20.0	41.09	34.4	29.3	25.2

Table 6. PowerPC 604 Microprocessor Detailed Model Die-junction Temperature Rise Above Ambient vs. Flowrate (Tj-Ta vs. flowrate)

PCB Conductivity (W/mK)	Temperature Rise (Tj-Ta,°C) at Flowrate (m/s)			
	0.5	1.0	2.0	4.0
0.4	53.1	39.2	31.8	27.5
20.0	46.1	34.3	28.0	24.2

Again, to ensure that the differences observed in the study are due to differences in the models and their interaction with the environment, identical grids were used for all calculations. For the calculations performed on the PowerPC 603 microprocessor a total mesh density of 51,000 nodes was used. For the PowerPC 604 microprocessor 181,000 cells were used. The grid distributions were chosen to resolve the boundary layers adjacent to the exposed surfaces and the temperature distribution within the assemblies.

In the calculations performed, the PowerPC 603 microprocessor was powered to 3W, with the top of the
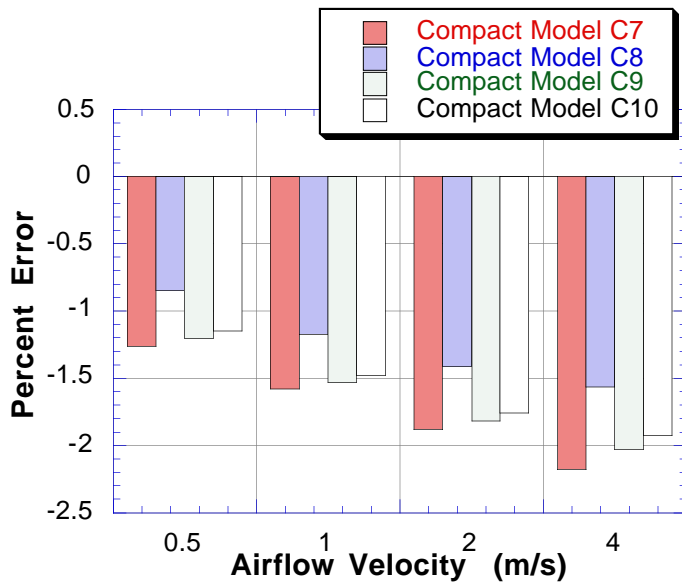
Figure 8. PowerPC 604 Microprocessor with a Printed-Circuit Board Conductivity of 0.4 W/mK: Compact Model Die-junction Temperature Error vs. Flowrate.
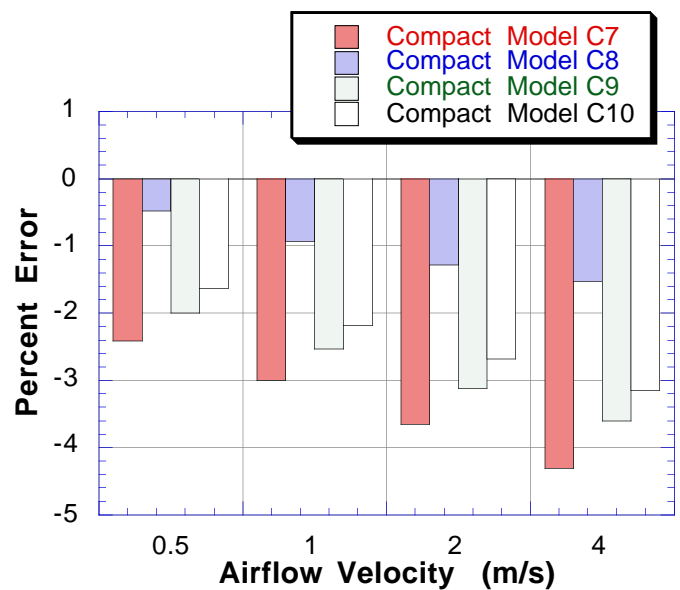

Figure 9. PowerPC 604 Microprocessor with a Printed-Circuit Board Conductivity of 20 W/mK: Compact Model Die-junction Temperature Error vs. Flowrate.

package exposed to the passing air flow. Radiative heat transfer from the package was omitted from the calculations as this would mask differences between the models. The PowerPC 604 microprocessor was powered to 18W and had a clip-mounted commercially-available heat sink. To reduce the thermal contact resistance between the die and the heat sink, this heat sink incorporates a pre-applied thermal interface material to the exposed die surface [22].

RESULTS

The detailed model die-junction temperatures for the wind tunnel predictions for the PowerPC 603 and PowerPC 604 microprocessors are given in Tables 5 and 6; respectively. The corresponding errors in the die-junction temperature obtained with the compact models are given in Figures 6, 7, 8 and 9.

Discussion Of Results

The wind tunnel calculations for the PowerPC 603 microprocessor reported in Table 5 also showed that between 41% and 89% of the die power leaves the package via the board, with the higher figure found for the package mounted on the high conductivity board at 0.5m/s. This makes the interaction between the package and the board an important factor in the prediction of the die-junction temperature. Figure 5 shows the relative errors in die-junction temperature for the PowerPC 603 microprocessor compact models C1 to C4. For the low conductivity board a general over-prediction is seen with the over-prediction for the 5 node models being slightly greater than the corresponding 4 node models. This is consistent with the earlier comments regarding the heat flux distribution into the board.

The largest under-prediction was found for the C1 model on a high conductivity board, with the C2 model on the low

conductivity board giving the largest over-prediction. These results, obtained for the models in an application-specific environment, are supported by the values for the minimum and maximum percentage error on die-junction temperature reported in Table 3. Overall, all the compact models seem able to predict the die-junction temperature rise in this particular environment to within ± 15 to $\pm 20\%$.

The agreement between the detailed and compact models for the PowerPC 604 microprocessor is much closer than for the PowerPC 603 microprocessor. A thermal budget on the PowerPC 604 microprocessor revealed that between 80% and 95% of the heat enters the heat sink, with the higher figure obtained for the low conductivity board at the lowest flowrate. As almost all the heat is dissipated through the heat sink, the thermal resistance of this heat flow path controls the temperature of the package. The heat sink attach itself has a thermal resistance of 0.51°C/W, some 20 times the R12 resistance. Clearly, the external resistances dominate the predicted temperature rises making the results insensitive to the model used for the package. As the R12 resistance is the same in all the compact models the results obtained in this environment are nearly identical.

SUMMARY AND CONCLUSIONS

As the intrinsic package conduction thermal resistance for this C4/CBGA interconnect technology is very low, proper thermal control is primarily dependent upon the system-level design. However, for the PowerPC 603 microprocessor where the interaction of the package and the board plays a greater role in determining the package die-junction temperature a more reliable network model is desirable. The requirement to use a heat sink with the PowerPC 604

microprocessor makes any of the above models suitable for design purposes.

The Method III models C5, C6, C11 and C12 are clearly superior to the star networks considered here. However, the performance of these models in a wind tunnel environment has yet to be assessed. This is identified as one of a number of future work items. Others include examining the behavior of compact models of the 208-lead PQFP reported in [9] and the 273-pin CPGA in [8].

ACKNOWLEDGMENTS

REFERENCES

1) PowerPC 604 RISC Microprocessor Hardware Specifications, Motorola, 1995.

2) PowerPC 603 RISC Microprocessor User's Manual, IBM/Motorola, 1994.

3) Motorola's PowerPC 603™ and PowerPC 604™ RISC Microprocessor: the C4/Ceramic-ball-grid Array Interconnect Technology, Gary B. Kromann, et.al., Proceedings of the 45th Electronic Components & Technology Conf., May 1995

4) Thermal Management of a C4/Ceramic-Ball-Grid Array: The Motorola PowerPC 603™ and PowerPC 604™ RISC Microprocessors, Gary B. Kromann, SEMITHERM-96, March 1996

5) The Effect of Solder-joint Temperature Rise on Ceramic-Ball-Grid Array to Board Interconnection Reliability: Motorola PowerPC 603™ and PowerPC 604™ Microprocessors and MPC 105 Bridge/Memory Controller,R.D. Gerke and Gary B. Kromann, ASME/JSME INTERpack-95, March 1995

6) "DELPHI - A Status Report on the European-funded Project for the Development of Libraries and Physical Models for an Integrated Design Environment", H Rosten, Presented at 46th Electronic Components & Technology Conference, Orlando, May 28-31 1996.

7) "Rjc Characterisation of Chip Packages - Justification, Limitations and Use", A Bar-Cohen, T Elperin and Reliasi, IEEE Trans. CHMT, Vol 12, pp 724-731, 1989.

8) "Thermal Modelling of the Pentium Processor Package", H I Rosten and R Viswanath, Proceedings of the 44th Electronic Components & Technology Conference, Washington DC, 1-4 May 1994, pp 421-428.

9) "Development, Validation and Application of a Thermal Model of a Plastic Quad Flat Pack", H Rosten, J Parry, S Addison, R Viswanath, M Davies and E Fitzgerald, Proceedings of the 45th Electronic Components & Technology Conference, Las Vegas AZ, May 1995, p1140-1151

10) "Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)", EIA/JEDEC Standard EIA/JESD51-2, December 1995

11) "Package Thermal Resistance Model Dependency on Equipment Design", J. Andrews, IEEE Components, Hybrids, and Manufacturing Technology, vol. 11, No. 4, pp. 528-537, Dec. 1988.

12) "Microelectronic Device Thermal Resistance: A Format for Standardization", R. Hanneman, Heat Transfer in Electronic Equipment, ASME HTD-20, pp. 39-48, 1981.

13) "Thermal Characteristics of IC Packages", P C Lin and L I Nquyen, Presented at EUROTHERM Seminar 29, Delft, The Netherlands, 14-16 June 1993.

14) "Thermal Modeling and Experimental Characterization of the C4/Surface-Mount-Array Interconnect Technologies", Gary B. Kromann, IEEE Transactions on Components, Packaging, and Manufacturing Technology, March 1995

15) "A Hi-Density C4/CBGA Interconnect Technology for a CMOS Microprocessor," Gary B. Kromann, et.al., IEEE Transactions on Components, Packaging, and Manufacturing Technology, Feb. 1996

16) Motorola Customer Version of "C4 Product Design Manual-Volume I: Chip and Wafer Design," Motorola C4 Product Design Center, Austin, TX, 1993.

17) Motorola Customer Version of "C4 Product Design Manual-Volume 2: Packaging Design" Motorola C4 Product Design Center, Austin, TX, 1994.

18) "Controlled Collapse Chip Connection (C4) - An Enabling Technology", Keith DeHaven and Joel Dietz, Proceedings of the 44th Electronic Components & Technology Conference, Washington, D.C., May 1-4, 1994, pp. 1-6.

19) "Ceramic Solder-Grid-Array Interconnection Reliability Over a Wide Temperature Range," R.D. Gerke, Proceedings of NEPCON/West '94, Anaheim, CA, February 27 - March 4, 1994, pp 1087 - 1094.

20) FLOTHERM® User's Guide, Version 1.4; Flomerics Limited; Surrey, England, 1993

21) "A Novel Approach for the Thermal Characterization of Electronic Parts", C Lasance, H Vinke, H Rosten and K-L Weiner, 11th SEMI-THERM, San Jose CA, February 1995.

22) Aavid Thermal Technologies Inc, Part no 340814B00068 with A-Pli thermal interface material. Aavid and A-Pli are trademarks of Aavid Thermal Technologies Inc

APPENDIX

Table 7. PowerPC 603 and PowerPC 604 RISC Microprocessors [1,2]

Microprocessor	Transistors	Performance	Power Dissipation: Typical/Maximum	Die Size	CBGA Substrate Size	CBGA Substrate Balls
		SPECint92/ SPECfp92	(watt)	(mm)	(mm)	
PowerPC603 Microprocessor	1.6 million	75/85	3 @80 MHZ (Full)	7.5x11.5	21x21	255
PowerPC604 Microprocessor	3.6 million	160/165 @100 MHz 225/250 @133 MHz	14.5 to 24.0 @100 to 133 MHz	12.4x15.8	21x21	255

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