UM12416

UJA1023 evaluation board user manual

Rev. 1.0 — 20 January 2026 User manual

Document information

Information	Content
Keywords	UJA1023, local interconnect network (LIN), remote controlled LIN I/O responder, auto bit rate detection, automotive, GPIO, PWM, ADC
Abstract	This user manual describes the usage of the UJA1023 evaluation board (EVB): UJA1023-EVB.

1 Introduction

This user manual describes the usage of the UJA1023 evaluation board (EVB): UJA1023-EVB. The UJA1023 is a fully integrated, remote-controlled local interconnect network (LIN) input/output (I/O) responder IC for common automotive input and output applications. It combines all blocks commonly used in electronic control units (ECU) for I/O handling, such as:

- Automatic bit rate synchronization to any bit rate between 1 kbit/s and 20 kbit/s
- LIN controller
- LIN transceiver
- Oscillator
- I/O block containing eight bidirectional I/O pins with:
  - Pulse width modulation (PWM)
  - Simple 8-bit A/C converter
  - Switch matrix inputs
  - Cyclic sense
- Configurable low-power modes with:
  - Remote LIN wake-up detection
  - Local I/O pin wake-up detection
- LIN node address (NAD) configuration via daisy chain or plugcoding

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on www.nxp.com.

The information page for the UJA1023-EVB (UJA1023 remote controlled LIN I/O responder EVB) is at www.nxp.com/design/design-center/development-boards-and-designs/UJA1023-EVB. The information page provides overview information, documentation, design resources and ordering information. The Design Resources tab provides information schematic and board design files from the UJA1023 evaluation board (UJA1023-EVB), including the downloadable assets referenced in this document.

3 Getting ready

Working with the UJA1023-EVB (UJA1023 remote-controlled LIN I/O responder) requires a LIN commander board as additional hardware.

3.1 Kit contents

- UJA1023-EVB in an antistatic bag
- Quick Start Guide

3.2 Additional hardware

The following hardware is necessary, but not included in this kit:

- 12 V power supply
- LIN bus cable
- LIN commander

The following is a selection of LIN commander hardware options:

- LIN interface tools
- S32K116EVB: S32K116-Q048 evaluation board for automotive general purpose
- S32K144EVB: S32K144-Q100 evaluation board for automotive general purpose
- S32K312MINI-EVB: S32K312MINI-EVB evaluation board for automotive general purpose
- S32K3X4EVB-T172: S32K3X4EVB-T172 evaluation board for automotive general purpose

3.3 Assumptions

Basic knowledge of the LIN Diagnostic and Configuration Specification from LIN Specification Package Revision 2.0, September 2003, is expected.

3.4 Static handling requirements

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling. You must use a ground strap or touch the PC case or other grounded source before unpacking or handling the hardware.

4 Getting to know the UJA1023-EVB

4.1 Board features

The UJA1023-EVB incorporates a user switch panel application example, which consists of:

- UJA1023 remote controlled LIN I/O responder IC
- 2x4 switch matrix (eight buttons)
- LED background light
- Photo resistor sensor input
- DIP switch for NAD configuration
- Supply and bus connector

4.2 Block diagram

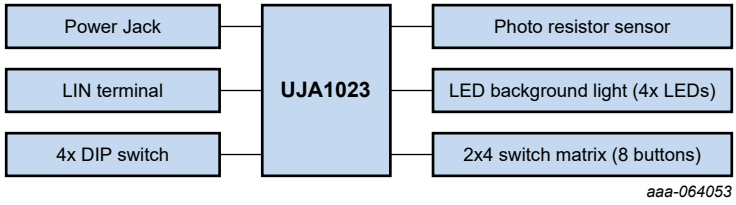

Figure 1. UJA1023-EVB block diagram

4.3 EVB featured components

Figure 2 provides an overview of the UJA1023-EVB and shows the location of the components on the board. Table 1 provides additional details about these components.

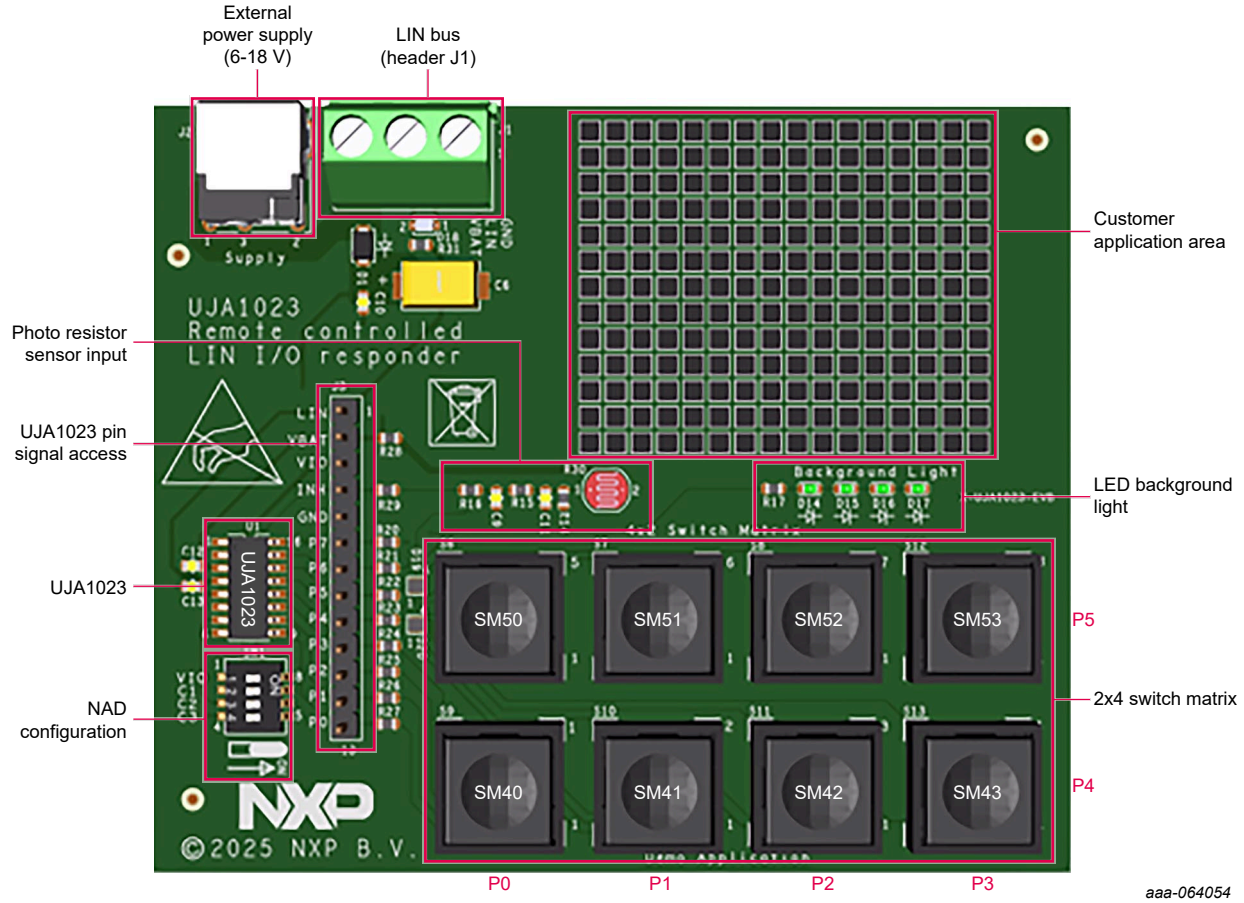

Figure 2. Frontside of UJA1023-EVB

Table 1. Evaluation board featured components

Name	Description
External power supply	Power supply connector for the UJA1023-EVB
LIN bus	LIN bus connector including alternative power supply terminals
NAD configuration	DIP switch for LIN node address (NAD) configuration and VIO connection to VBAT
UJA1023	Remote controlled LIN I/O responder IC: UJA1023
UJA1023 pin signal access	Connector to provide access to UJA1023 pins
2x4 switch matrix	Switch panel application circuit with eight buttons
LED background light	Background light application with 4x LEDs
Photo resistor sensor input	ADC application circuit with photo resistor sensor input signal
Customer application area	Area for application prototyping

4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the UJA1023 evaluation board (UJA1023-EVB) are available at www.nxp.com/design/design-center/development-boards-and-designs/UJA1023-EVB.

4.4.1 Supply circuit

The connectors J1 and J2 are populated on the PCB.

The power jack J2 is used to supply the UJA1023-EVB (max 16 V), where terminal J2-1 is the battery supply and terminal J2-2 is ground. As an alternative, LIN bus connector terminal J1-1 (ground) and J1-3 (battery supply) can be used to supply the UJA1023. The supply connectors are protected against false polarity with diode D1.

The LIN terminal is the LIN bus connector terminal J1-2.

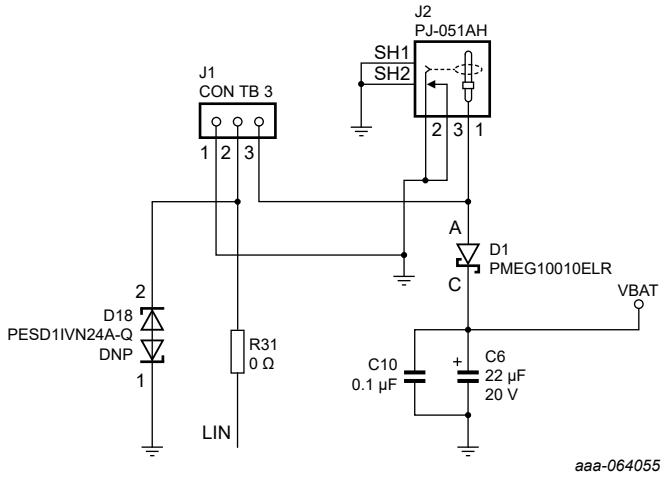

Figure 3. Supply circuit

Table 2. Power jack J2

Connector pin	Signal	Description
J2-1	VPS	Power supply (max 16 V)
J2-2, J2-3	GND	Ground

Table 3. LIN bus connector J1

Connector pin	Signal	Description
J1-1	GND	Ground
J1-2	LIN	LIN bus
J1-3	VPS	Power supply

4.4.2 UJA1023 circuit

Except for pins C1, C2, and C3, all UJA1023 pins are accessable via the not-populated connector J3. Details are listed in Table 4. Most of the signals are connected to EVB application circuits via 0 Ω resisitors. By removing the 0 Ω resistors, the UJA1023 I/Os can be made available for other customer application circuits. The UJA1023 provides a customer application area for this purpose.

The SW1 DIP switch connects the pins C1 (SW1-2), C2 (SW1-3), and C3 (SW1-4) to ground. This provides an option to adapt the LIN node address of the UJA1023.

SW1-1 sets the VBAT supply as reference for the VIO pin. Close SW1-1 to run the application on the UJA1023-EVB. Open SW1-1 to disconnect from VBAT supply if the user wants to use another reference voltage for pin VIO.

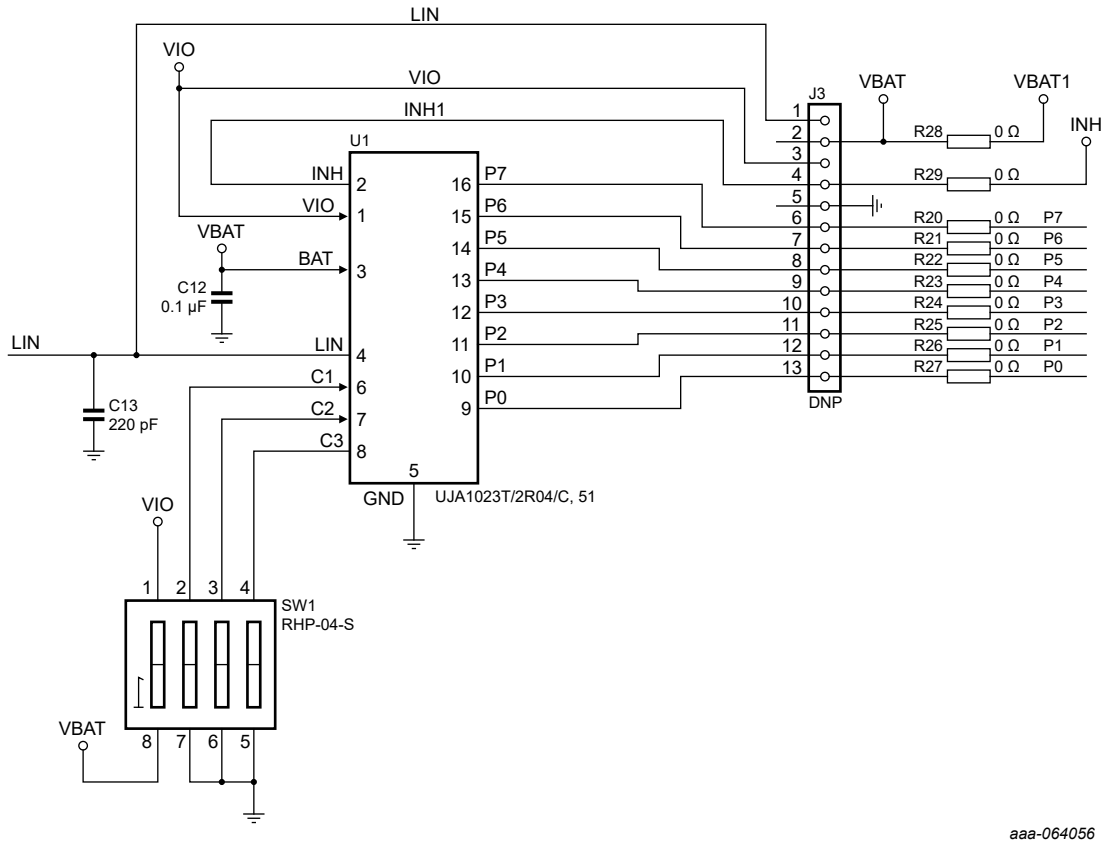

Figure 4. UJA1023 circuit

Table 4. Connector J3

Connector pin	Signal	Description
J3-1	LIN	LIN bus signal
J3-2	VBAT	Supply voltage on
J3-3	VIO	Reference voltage for the I/O pins P0 to P7
J3-4	INH	Inhibit output for controlling an external voltage regulator or signal for UJA1023 ADC function (on EVB connected to photo resistor circuit)
J3-5	GND	Ground
J3-6	P7	Bidirectional I/O pin 7 (on EVB connected to LED background light circuit)
J3-7	P6	Bidirectional I/O pin 6 (on EVB connected to photo resistor circuit)
J3-8	P5	Bidirectional I/O pin 5 (on EVB connected to 2x4 switch matrix circuit)
J3-9	P4	Bidirectional I/O pin 4 (on EVB connected to 2x4 switch matrix circuit)
J3-10	P3	Bidirectional I/O pin 3 (on EVB connected to 2x4 switch matrix circuit)
J3-11	P2	Bidirectional I/O pin 2 (on EVB connected to 2x4 switch matrix circuit)
J3-12	P1	Bidirectional I/O pin 1 (on EVB connected to 2x4 switch matrix circuit)
J3-13	P0	Bidirectional I/O pin 0 (on EVB connected to 2x4 switch matrix circuit)

4.4.3 2x4 switch matrix circuit

The switch matrix function of the UJA1023 scans eight buttons via six I/O pins (P0 to P5). The optional diodes D19 and D20 are used to prevent wrong switch detection if multiple buttons are push simultaneously.

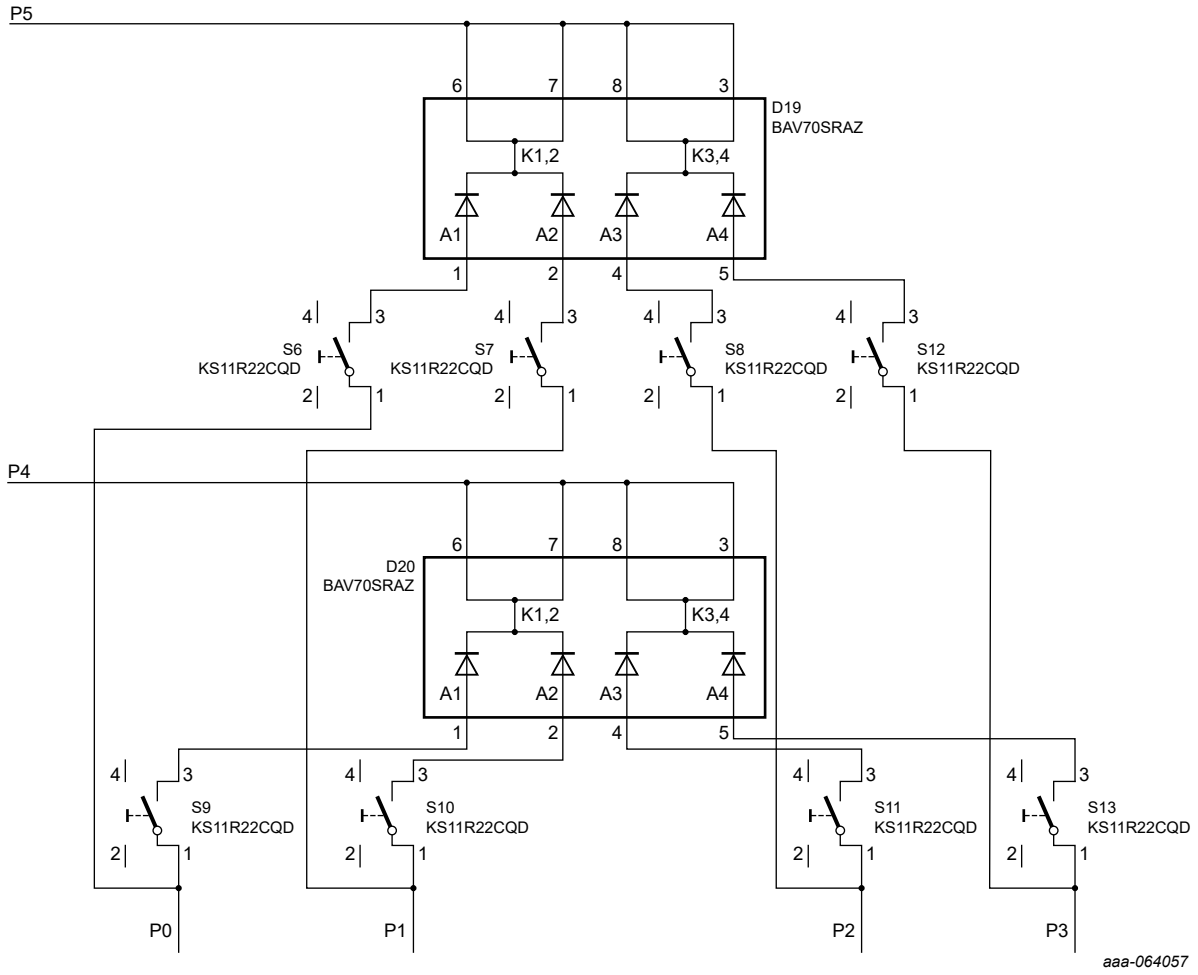

Figure 5. 2x4 switch matrix circuit

Table 5. Button assignment

Button	Description
S6	P5-P0: PxResp frame bit SM50
S7	P5-P1: PxResp frame bit SM51
S8	P5-P2: PxResp frame bit SM52
S12	P5-P3: PxResp frame bit SM53
S9	P4-P0: PxResp frame bit SM40
S10	P4-P1: PxResp frame bit SM41
S11	P4-P2: PxResp frame bit SM42
S13	P4-P3: PxResp frame bit SM43

4.4.4 LED background light circuit

The LED background light application circuit is a series of four LEDs connected to UJA1023 pin P7.

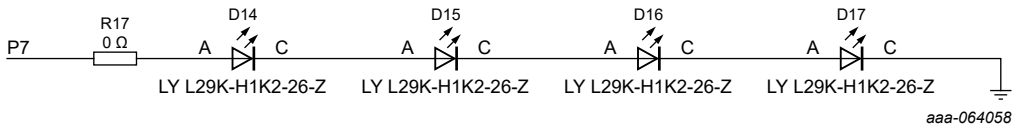

Figure 6. LED background light circuit

4.4.5 Photo resistor sensor input circuit

On the UJA1023-EVB, the analog-to-digital converter (ADC) of the UJA1023 is used for the photo resistor sensor input circuit. A description of the ADC can be found in the UJA1023 data sheet and application note. The ADC value is provided in the LIN responder response frame PxResp byte D3, provided the configuration bits IM0 = 1 and IM1 = 0.

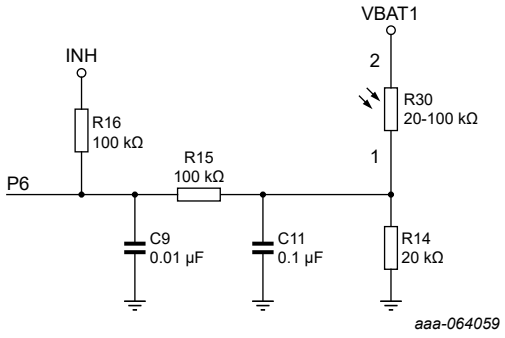

Figure 7. LED background light circuit

5 Configuration example for UJA1023

In this section, an example configuration for the UJA1023 is given for the use of the UJA1023-EVB onboard application examples. For this example, the DIP switch settings are listed in Table 6.

Table 6. DIP switch setting

DIP switch	Setting	Description
SW1.1	On	VBAT supply voltage is used as reference voltage for pin VIO
SW1.2	Off	Pin C1 is high
SW1.3	Off	Pin C2 is high
SW1.4	Off	Pin C3 is high

Table 7 shows the configured LIN protected identifier (PID) for PxReq ID and PxResp ID.

Table 7. UJA1023 LIN message identifier

LIN ID	LIN protected identifier (PID)	Description
16h	D6h	UJA1023 PxReq
17h	97h	UJA1023 PxResp

Table 8 shows an example configuration for the UJA1023-EVB.

Table 8. Example configuration for UJA1023-EVB

LIN configuration service	LIN frame SDU data (hex format)	Description
Assign NAD (Optional)	0F 06 B0 11 00 00 00 67	Plug ID initial NAD: 0Fh; PCI: 06h; SID: B0h; supply ID: 0011h; function ID: 0000h; NAD: 67h (default NAD)
Assign frame ID	67 06 B1 11 00 00 00 D6	NAD: 67h (default NAD); PCI: 06h; SID: B1h; supply ID: 0011h; message ID: 0000h; PID: D6h (LIN ID: 16h)
Data dump (1)	67 06 B4 16 80 80 80 80	NAD: 67h (default NAD); PCI: 06h; SID: B4h; IM: 01b (ADC); RxDL: 0b; ADCIN:110b (P6); HSE: 80h; LSE: 80h; OM0: 80h; OM1: 80h (PWM at P7)
Data dump (2)	67 06 B4 51 00 00 00 00	NAD: 67h (default NAD); PCI: 06h; SID: B4h; LSLP: 0b; TxDL: 1b; SMC: 0b; SMW: 0b; SM: 01b (4 x 2 switch matrix); CM0: 00h; CM1: 00h; TH: 00h; LWM: 00h
Data dump (3)	67 04 B4 81 00 00 FF FF	NAD: 67h (default NAD); PCI: 04h; SID: B4h; LSC: 0b (20 kbit/s); ECC: 1b (enhance checksum); LH: 00h; PWM: 00h

6 Abbreviations

Table 9. Abbreviations

Acronym	Description
ADC	Analog-to-digital converter
ECU	Electronic control unit
EVB	Evaluation board
NAD	Node address
PWM	Pulse width modulation

7 References

[1] **Product data sheet UJA1023, LIN-I/O slave, NXP Semiconductors**
https://www.nxp.com/docs/en/data-sheet/UJA1023.pdf

[2] **Application Note AN10704, UJA1023 LIN I/O slave with automatic bit rate detection** — detailed application information on UJA1023
https://www.nxp.com/docs/en/application-note/AN10704.pdf

8 Revision history

Table 10. Revision history

Document ID	Release date	Description
UM12416 v.1.0	20 January 2026	Initial version

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