UM12319

PF9453 QFN - EVB evaluation board user manual

Rev. 1.0 — 2 May 2025 User manual

Document information

Information	Content
Keywords	PF9453, PMIC, i.MX91X, i.MX93X
Abstract	This document describes the operation of the PF9453 QFN - EVB evaluation board.

1 Introduction

The PF9453 is a single chip Power Management IC (PMIC) designed for i.MX 91 and i.MX 93 processors. It provides power supply solutions for IoT, smart appliance, and portable applications.

This document is the user manual for the PF9453 QFN evaluation kit. It is intended for the engineers involved in the evaluation, design, implementation, and validation of this single PMIC PF9453.

The PF9453 user manual covers information regarding connecting the hardware, installing the software and tools, configuring the environment, and using the kit.

This customer evaluation board provides full access to all the features of the PF9453 device.

2 PF9453 key features

- Four buck regulators:
  - BUCK1: 0.6 V to 3.775 V, 25 mV step, 2000 mA
  - BUCK2: 0.6 V to 2.1875 V, 12.5 mV step, 2700 mA
  - BUCK3: 0.6 V to 3.775 V, 25 mV step, 2000 mA
  - BUCK4: 0.6 V to 3.775 V, 25 mV step, 2500 mA
  - Dynamic voltage scaling on BUCK2.
  - Monitor fault condition.
- Three linear regulators:
  - LDO_SNVS, always-on, with 25 mV step, 10 mA.
  - LDO1, 0.8 V to 3.3 V with 25 mV step, 250 mA, voltage selection through SD_VSEL pin.
  - LDO2, 0.5 V to 1.95 V with 25 mV step, 200 mA.
  - Built-in active discharge resistor.
- One 400 mA load switch with a built-in active discharge resistor and GPIO/I2C control, multiplexed with DBUS debounce filter.
- 32.768 kHz crystal oscillator driver and buffer output.
- Power control IO:
  - Power ON/OFF control.
  - Standby/Deep Standby/Run mode control.
  - Watchdog reset input.
- Flexible power ON/OFF sequence.
- One-time programmable (OTP) device configuration.
- Built-in active discharge resistor.
- Fm+ 1 MHz I2C interface.
- ESD protection:
  - Human body model (HBM): ±2000.
  - Charged device model (CDM): ±500 V.
- Available in:
  - 40-pin QFN, 5 mm x 5 mm, 0.4 mm pitch.

Note: *The output current of the BUCK regulators in the PF9453 varies according to the part number. Refer to Table 1 of the PF9453 QFN data sheet for more details.*

3 Applications

- IoT Devices

- White goods appliances
- Industrial applications
- Portable devices

4 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for evaluation boards and its supported device(s) on http://www.nxp.com.

The information page for evaluation boards is PF9453 QFN Evaluation Board | NXP Semiconductors.

The information page provides overview information, documentation, software, and tools, parametric, ordering information, and a getting started tab. The getting started tab provides quick-reference information applicable to these evaluation boards, including the downloadable assets referenced in this document.

4.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic. The NXP community is at http://community.nxp.com.

5 Getting ready

Working with this evaluation board requires the evaluation kit components, additional hardware, and a Windows PC workstation with installed software.

5.1 Evaluation kit components

- One PF9453 evaluation board, which allows the evaluation of functions and features.
- One USB-Type C cable.

5.2 Additional hardware

In addition to the kit components, the following hardware are recommended when working with this kit.

- Power supply with a range of 2.7 V to 5.0 V and a current limit set initially to 1.0 A (maximum power consumption at default voltages can be up to 22 W).
- Oscilloscope/multimeter.
- Electronic load (optional) - each power rail output can be connected to electronic load for testing.

5.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should provided the expected outcome when working with this evaluation board.

- USB-enabled computer with Windows 7, Windows 8, or Windows 10

5.4 PF9453-EVK GUI software

Installing software is necessary to work with this evaluation board.

- Go to PF9453 EVB graphical user interface.
- Extract the Evaluation Kit GUI zip file, PF9453_EVB_GUI_1.25.2.21-x64, into the selected folder. No need to install. (If the password is requested to unzip, type “NXP”.)

- Install the FTDI D2XX direct drivers from https://www.ftdichip.com/Drivers/D2XX.htm
- Run the file PF9453.exe. The interface window is shown in Figure 1.

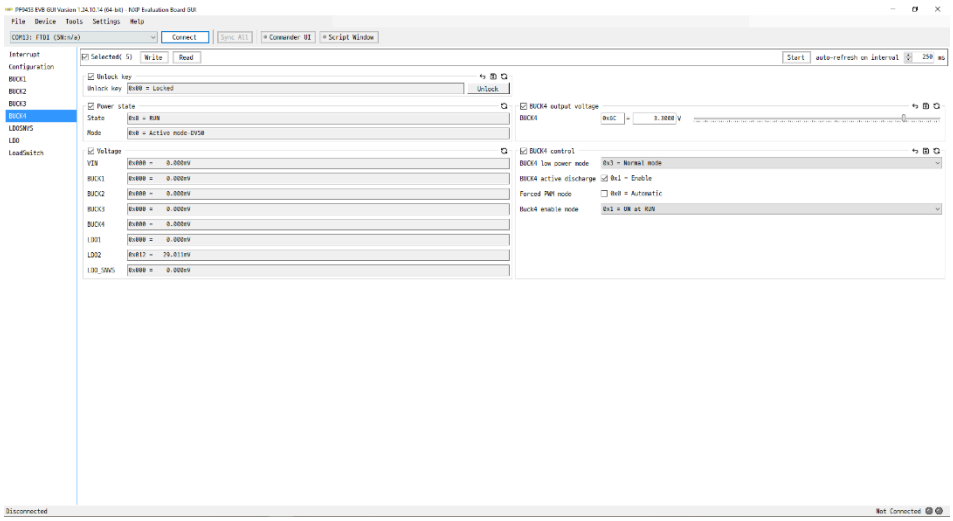

Figure 1. Interface window

6 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic ICs and system-in-package devices that use proven high-volume technology.

6.1 Kit overview

This evaluation board features the PF9453 PMIC. The kit integrates all hardware needed to evaluate the PMIC and a communication bridge based on FTDI to interface with the PF9453 GUI software interface to configure and control the PMIC.

6.1.1 Evaluation board features

- Four BUCK regulators:
  - One 2.7 A BUCK regulator with DVS.
  - Two 2 A BUCK regulators.
  - One 2.5 BUCK regulator.
  - Three linear regulators:
    - One 10 mA LDO.
    - One 250 mA LDO.
    - One 200 mA LDO.
  - 400 mA load switch with a built-in active discharge resistor.
  - 32.768 kHz crystal oscillator driver and buffer output.
  - System features:
    - 2.7 V to 5.5 V operating input voltage range.
    - Power ON/OFF control.
    - Standby/Deep Standby/Run mode control.
    - Smart DVS control.
    - Interrupt configuration.

– Fm+ 1 MHz I2C interface (via FTDI USB to I2C IC).

6.2 Kit featured components

Figure 2 helps to identify the different main sections on the board.

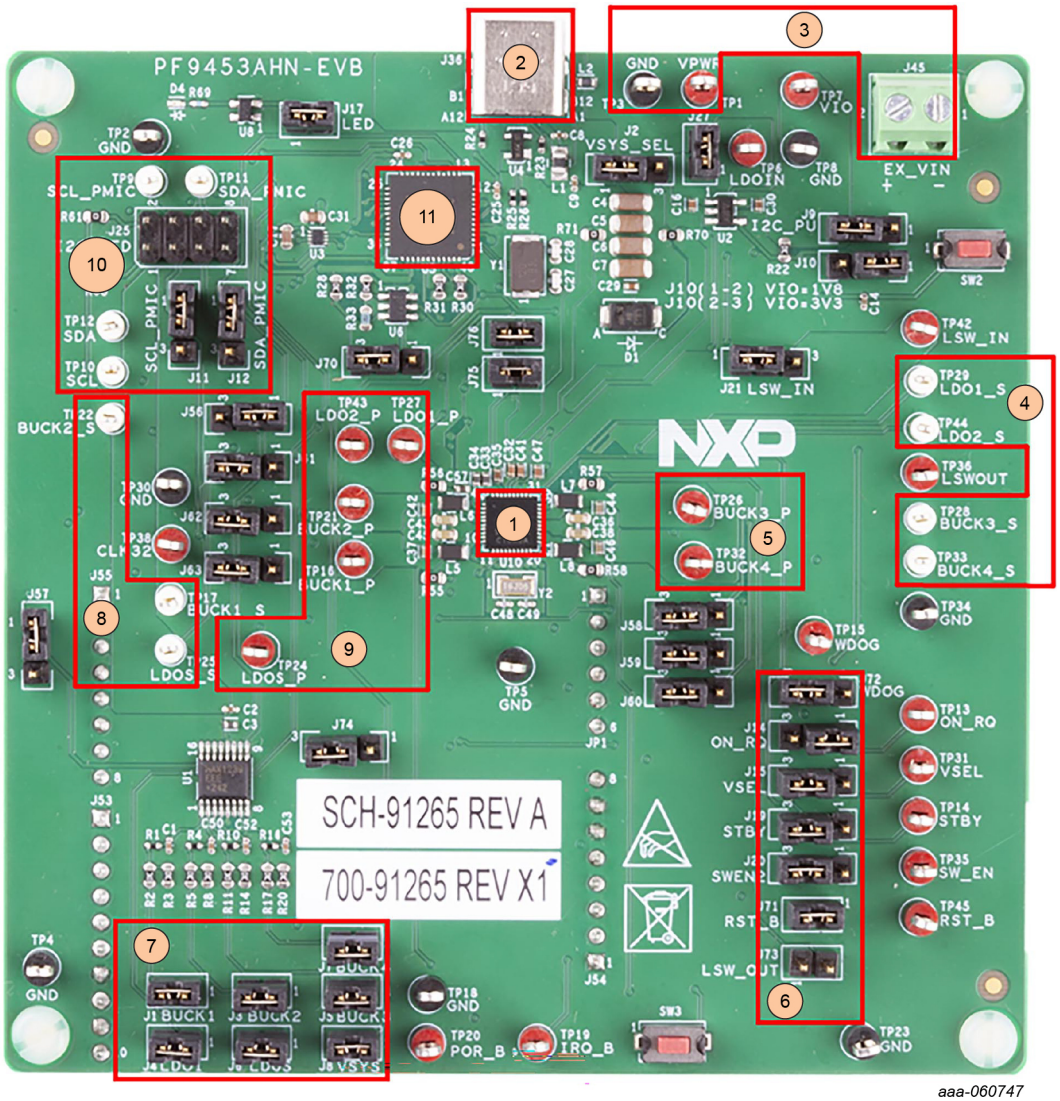

Figure 2. Evaluation board featured component locations

1. PF9453 PMIC (QFN package).
2. USB type C connector.
3. VPWR and GND input power connectors.
4. LDO1, LDO2, BUCK3 and BUCK4 sensing test points.
5. BUCK3 and BUCK4 power test points.
6. Digital signals jumper selectors.
7. ADC jumpers.

8. BUCK1, BUCK2 and LDO_SNVS sensing test points.
9. LDO1, LDO2, LDO_SNVS, BUCK2 and BUCK1 power tests points.
10. I2C headers and tests points.
11. FTDI (I2C to USB IC)

6.3 Default jumper configuration

Figure 3 shows the default jumper configuration of the board.

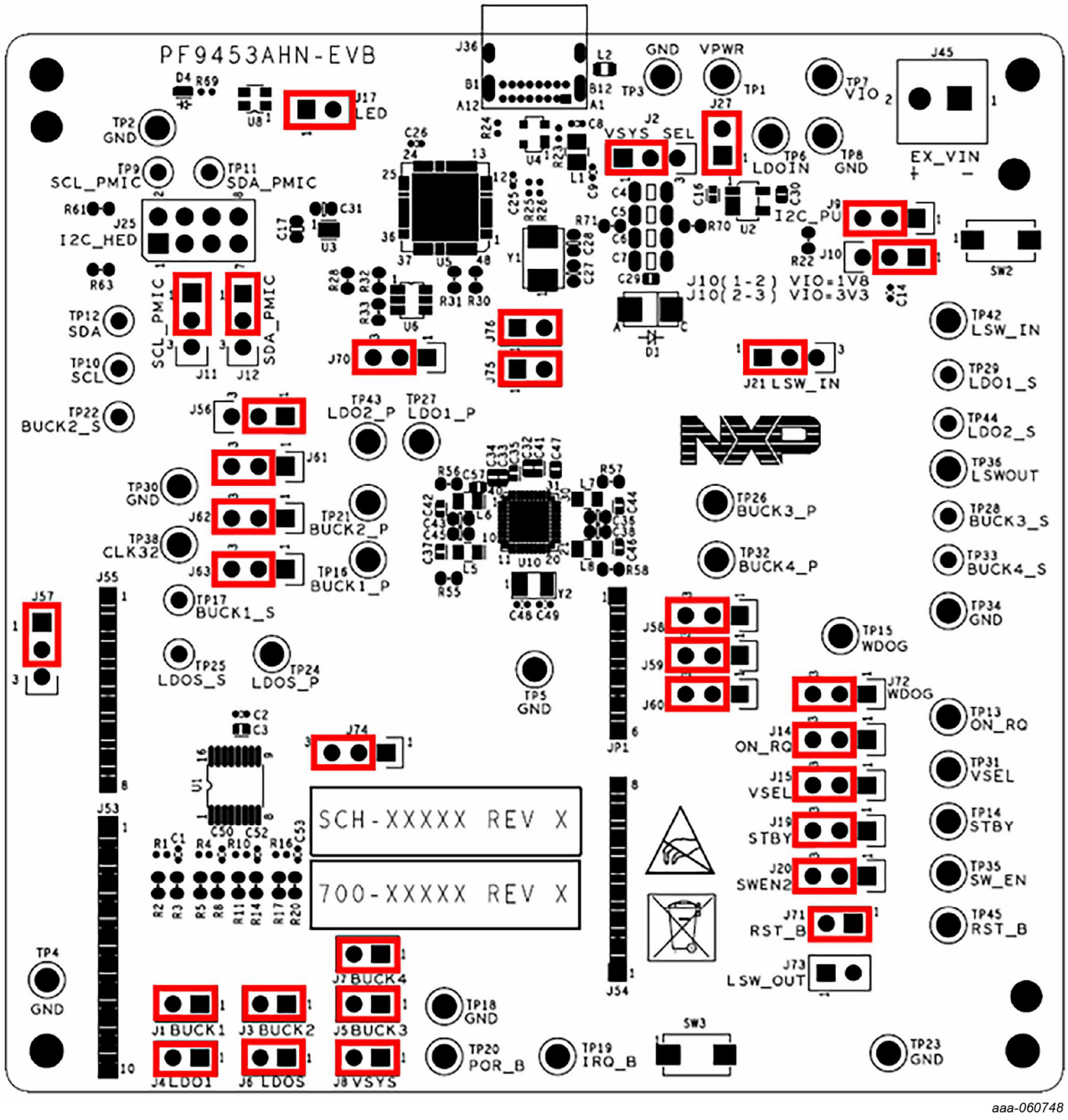

Figure 3. Evaluation board default jumper configuration

Table 1. Evaluation board jumper descriptions

Name	Default	Description
J1	CLOSED	Connects BUCK1_OUT voltage to ADC0 channel.
J2	1 to 2	Select source voltage for VSYS and PSYS (PMIC input voltage): • 1 to 2 → PMIC input voltage comes from the USB type C connector. • 2 to 3 → PMIC input voltage comes from external connector (J45) or test points (TP1 and TP3)
J3	CLOSED	Connects BUCK2_OUT voltage to ADC1 channel.
J4	CLOSED	Connects LDO1_OUT voltage to ADC4 channel.
J5	CLOSED	Connects BUCK3_OUT voltage to ADC2 channel.
J6	CLOSED	Connects LDO_SNVS voltage to ADC5 channel.
J7	CLOSED	Connects BUCK4_OUT voltage to ADC3 channel.
J8	CLOSED	Connects PSYS voltage to ADC6 channel.
J9	2 to 3	Select source voltage for VIO (Voltage for input and output signals): • 1 to 2 → VIO source voltage is LDO_SNVS. • 2 to 3 → VIO source voltage is an external LDO (U2)
J10	1 to 2	Select output voltage of the external LDO (U2): • 1 to 2 → External LDO output voltage = 1.8 V • 2 to 3 → External LDO output voltage = 3.3 V
J11	1 to 2	Select if SCL_PMIC signal (PMIC I2C signal) passes through the level shifter (U3) or not: • 1 to 2 → SCL_PMIC signal passes through level shifter (U3) • 2 to 3 → SCL_PMIC signal does not passes through level shifter (U3)
J12	1 to 2	Select if SDA_PMIC signal (PMIC I2C signal) passes through the level shifter (U3) or not: • 1 to 2 → SDA_PMIC signal passes through level shifter (U3) • 2 to 3 → SDA_PMIC signal does not passes through level shifter (U3)
J14	2 to 3	Select PMIC_ON_REQ level: • 1 to 2 → PMIC_ON_REQ = High (start power-up sequence) • 2 to 3 → PMIC_ON_REQ = Low (start power-down sequence)
J15	2 to 3	Select SD_VSEL level: • 1 to 2 → SD_VSEL = High (LDO5 = 1.8 V default output) • 2 to 3 → SD_VSEL = Low (LDO5 = 3.3 V default output)
J17	CLOSED	Connects the green LED driver (U8) to PSYS voltage.
J19	2 to 3	Select PMIC_STBY_REQ level: • 1 to 2 → PMIC_STBY_REQ = High • 2 to 3 → PMIC_STBY_REQ = Low
J20	2 to 3	Select LSW_EN level: • 1 to 2 → LSW_EN = High (load-switch ON) • 2 to 3 → LSW_EN = Low (load-switch OFF)
J21	1 to 2	Select load-switch in put voltage: • 1 to 2 → Load switch input voltage = BUCK4. • 2 to 3 → Load switch input voltage = PSYS.
J27	CLOSED	Connects the external LDO (U2) to PSYS voltage.
J56	1 to 2	Select an SCL connection: • 1 to 2 → SCL connected to the FTDI IC.

Table 1. Evaluation board jumper descriptions...*continued*

Name	Default	Description
		• 2 to 3 → SLC connected to J53 Arduino connector.
J57	1 to 2	Select an SDA connection: • 1 to 2 → SDA connected to the FTDI IC. • 2 to 3 → SDA connected to J53 Arduino connector.
J58	2 to 3	Select if PMIC_ON_REQ connection: • 1 to 2 → PMIC_ON_REQ connected to the FTDI IC. • 2 to 3 → PMIC_ON_REQ connected to J55 Arduino connector.
J59	2 to 3	Select if PMIC_STBY_REQ connection: • 1 to 2 → PMIC_STBY_REQ connected to the FTDI IC. • 2 to 3 → PMIC_STBY_REQ connected to J55 Arduino connector.
J60	2 to 3	Select if WDOG_B connection: • 1 to 2 → WDOG_B connected to the FTDI IC. • 2 to 3 → WDOG_B connected to J55 Arduino connector.
J61	2 to 3	Select if IRQ_B connection: • 1 to 2 → IRQ _B connected to the FTDI IC. • 2 to 3 → IRQ _B connected to J55 Arduino connector.
J62	2 to 3	Select if POR_B connection: • 1 to 2 → POR _B connected to the FTDI IC. • 2 to 3 → POR _B connected to J55 Arduino connector.
J63	2 to 3	Select if LSW_EN connection: • 1 to 2 → LSW_EN connected to the FTDI IC. • 2 to 3 → LSW_EN connected to J55 Arduino connector.
J70	2 to 3	Select if SD_VSEL connection: • 1 to 2 → SD_VSEL connected to the FTDI IC. • 2 to 3 → SD_VSEL connected to J55 Arduino connector.
J71	CLOSED	Connects PMIC_RET_B to the reset button (SW3).
J72	2 to 3	Select WDOG_B (watchdog reset input) signal: • 1 to 2 →WDOG_B = High (normal operation) • 2 to 3 → WDOG_B = Low (pull-down to GND and start a WDOG_B function that can be configure by i2C in the WDOG_B registers)
J73	OPEN	Jumper for internal valiation only.
J74	2 to 3	Select if PMIC_RST_B connection: • 1 to 2 → PMIC_RST_B connected to the FTDI IC. • 2 to 3 → PMIC_RST_B connected to J53 Arduino connector.
J75	CLOSED	Connects LDO1 input voltage (INL1) to PSYS.
J76	CLOSED	Connects LDO2 input voltage (INL2) to PSYS.

6.4 Test points

Use the test points to measure the output voltage signal of the PMIC regulators and load switch by oscilloscope/ multimeter.

Table 2. Table 2. Evaluation board test point descriptions

Name	Signal	Description
TP1	VPWR	Power test point for VPWR voltage (external input voltage for the PMIC)
TP2	GND	GND test point
TP3	GND	GND test point
TP4	GND	GND test point
TP5	GND	GND test point
TP6	PSYS	Sensing test point for input voltage (PSYS) for the external LDO (U2)
TP7	LDO_EXT_ VOUT	Sensing test point for output voltage for the external LDO (U2)
TP8	GND	GND test point
TP9	SCL_PMIC	Sensing test point for SCL_PMIC signal (this I2C signal comes from the PMIC)
TP10	SCL	Sensing test point for SCL signal (this I2C signal comes from lever shifter U3 or jumper J11)
TP11	SDA_PMIC	Sensing test point for SDA_PMIC signal (this I2C signal comes from the PMIC)
TP12	SDA	Sensing test point for SDA signal (this I2C signal comes from lever shifter U3 or jumper J12)
TP13	PMIC_ON_REQ	Sensing test point for PMIC_ON_REQ signal
TP14	PMIC_STBY_ REQ	Sensing test point for PMIC_STBY_REQ signal
TP15	WDOG_B	Sensing test point for WDOG_B signal.
TP16	BUCK1_OUT	Power test point for the BUCK1 output voltage
TP17	BUCK1_OUT	Sensing test point for the BUCK1 output voltage
TP18	GND	GND test point
TP19	IRQ_B	Sensing test point for IRQ_B signal
TP20	POR_B	Sensing test point for POR_B signal
TP21	BUCK2_OUT	Power test point for the BUCK2 output voltage
TP22	BUCK2_OUT	Sensing test point for the BUCK2 output voltage
TP23	GND	GND test point
TP24	LDO_SNVS	Power test point for LDO_SNVS output voltage
TP25	LDO_SNVS	Sensing test point for LDO_SNVS output voltage
TP26	BUCK3_OUT	Power test point for the BUCK3 output voltage
TP27	LDO1	Power test point for LDO1 output voltage
TP28	BUCK3_OUT	Sensing test point for the BUCK3 output voltage
TP29	LDO1	Sensing test point for LDO1 output voltage
TP30	GND	GND test point
TP31	SD_VSEL	Sensing test point for SD_VSEL signal.
TP32	BUCK4_OUT	Power test point for the BUCK4 output voltage
TP33	BUCK4_OUT	Sensing test point for the BUCK4 output voltage
TP34	GND	GND test point
TP35	LSW_EN	Sensing test point for LSW_EN signal

Table 2. Table 2. Evaluation board test point descriptions*...continued*

Name	Signal	Description
TP36	LSWOUT	Power test point for LSWOUT voltage
TP38	CLK_32_OUT	Sensing test point for CLK_32_OUT signal
TP42	LSWIN	Power test point for LSWIN voltage
TP43	LDO2	Power test point for LDO2 output voltage
TP44	LDO2	Sensing test point for LDO2 output voltage
TP45	PMIC_RST_B	Sensing test point for PMIC_RST_B signal

6.5 Connectors

6.6 Main input power connectors

Main input power VPWR is supplied using TP1 and TP3 Test points or J45 connector.

Table 3. Main input power connectors

Name	Signal	Description
J45-1	GND	GND test point
J45-2	VPWR	Power test point for VPWR voltage (external input voltage for the PMIC)
TP1	VPWR	Power test point for VPWR voltage (external input voltage for the PMIC)
TP3	GND	GND test point

6.7 FRDM/Arduino connectors

FRDM/Arduino connectors J53, J54 and J55, are used to have access to the digital pins of the PF9453 by using a FRDM or Arduino board to monitor and set. Table Table 4 explains each of the pins included in these connectors.

Table 4. FRMD/Arduino connectors J54, J53, J55

Name	Signal	Type	Description
J54-05	GND	GND	GND
J54-06	GND	GND	GND
J53-01	PMIC_RST_B_FRDM	Input	PMIC reset input pin. Once it is asserted low, PMIC performs cold reset.
J53-07	GND	GND	GND
J53-09	SDA_FRDM	Input/output	Connection to SDA signal
J53-10	SCL_FRDM	Input/output	Connection to SCL signal.
J55-01	PMIC_ON_REQ_FRDM	Input	PMIC ON signal input from an application processor.
J55-02	PMIC_STBY_REQ_FRDM	Input	Standby mode input from application processor.
J55-03	WDOG_B_FRDM	Input	Watchdog reset input from application processor.
J55-04	IRQ_B_FRDM	Output	PMIC interrupt pin, open drain output requiring external pull-up resistor.

Table 4. FRMD/Arduino connectors J54, J53, J55*...continued*

Name	Signal	Type	Description
J55-05	POR_B_ FRDM	Output	Power-on reset output pin. Open drain output requiring external pull-up resistor.
J55-06	LSW_EN_ FRDM	Input	Load switch enable input pin. It has internal 1.5 Ω pull down resistor or output pin for DBUS debounce filter function.
J55-07	SD_VSEL_ FRDM	Input	LDO1 voltage selection input pin. LDO1 output is 3.3 V when it is driven low and 1.8 V when it is driven high.

Note: *The pins are not mentioned in the tables of the J53, J54 and J55 connectors are also not connected to any signal. J25 is a reserved connector for internal validations.*

7 Evaluation kit connections and configuration

7.1 Test setup

Figure 4 shows test setup block diagram.

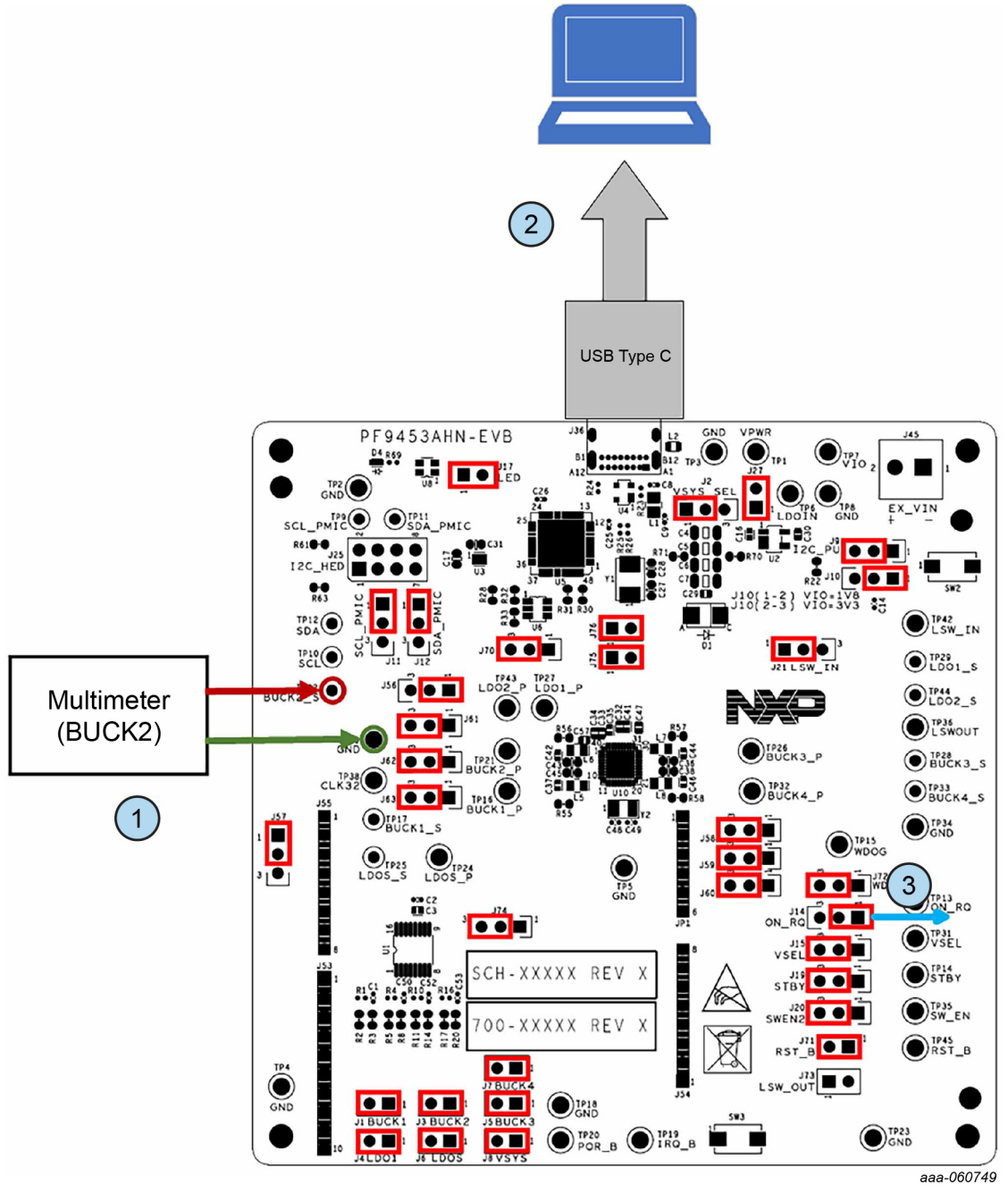

Figure 4. PF9453 EVB test set up

7.2 Configure and power the board

Refer to the Figure 4 and follow the next steps to test the PF9453 QFN – EVB. Make sure that all jumpers are in the default positions before starting. (See section Section 6.3) and no other cables are connected to the PF9453 QFN – EVB:

1. Connect the positive terminal of the multimeter to TP22 (BUCK2_OUT) test point and the negative terminal of the multimeter to TP30 GND test point, see the Figure 4 where step 1 is represented with the circle with number 1.

2. Connect the USB-Type C to the PF9453 QFN –EVB. See that the green LED D4 is ON, refer to Figure 4 circle with number 2.
   Note: *With this configuration, use the USB-Type C connector as the power supply. Consider not connecting loads that may demand more power than the USB-Type C supply can deliver. If tests that could demand more current that the USB-Type C power supply allows must be dione, for example, efficiency tests, it is recommended to use an external power supply. For more details about how to set up, see section 7.4 Using an External power supply. If the USB-Type C power supply is enough, continue with the next step.*
3. Move the J14 to position J14 (1 to 2), refer to Figure 4, circle with number 3 (this turns on the PMIC by setting the high state the PMIC_ON_REQ pin)
4. Measure the default voltage of BUCK2 in the multimeter, must be 0.85 V (default voltage).

7.3 Default power configuration

The default power configuration can be checked without doing any hardware (HW) or software (SW) modifications. Check the default voltage configuration using a multimeter on BUCK1, BUCK2, BUCK3, BUCK4, LDO1, LDO2, and LDO SNVS test points.

Regulator	PF9453 QFN
BUCK1	1.1 V
BUCK2	0.85 V
BUCK3	1.8 V
BUCK4	3.3 V
LDO1	3.3 V/1.8 V
LDO2	0.8 V
LDO SNVS	1.8 V

7.4 Using an external power supply

Figure 5 shows how to connect an external power supply in the PF9453 QFN – EVB.

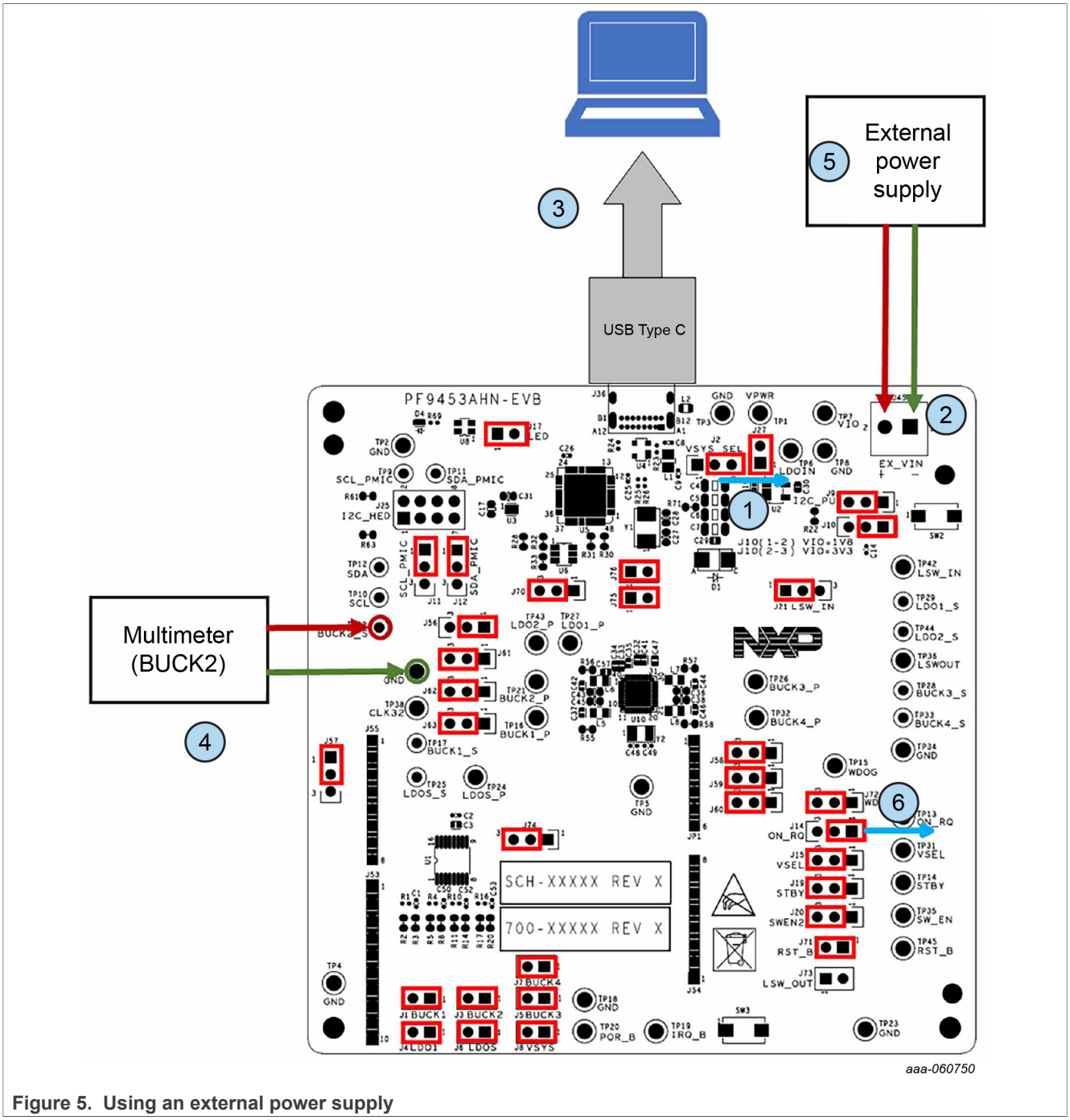

Figure 5. Using an external power supply

Follow the next steps to start testing the PF9453 QFN – EVB with an external power supply. Before starting make sure that all jumpers are in the default position. (See section Section 6.3) and no other cables are connected to the PF9453 QFN – EVB:

1. Move the J2 jumper to position J2 (2 to 3). Input PMIC voltage from an external power supply, see Figure 5. Step 1 is represented with the circle with number 1.
2. Connect the external power supply to the J45 connector: positive terminal to J45 (pin 2), negative terminal J45(pin 1) see Figure 5, circle with number 2. The xternal power supply can also be conneceted to the following tests points: positive terminal to TP1 (VPWR) and negative terminal to TP3 (GND).
3. Connect the USB-Type C to the PF9453-EVB, see Figure 5, circle with number 3.

4. Connect the positive terminal of the multimeter to TP22 (BUCK2_OUT) test point and the negative terminal of the multimeter to TP30 (GND) test point. See Figure 5, circle with number 4.
5. Configure the power supply to 5.0 V, 1 A, and turn it on. See that the green LED D4 is ON, see the Figure 5, circle with number 5.
6. Move the J14 Jumper to position J14 (1 to 2), see Figure 5, circle with number 6. (This turns on the PMIC by setting the high state the PMIC_ON_REQ pin.)
7. Measure the default voltage of BUCK2 in the multimeter, you see 0.85 V (default voltage.)

8 PF9453 QFN GUI

8.1 GUI Overview

As shown in Figure 6, the PF9453 software GUI is a tool to access the on-chip registers to perform write/read commands manually or automatically (depending on different settings chosen from the GUI). The following is a guide of the key blocks that the PF9453 software GUI provides.

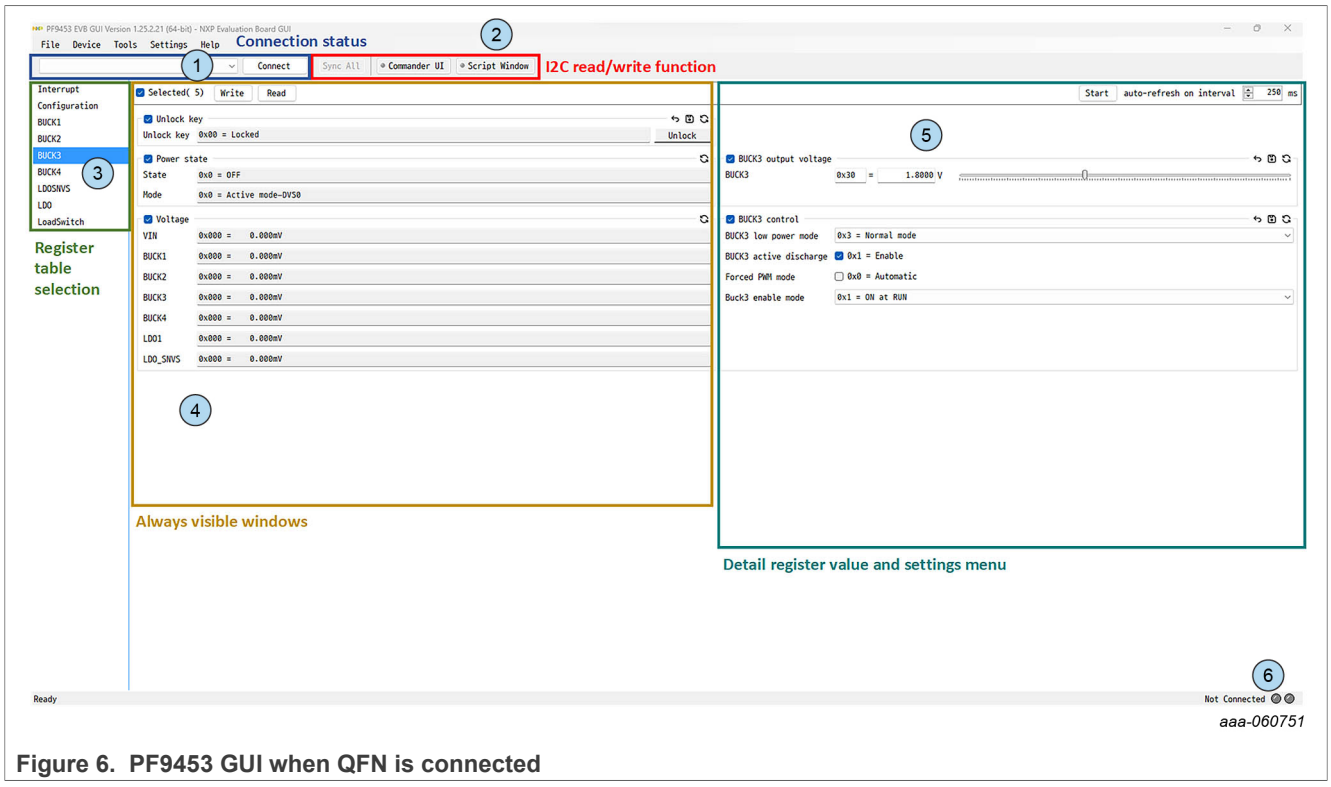

Figure 6. PF9453 GUI when QFN is connected

Note: *The GUI supports WCLSP and QFN packages. Depending on the EVB, the GUI automatically detects which it is and it displays the registers available for this package.*

8.2 GUI setup

After plugging in the USB-Type C cable as is mentioned in Section 7, the GUI should detect the EVB.

Select the driver type (FTDI Sn: n/a) from the drop-down menu on Connection status (see Figure 6, number 1), and then click the **Connect** button.

If the connection was successfully done, see in the interrupt sheet: the device ID information (see Figure 6, number 5), the name of the device PF9453, the revision of the devices, that is, 0x0 and the green button with the legend “connected” (see Figure 6, number 6).

Note: *If there is an issue connecting with the PF9453 GUI be sure you have the FTDI drivers installed, refer to section Section 5.4 for more details.*

8.3 Register table section

The registers are categorized as shown below:

- INTERRUPT – Includes status registers of Interrupts source, voltage regulator fault, OTP version information and device ID information.
- CONFIGURATION – system configuration, reset behaviors, UVLO threshold, and clock driver enable register.
- BUCK1 – Includes all the configuration registers for BUCK1.
- BUCK2 – Includes all the configuration registers for BUCK2 including DVS.
- BUCK3 – Includes all the configuration registers for BUCK3.
- BUCK4 – Includes all the configuration registers for BUCK4.
- LDOSNVS – Includes all the configuration registers for LDO SNVS.
- LDO – Includes all the configuration registers for LDO1 and LDO2.
- Load switch – Includes all the configuration registers for the load switch.

8.4 Always-visible window

PF9453 GUI has an always-visible window (see Figure 6, number 4.) This window allows to see the unlocked key and power state registers plus the measurement of each voltage of the PMIC regulators. The following are descriptions of each of these sections:

- Unlock key register: These registers lock and unlock the registers related to the voltage level of each regulator, for more details refer to the PF9453 data sheet.
- Power state register: This registers allows to see the state of the PMIC for example RUN, STBY, OFF. For more details refer to PF9453 Datasheet.
- Voltage: PF9453 QFN – EVB has an ADC IC connected to different voltages in the board. Those voltages are shown in the current section. The voltages measurements can be refreshed by the read button on this section or the auto refresh button at the top right of the GUI.

For more details about the ADC, connection refer to the SCH file of the PF9453 QFN – EVB.

8.5 I2C read and write

PF9453 software GUI provides three ways to read and write.

1. On register table, click the **read/write** button for the whole table, or click:

   
   For Write

   
   For Read

2. Command. Read or write the hex value to a specific register.
3. Script. Run the script to read or write a series of registers. Using guideline can be found in the help menu.

9 PF9453 evaluation steps

The following sections show how to perform an evaluation of the PF9453 using the evaluation board and the software GUI.

9.1 Jumper configuration

This step must be done with the USB-Type C cable disconnected. Connect the jumpers in the default configuration as shown in section Section 6.3.

9.2 Connect and power the board

As shown in Figure 4 of the section Section 7.1 connect the USB-Type C cable and follows the steps of Section 7.2, if an external power supply is needed for especial test, i.e., efficiency tests refer to section Section 7.4.

9.3 Working on the PF9453 software GUI

Open, setup, and connect the GUI as directed in Section 8.2 then configure the PMIC using the different tabs. In the always visible-window, press the **read** button on the voltage section to see the voltage level of each regulator and see the default voltage of them.

9.3.1 Buck configuration

Select the BUCKx tab from the register table selection.

Click the **unlock** button in the always visible window (see Figure 6 , number 4), to unlock the regulator registers.

From here: Change all the configuration registers for all the buck regulators of the PF9453, then configure the low power modes. Enable the active discharge resistor, use forced PWM, and change enable modes. Finally, configure the DVS speed (for BUCK2), and change output voltages by either by writing the value or using the horizontal slide bar.

Use the multimeter to check the voltage on the buck test points to confirm the voltage changes when finished.

9.3.2 LDO configuration

Select the ‘LDOx’ tab from the register table selection.

Be sure the **unlock** button in the Aways-visible window (see Figure 6, number 4) is enabled.

From here: Change all the configuration registers for all the LDO regulators of the PF9453, configure the low power modes, and enable the active discharge resistor. Change enable modes, and change output voltages by either by writing the value or using the horizontal slide bar.

Use the multimeter to check the voltage on the buck test points to confirm the voltage changes when finished.

9.3.3 Load-switch configuration

Select the Load switch tab from the register table selection.

From here: It is possible to change all the configuration registers for the load switch of the PF9453, enable the active discharge resistor, change enable modes, and configure the different protection mechanisms.

9.3.4 GUI close

Click the **disconnect** button and disconnect the USB cable from the PC and close the PF9453 GUI.

10 Revision history

Table 5. Revision history

Document ID	Release date	Description
UM12319 v.1.0	2 May 2025	Initial version

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents