UM12269

SJA1110 multi-gig secure evaluation board

Rev. 1.0 — 28 April 2025 User manual

Document information

Information	Content
Keywords	SJA1110, SJA1110A, SJA1110B, SJA1110C, SJA1110D, SJA1110-MGS-EVM, evaluation board, TJA1121, TJA1104, SMI, SPI, MACsec, TC10
Abstract	This document describes the operation of the SJA1110-MGS-EVM evaluation board.

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1 Introduction

This document is the user guide for the SJA1110-MGS evaluation board (SJA1110-MGS-EVM). The SJA1110-MGS-EVM is a compact, cost-effective multi-gig secure evaluation board, ideal for automotive Ethernet use cases. Consisting of the SJA1110 switch along with TJA1121 and TJA1104 PHYs, the board demonstrates MACsec security on both PHYs and enables rapid prototyping with integrated software examples based on Real-Time Drivers (RTDs).

Note that this board is not intended to be used for PMA testing of the internal and external PHYs. Signals that would be needed to take such measurements are not available at the SMA connectors.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for their evaluation board and supported device(s) on nxp.com.

The information page for the SJA1110-MGS-EVM is at http://www.nxp.com/SJA1110-MGS-EVM. The information page provides overview information, product details, documentation, software and tools.

3 Getting ready

The supplied kit contents, additional hardware and a Windows PC workstation with installed software are needed to work with the SJA1110-MGS-EVM.

3.1 Kit contents

- Assembled and tested SJA1110-MGS-EVM evaluation board in an antistatic bag
- Twisted-pair cable with MATEnet connectors
- Quick start guide

4 Getting to know the hardware

4.1 Board image

A top view of the SJA1110-MGS-EVM is shown in Figure 1. Board dimensions are 105 mm x 118 mm.

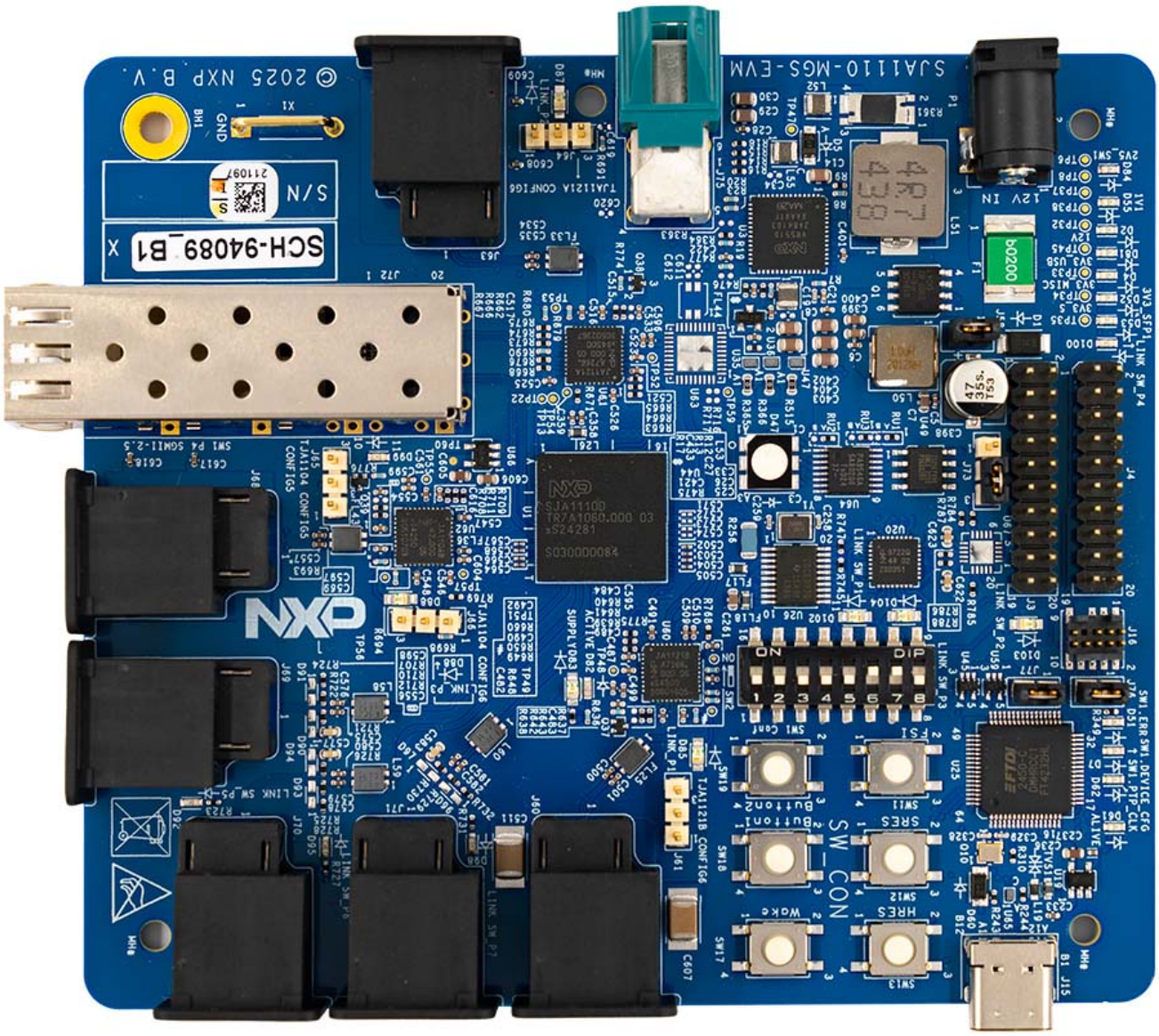

Figure 1. SJA1110-MGS-EVM

4.2 Board features

- SJA1110D secure variant
- Power supply based on VR5510 PMIC using a single 12 volt input
- Ethernet ports:
  - 3x 100BASE-T1 (SJA1110 internal PHYs)
  - 1x 100BASE-T1 Ethernet port using the TJA1104B automotive Ethernet PHY
  - 2x 1000BASE-T1 Ethernet port using the TJA1121A/B automotive Ethernet PHY
  - 1x SFP+ cage
  - 1x 2.5G Ethernet port using the TJA1230 automotive Ethernet PHY (not available on Rev. 1.0 of the board)
  - JTAG connector to access ARM core of SJA1110
  - Several LEDs controlled by HW and SW displaying useful information
  - Multiple DIP switches to change specific settings
  - USB-C connector for SPI access

4.3 Block diagram

A block diagram of the SJA1110-MGS-EVM is shown in Figure 2.

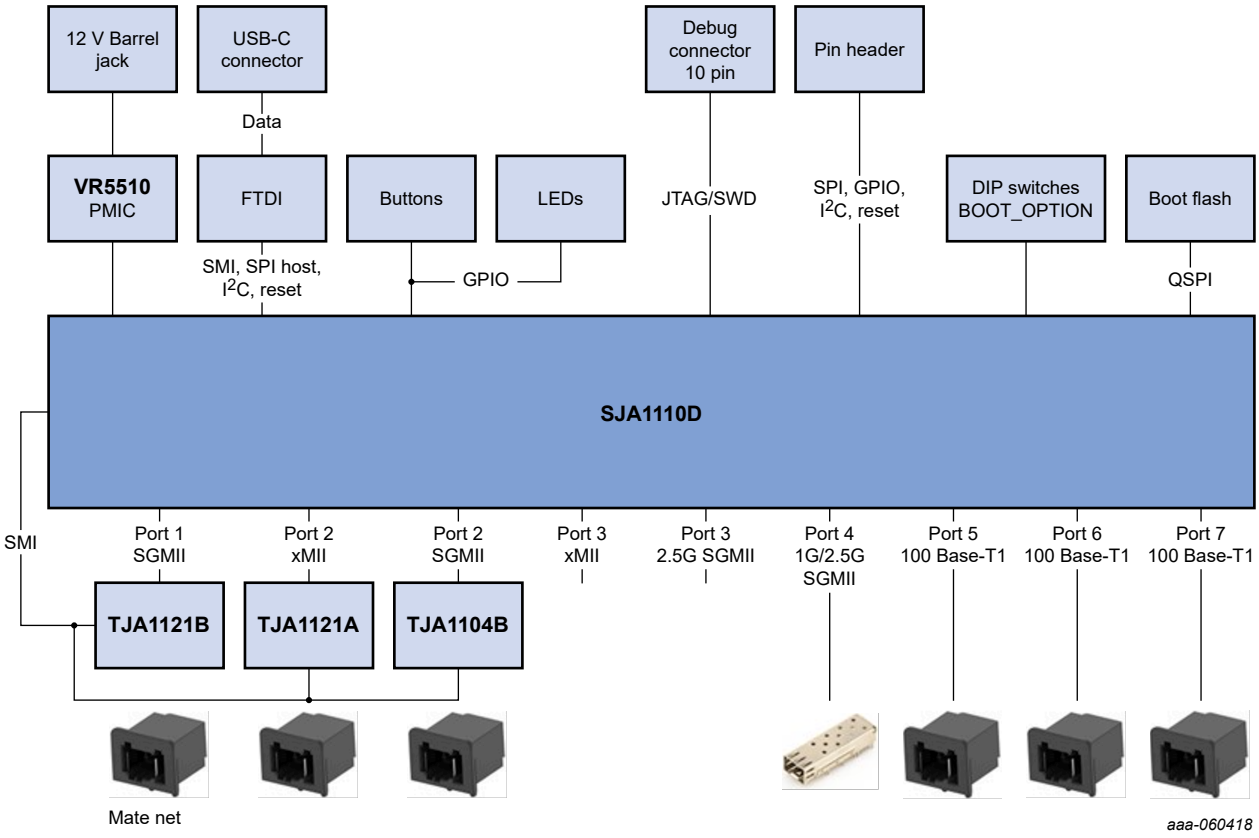

Figure 2. Block diagram of the SJA1110-MGS-EVM evaluation board

4.4 Board overview

The main components and ports on the SJA1110-MGS-EVM are indicated and labelled in Figure 3. Jumpers and DIP switches are highlighted in Figure 4 and described in Table 1 and Table 2.

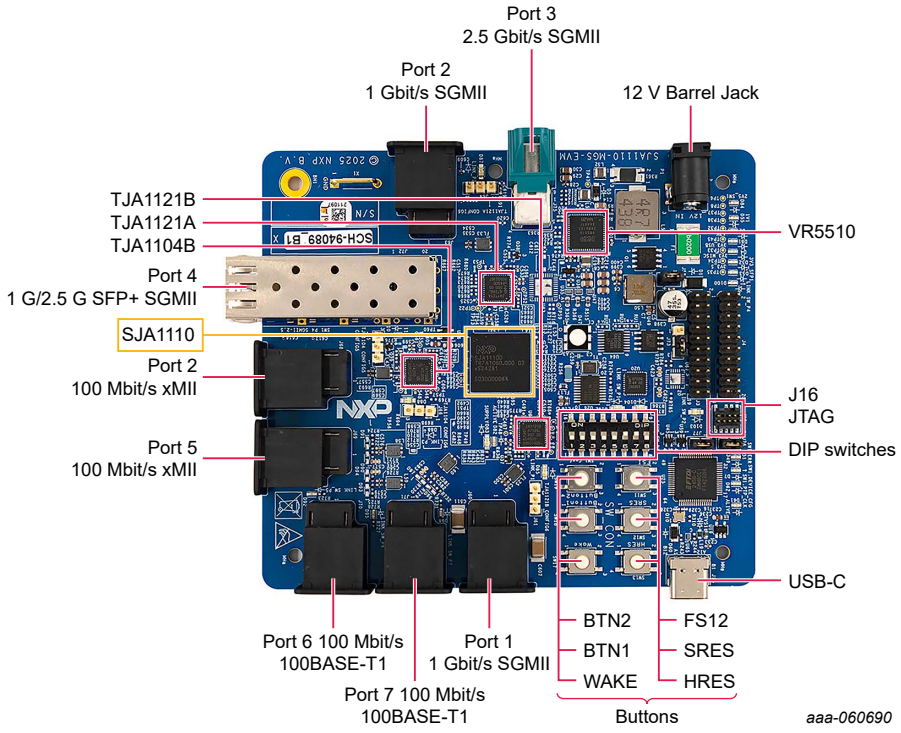

Figure 3. Main components and ports

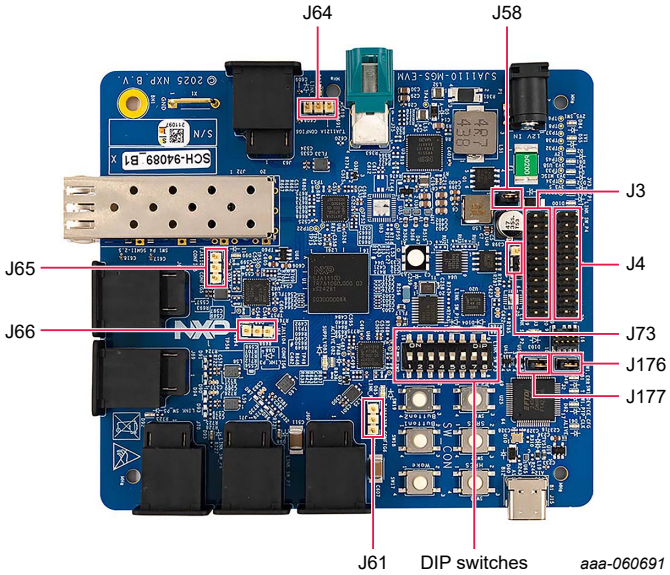

Figure 4. Jumpers and DIP switches

Table 1. Jumpers on SJA1110-MGS-EVM

Jumper	Function
J3	debug header (see Section 4.9)
J4	debug header (see Section 4.9)
J58	12 V power supply
J61	TJA1121B PHY role
J64	TJA1121A PHY role
J65	TJA1104B pin strap option
J66	TJA1104B pin strap option
J73	VDDA18_OTP_IN supply
J76	enable SOFT_RESET_N
J77	enable HARD_RESET_N

Table 2. SJA1110-MGS-EVM DIP switches

DIP switch	Signal	Comment
SW2.1	SW1_PHY_AUTO_MODE	Autonomous mode for internal PHYs 0 = autonomouse mode 1 = managed mode
SW2.2	SW1_PHY_AUTO_POL_DET	Polarity detection for internal PHYs 0 = polarity detection enabled 1 = polarity detection disabled
SW2.3	SW1_PHY_M_S5	Leader/follower settings for internal PHY on ports 5 to 7 0 = leader 1 = follower
SW2.4	SW1_PHY_M_S6	
SW2.5	SW1_PHY_M_S7	
SW2.6	SW1_BOOT_OPTION0	SJA1110 boot option selector
SW2.7	SW1_BOOT_OPTION1	SJA1110 boot option selector
SW2.8	n.c.	unused

Table 3. SJA1110 boot options

SW2.6	SW2.7	Boot mode
ON	ON	NVM
OFF	OFF	SDL

In NVM boot mode, the SJA1110 firmware boots from the external Flash memory on the board.

In SDL boot mode, the SJA1110 waits for a companion device to load the firmware via the SPI_HAP interface. SPI_HAP is a multiplexed SPI interface used to load firmware onto the device (SPI_HOST, via CS1) and for register-level access (SPI_AP, via CS0).

A number of LEDs are provided to indicate component, supply and port status. The LEDs are labelled in Figure 5 and detailed in Table 4 to Table 7. Some of the LED are hardware-controlled while others are controlled by the firmware running on the SJA1110.

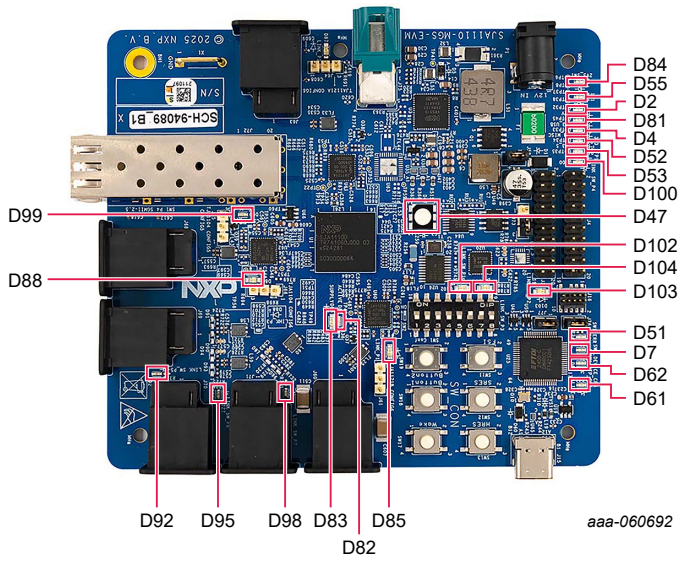

Figure 5. LEDs

Table 4. Voltage LEDs

LED	SW/HW controlled	Indicates when lit
D2	hardware	12 V supply present
D81	hardware	3.3 V USB supply present
D4	hardware	3.3 V LED supply present
D52	hardware	3.3 V supply for PHYs and SJA1110 present
D53	hardware	3.3 V supply for SFP+ cage supply present
D55	hardware	1.1 V supply for SJA1110
D54	hardware	2.2 V LDO output from SJA1110 present

Table 5. SJA1110 status LEDs

LED	SW/HW controlled	Indicates when lit
D7	hardware	SJA1110 holds a valid configuration
D61	software	indicates firmware running on SJA1110
D62	hardware	PTP clock output on SJA1110 on (PTP_CLK)
D51	hardware	fail-safe output on SJA1110 triggered (ERR_N)
D49	hardware	soft or hard reset generated
D47	software	multi-purpose RGB LED

Table 6. PHY status LEDs

LED	SW/HW controlled	Indicates when lit
D82	hardware	INH pin high

Table 6. PHY status LEDs*...continued*

LED	SW/HW controlled	Indicates when lit
D83	hardware	3.3 V supply present
D85	hardware	TJA1121B MDI link-up
D102	software	TJA1121B SGMII link-up
D87	hardware	TJA1121A MDI link-up
D103	software	TJA1121A RGMII link-up
D88	hardware	TJA1104B MDI link-up
D104	software	TJA1104B SGMII link-up
D92	software	SJA1110 port 5 link-up
D95	software	SJA1110 port 6 link-up
D98	software	SJA1110 port 7 link-up

Table 7. SPF+ cage LEDs

LED	SW/HW controlled	Indicates when lit
D100	software	SFP port link-up to SJA1110
D99	hardware	SFP present

4.5 PHYs

4.5.1 SMI addresses

Table 8 provides an overview of the SMI addresses of the onboard PHYs (internal and external). To prevent them being misconfigured, the SMI addresses can only be changed by soldering and not via DIP switches.

Table 8. PHY SMI addresses

Device	SMI address
TJA1121B	1
TJA1121A	2
TJA1104B	3
unused	4
Internal 100BASE-T1 P5	5
Internal 100BASE-T1 P6	6
Internal 100BASE-T1 P7	7

4.5.2 TJA1121B

The TJA1121B is configured automatically via pin strapping.

CONFIG6 pin strapping can be changed using the pin header. It controls the following miscellaneous settings:

- PHY role (follower or leader)
- Autonomous mode[1]

Pin strapping changes will only be applied after a reset has been completed. This can be triggered by pressing the HRES button or by a power-on reset.

Table 9. CONFIG6 settings

Pin header CONFIG6	Leader/follower	AUTONOMOUS mode
open	leader	enabled
HIGH	follower	enabled
LOW	disabled	disabled

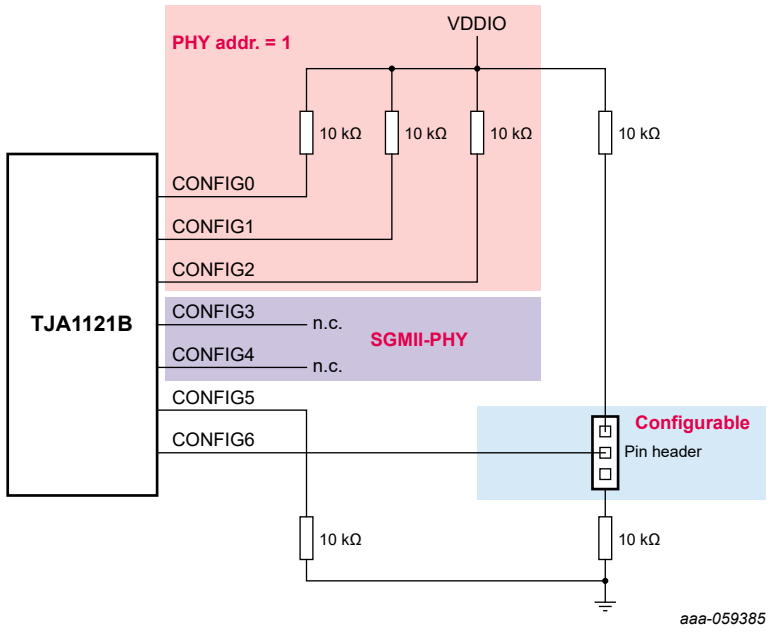

Figure 6. TJA1121B pin strapping

1 Unlike the TJA1104, polarity correction cannot be selected via pin strapping. The default configuration is 'enabled', which can be changed via register configuration.

4.5.3 TJA1121A

The TJA1121A is configured automatically via pin strapping.

CONFIG6 pin strapping can be changed using the pin header. It controls the following miscellaneous settings:

- PHY role (follower or leader)
- Autonomous mode[2]

Pin strapping changes will only be applied after a reset has been completed. This can be triggered by pressing the HRES button or by a power-on reset.

Table 10. CONFIG6 settings

Pin header CONFIG6	Leader/follower	AUTONOMOUS mode
open	leader	enabled
HIGH	follower	enabled
LOW	disabled	disabled

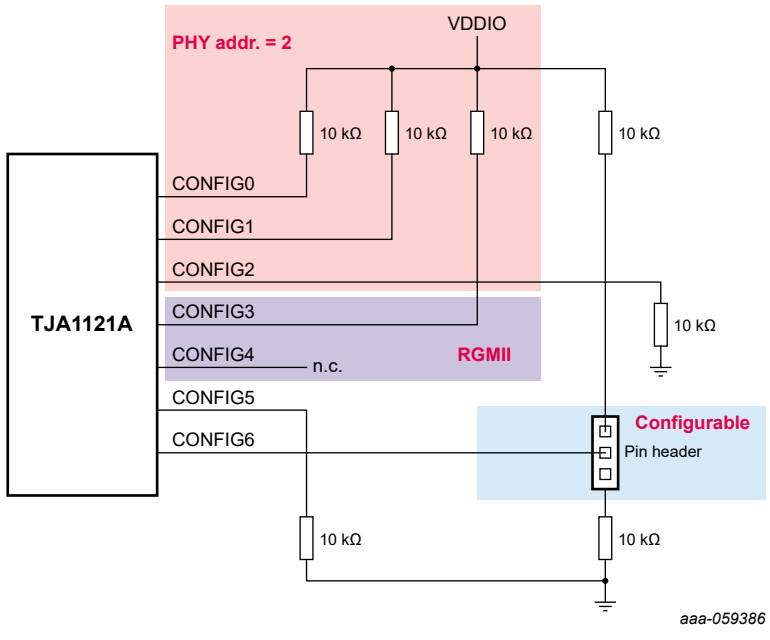

Figure 7. TJA1121A

2 Unlike the TJA1104, polarity correction cannot be selected via pin strapping. The default configuration is ‘enabled’, which can be changed via register configuration.

4.5.4 TJA1104B

The TJA1104B is configured automatically via pin strapping.

Pin headers for CONFIG5 and CONFIG6 can be used to change a number of pin strapping settings, as detailed in Table 11:

Table 11. CONFIG5/6 pin strapping settings

Leader/follower	Autonomous	Polarity correction	CONFIG5	CONFIG6
leader	enabled	enabled	O	O
leader	disabled	enabled	O	H
follower	enabled	enabled	O	L
follower	disabled	enabled	H	O
leader	enabled	disabled	H	H
leader	disabled	disabled	H	L
follower	enabled	disabled	L	O
follower	disabled	disabled	L	H
reserved	*reserved*	*reserved*	L	L

Pin strapping changes will only be applied after a reset has been completed. This can be triggered by pressing the HRES button or by a power-on reset.

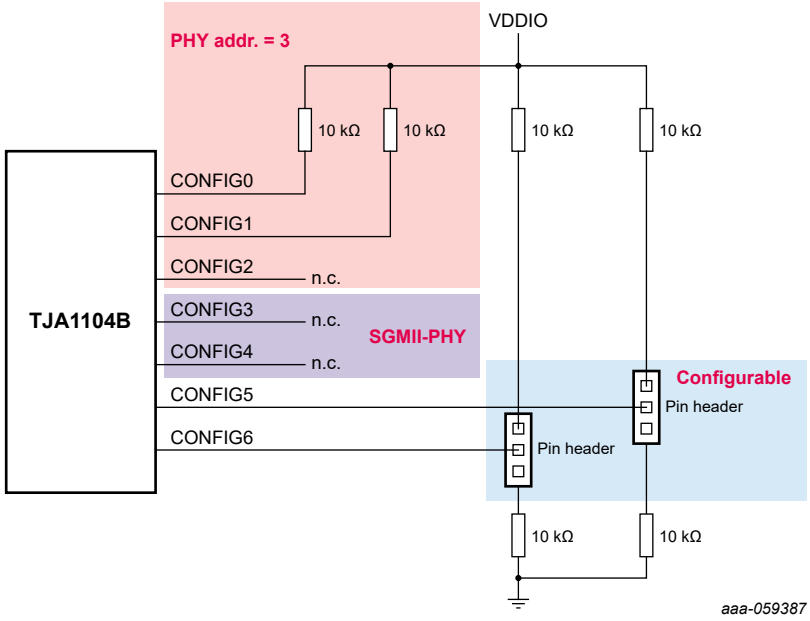

Figure 8. TJA1104B

4.6 Power supply

The power supply for the SJA1110-MGS-EVM is built around the VR5510 PMIC to exploit and demonstrate synergies with S32G projects.

The board is powered by a single 12 V input. It is advised to use an adapter that can deliver at least 1 A of current. The power connector is a barrel connector for standard DC plugs. It is connected to the PMIC via a jumper (J58).

The power supply topology of the SJA1110-MGS-EVM is shown in Figure 9.

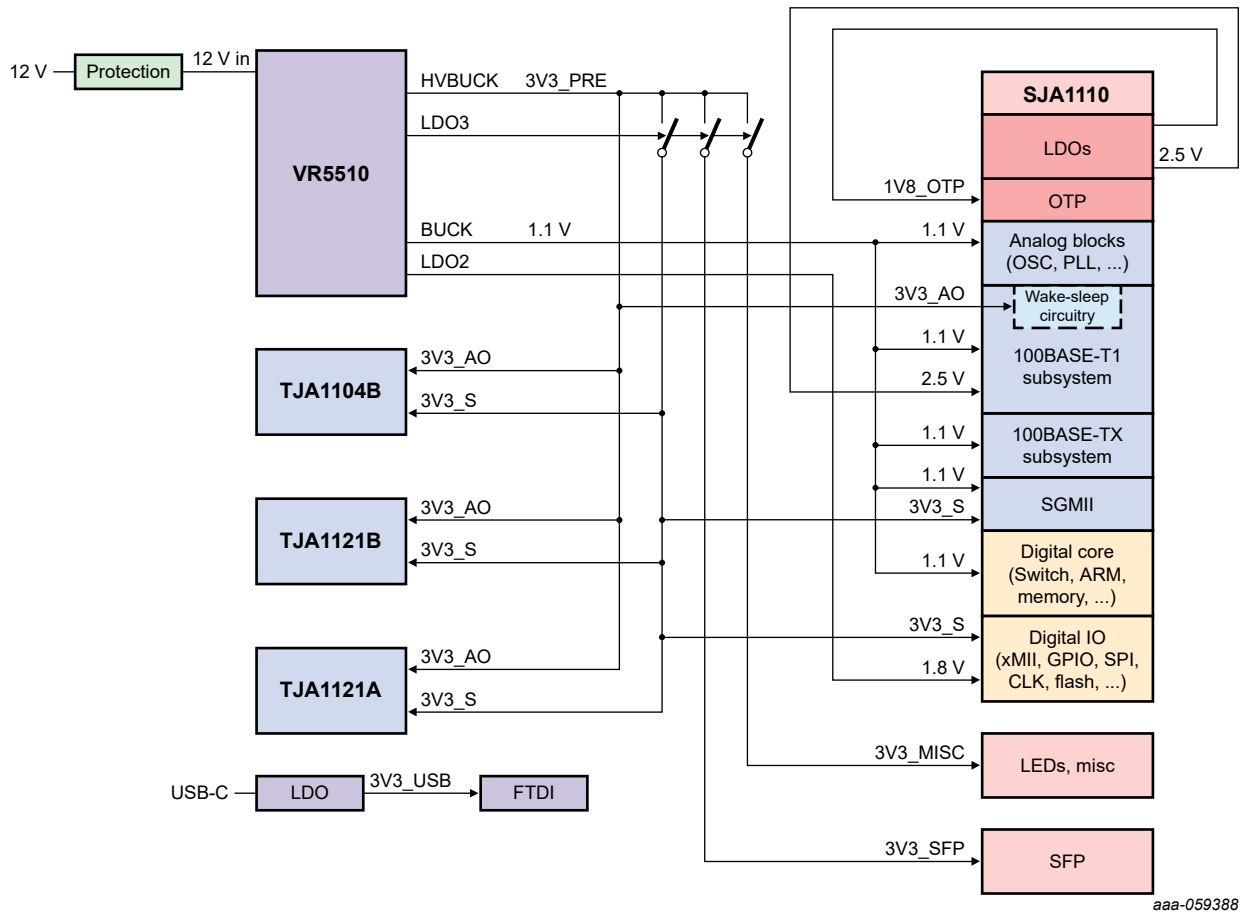

Figure 9. SJA1110-MGS-EVM power supply topology

The input protection includes polarity protection (serial schottky), a self-healing PTC and an EMC filter.

4.7 Interfaces

4.7.1 SMI

All external PHYs are connected to the SMI_OUT_MDIO and SMI_OUT_MDC pins on the SJA1110. Thus, the switch has register-level access to the external PHYs. This can be used for advanced configuration or to obtain status information (e.g. TC10, BIST, SQI, etc.). An overview of the SMI addresses can be found in Section 4.5.1.

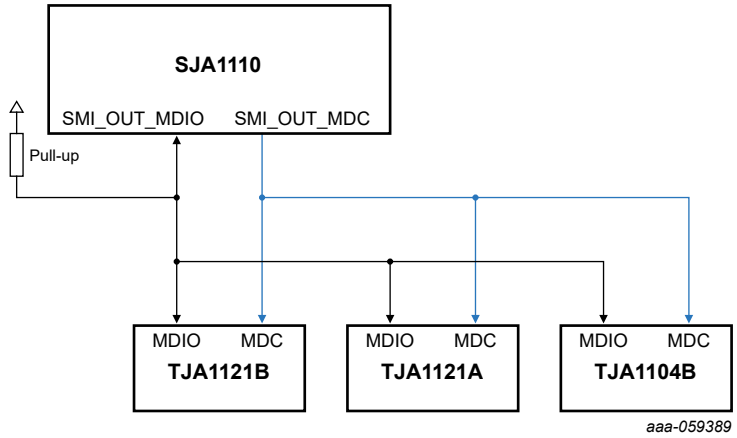

Figure 10. SMI interface

4.7.2 SPI

The SPI_PER interface on the SJA1110 is available on pin header J3, allowing another device to be connected to this interface. The SJA1110 be used as SPI leader to this device.

A typical use-case would be a cascaded switch architecture with two switches, in which one switch loads the configuration to the seconds switch via SPI.

4.8 GPIO extender

The PCAL9722 is a 22-bit general purpose I/O extender that provides remote I/O extension for many microcontroller families via the SPI interface. It is used to extend the 16 I/O pins on the SJA1110. Table 12 provides an overview of signals connected to the GPIO extender.

Table 12. GPIO pin extender

Port extender pin	Signal	Remark
P0_0	RESET_TJA1104B	-
P0_1	RESET_TJA1121A	-
P0_2	RESET_TJA1121B	-
P0_3	RESET_TJA1230	reserved for future use
P0_4	GPIO1_J4	connect to pin header J4
P0_5	GPIO2_J4	connect to pin header J4
P0_6	GPIO3_J4	connect to pin header J4
P0_7	GPIO4_J4	connect to pin header J4

Table 12. GPIO pin extender*...continued*

Port extender pin	Signal	Remark
P1_0	SW1_P1_LED	link LED switch xMII port 1
P1_1	SW1_P2_LED	link LED switch xMII port 2
P1_2	SW1_P3_LED	link LED switch xMII port 3
P1_3	SW1_P4_LED	link LED switch xMII port 4
P1_4	SW1_P5_LED	link LED switch port 5
P1_5	SW1_P6_LED	link LED switch port 6
P1_6	SW1_P7_LED	link LED switch port 7

4.9 Debug headers

Two debug headers (J3 and J4) are provided on the board to make the following signal groups available:

- I2C bus
- SMI interface (MDC, MDIO)
- SPI leader interface (SPI_PER)
- TC10 related signals (WAKE_IN_OUT, LOC_WAKE_IN, INH)
- 4 GPIOs from GPIO extender
- PTP related pins (DEVICE_SYNC, PTP_CLK)
- Switch status pins (ERR_N, DEVICE_CFG_N)
- Reset lines (SOFT_RESET_N, HARD_RESET_N)

J3 and J4 pinning is shown in Figure 11 and Figure 12.

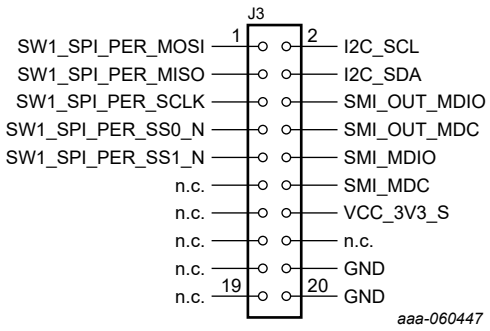

Figure 11. J3 pinning

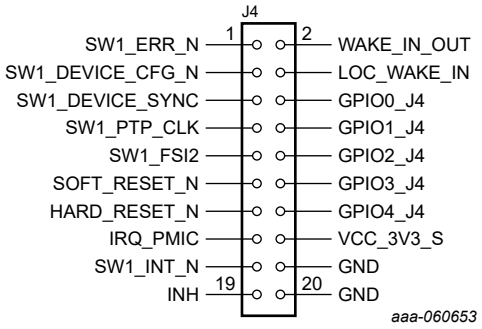

Figure 12. J4 pinning

5 Revision history

Table 13. Revision history

Document ID	Release date	Description
UM12269 v.1.0	28 April 2025	• Initial version

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