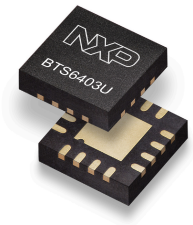

UM11862

BTS6403U evaluation board, quick starter guide

Rev. 1 — 18 November 2022 User manual

Document information

Information	Content
Keywords	BTS6403U, 5G Sub 6 GHz, pre-Driver, massive MIMO, evaluation board.
Abstract	This user manual describes the design considerations/choices for the product evaluation board (EVB) and gives an overview of the typical performance as measured on the EVB. The BTS6403U is a wideband, high linearity, pre-driver amplifier for 5G massive MIMO infrastructure applications. To enable easy evaluation of the product, the EVB is supplied with all necessary connectors.

Revision history

Rev	Date	Description
BTS6403U v.1	20221118	Initial version

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1 Introduction

This document describes the use, design, and test results of the BTS6403U.

1.1 BTS6403U product description

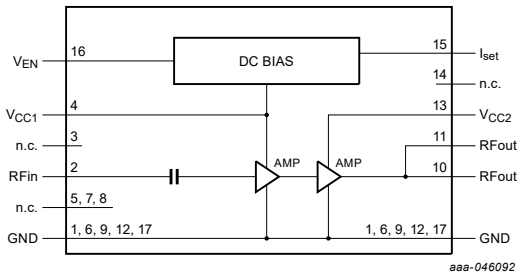
The BTS6403U is a wideband, high linearity, pre-driver amplifier for 5G massive MIMO infrastructure applications, with fast on-off switching to support TDD systems. The amplifier is designed to operate from 2.3 GHz to 4.2 GHz.

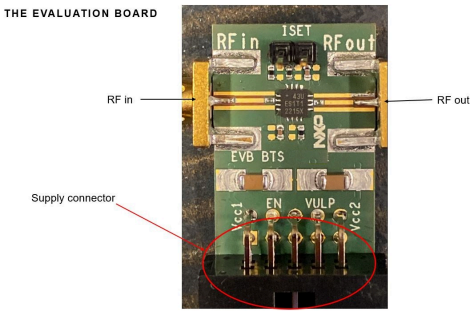
The BTS6403U is housed in a 3 mm x 3 mm x 0.85 mm 16-terminal HVQFN package.

The amplifier is ESD protected on all terminals.

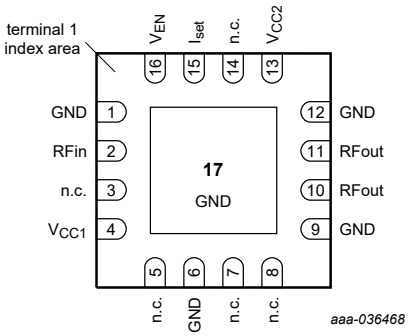
BTS6403U key features and benefits

- High saturated output power $P_{o(sat)}$ = 29.5 dBm
- High power-gain G_p = 38.5 dB
- High linearity performance ACLR = -45 dBc
- Unconditionally stable
- Fast switching to support TDD systems
- 5 V single supply, quiescent current 100 mA
- Small 16-terminal leadless package 3 mm x 3 mm x 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1





Note: *The EVB is shared with the BTS6201U, marking may be different.*



Transparent top view

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2 BTS6403U EVB properties

2.1 Schematic

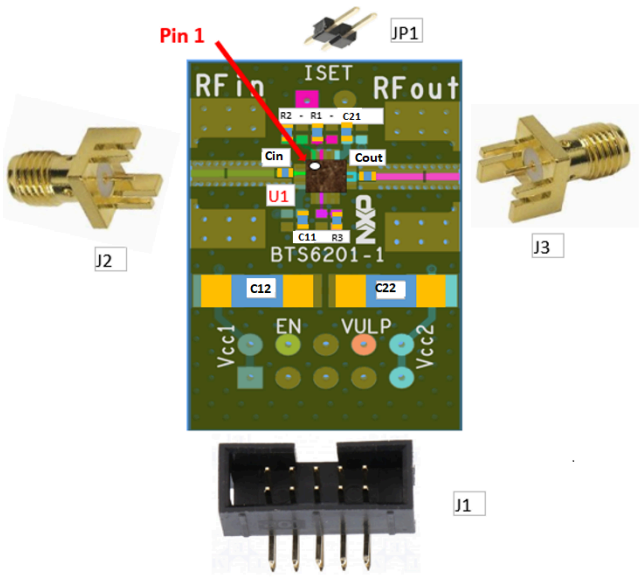

Figure 1. Location of the componenets

Note: *The EVB is shared with the BTS6201U, marking may be different.*

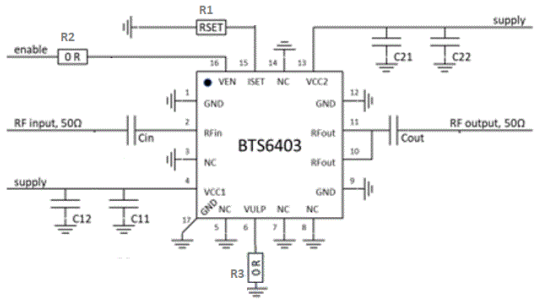

Figure 2. EVB schematic

Resistors, Coils, Capacitors						
ID	Shape	Value	Type	Manufacturer	Manufacturer Partnumber	Supplier/type
Cin	C0201	18 pF Tol:	COG	25V	GRM0335C1E180JD01D	MURATA
Cout	C0201	3.9 pF Tol:	COG	25V	GRM0335C1E3R9BD01D	MURATA
C21	C0402	10 nF Tol:	X7R	25V	GCM155R71E103KA37D	RNELL
C11	C0402	10 nF Tol:	X7R	25V	GCM155R71E103KA37D	FARNELL
C12	C1206	10 uF Tol:	X7R	10V	GRM31CR71A106KA01L	MURATA
C22	C1206	10 uF Tol:	X7R	10V	GRM31CR71A106KA01L	MURATA
R1	R0402	10 K Tol:	0	50V	WCR0402-10KFA	YAGEO
R2	R0402	0 R Tol:	0	0	RC0402JR-070RL	FARNELL
R3	R0402	0 R Tol:	0	0	RC0402JR-070RL	FARNELL
	-	-	-	-		-
	-	-	-	-		-
	-	-	-	-		-
	-	-	-	-		-
	-	-	-	-		-
	-	-	-	-		-

ID		Value		Manufacturer	Manufacturer Partnumber	Supplier/type
JP1				0	PIN HEADER Vertical - single row 3 2,5mm pitch	Texim-Europe
J2				JOHNSON EMERSON	CONNECTOR SMA CONN JACK END LAUNCH PC GOLD SMA-1,2mm	DIGI-KEY
J3				JOHNSON EMERSON	CONNECTOR SMA CONN JACK END LAUNCH PC GOLD SMA-1,2mm	DIGI-KEY
J1				Amphenol Socapex T821	PIN HEADER 10 Way, 2 Row, Right Angle, through hole	RS-online
EVB				0	PCB BTS6201X Tiger Shakti EVB (BTS6303)	Cibel

Figure 3. Bill of materials

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2.2 DC and control connections

Figure 4 shows the DC and enable connection, at the main header (J1). The connector can be straight or 90 degrees. The text is also on the EVB. Figure 5 shows connections JP1 GND, and JP1 ISET. JP1 (ISET) on the EVB can be applied to adjust the quiescent current in the final stage of the amplifier. R1 should be removed in case JP1 is applied to adjust the bias current.

Note: *NXP recommends that, using the setup as is shown in Figure 5 is R1 (10 kΩ).*

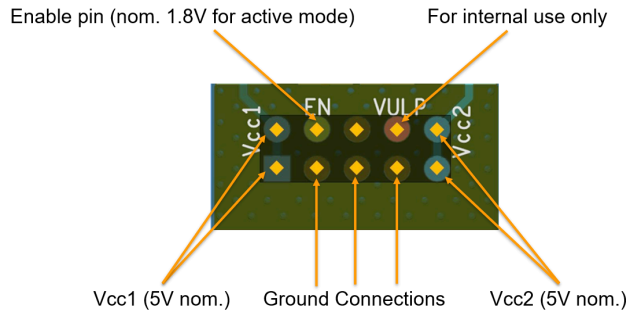

Figure 4. Main header J1

Note: *Connector may be straight or 90 degrees angled.*

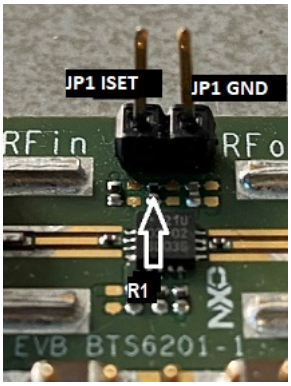

Figure 5. JP1

Figure 5

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2.3 Operations

Figure 6 shows the connections in a single ended to single ended operation.

If differential to single ended operation is also needed, NXP refers to UM11659 of the BTS6305U.

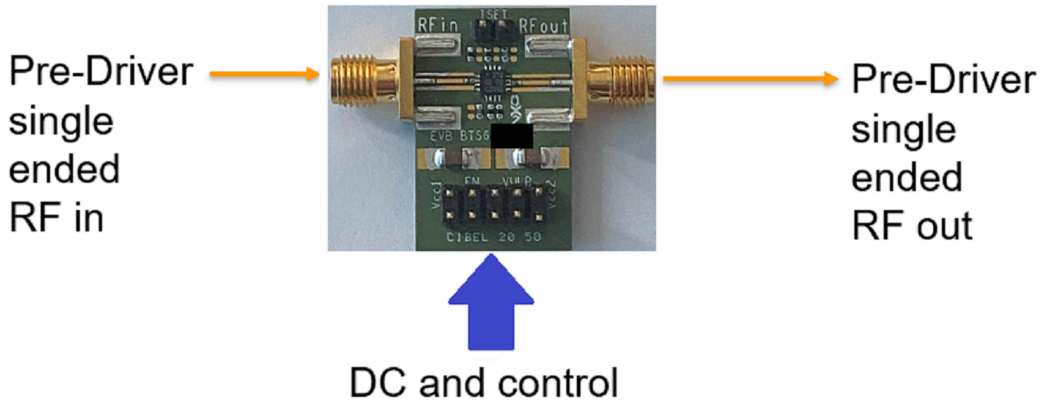

Figure 6. Single ended to single ended operation

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3 Measurements results

In the below graphics, the Spar measurements are shown. Measured at nominal conditions V_{CC} = 5 V, T_{case} = 25 °C, R_{set} = 10 KΩ.

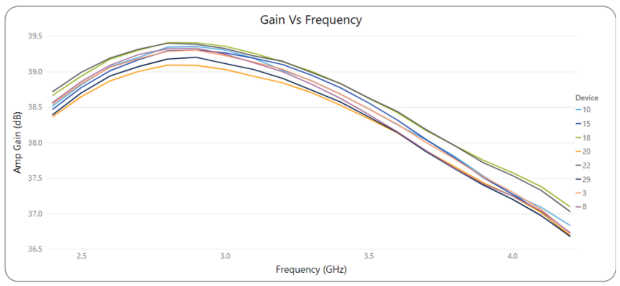

Figure 7. Gain at nominal conditions

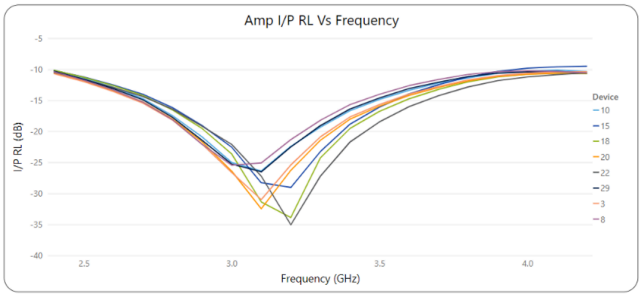

Figure 8. RL_i at nominal conditions

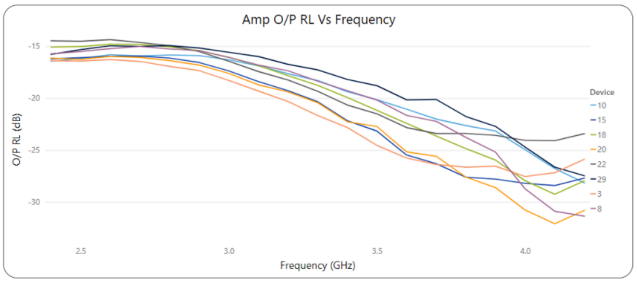

Figure 9. RL_o at nominal conditions

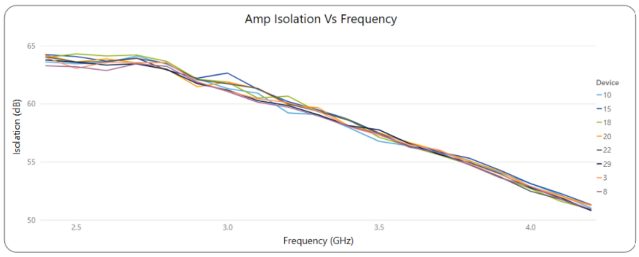

Figure 10. ISL_r (Gain mode) at nominal conditions

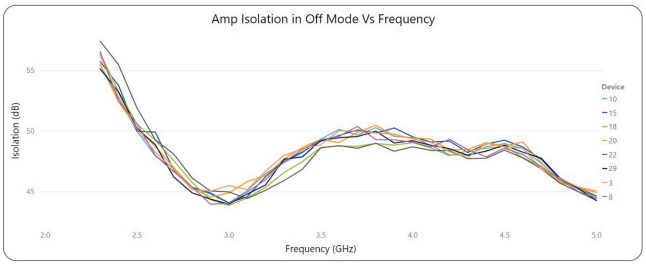

Figure 11. ISL_r (off mode) at nominal conditions

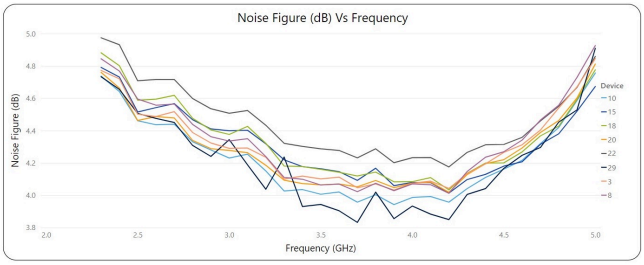

Figure 12. NF at nominal conditions

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4 Abbreviations

Table 1. Abbreviations

Acronym	Description
ACLR	adjacent channel leakage ratio
ESD	electrostatic discharge
EVB	evaluation board
MIMO	massive multiple-input multiple-output
RF	radio frequency
TDD	time-division duplexing

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