UM11494

FRDMGD31ECNEVM half-bridge evaluation board

Rev. 1 — 20 November 2020 User guide

Figure 1. FRDMGD31ECNEVM

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1 Introduction

This document is the user guide for the FRDMGD31ECNEVM half-bridge evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of GD3100. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The FRDMGD31ECNEVM is a half-bridge evaluation kit populated with two GD3100 single channel IGBT gate drive devices on a half-bridge evaluation board with pin configuration compatible with Econo IGBTs.

The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with SPIGen software for communication to the SPI registers on the GD3100 gate drive devices in either daisy chain or standalone configuration.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for FRDMGD31ECNEVM evaluation board is at http://www.nxp.com/FRDMGD31ECNEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the FRDMGD31ECNEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the FRDMGD31ECNEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- FRDM-KL25Z connected to translator board (3.3 V to 5.0 V)
- Cable, USB type A male/type mini B male 3 ft
- Quick start guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- IGBT or SiC MOSFET module in EconoDUAL™ package
- DC link capacitor compatible with IGBT or SiC MOSFET module

- 50 mil jumpers for configuration
- 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 25 V, 1.0 A DC power supply
- Pulse generator
- TEK MSO 4054 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R or CTW MiniHF30 (smaller diameter)
- Two isolated high voltage probes (CAL Test Electric CT2593-1, LeCroy AP030)
- Four low voltage probes
- Two digital voltmeters

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- Windows XP or higher operating system

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/FRDMGD31ECNEVM.

- SPI Generator (SPIGen) software, version 7.1.8 or later, a Graphical User Interface (GUI) http://www.nxp.com/SPIGEN

4 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

4.1 Kit overview

4.1.1 FRDMGD31ECNEVM features

- Capability to connect to SiC MOSFET or IGBT modules with an EconoDUAL™ footprint for half-bridge evaluations
- Daisy chain SPI communication capable
- Power supply and fail-safe jumper configurable
- Easy access power, ground and signal test points

4.1.2 Voltage domains, GD3100 pinout, logic header and IGBT pinout

Low voltage domain is 12 V VPWR domain that interfaces with the MCU and GD3100 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to IGBT single phase connections and test points.

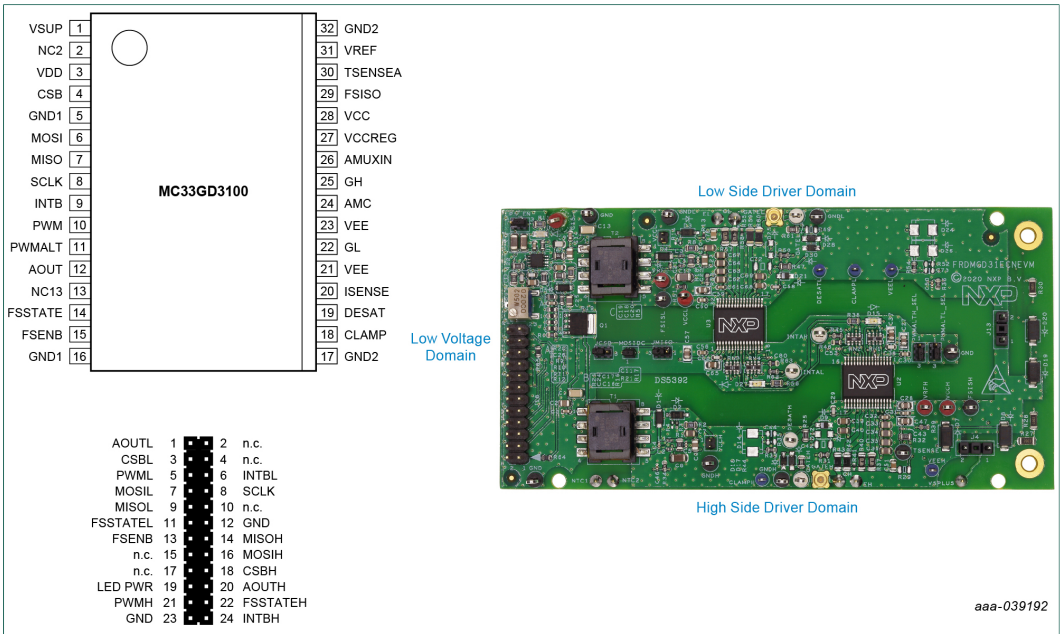


Figure 2. Evaluation board voltage and interface domains

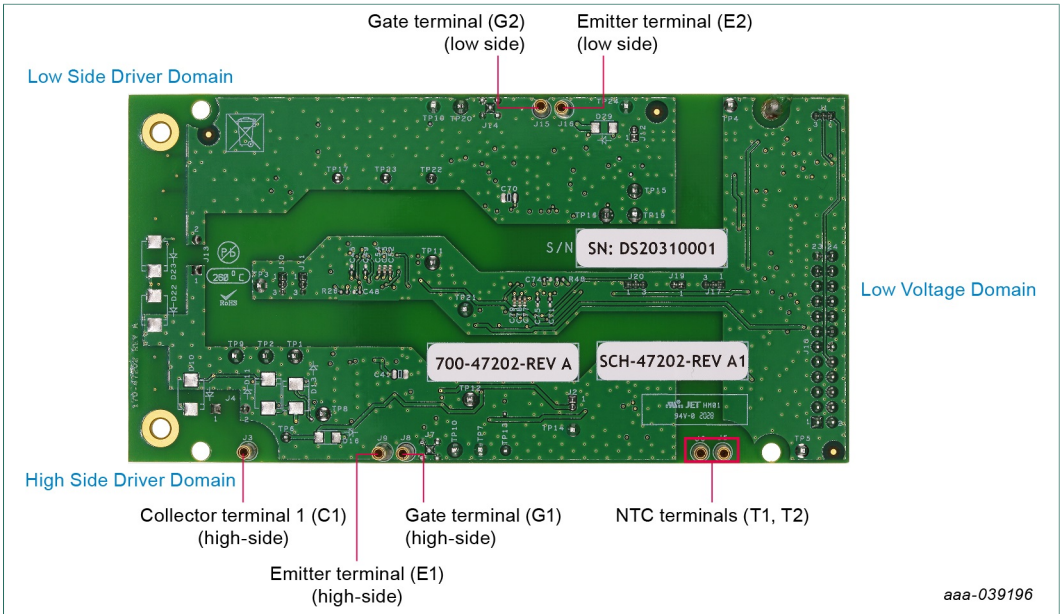


Figure 3. Bottom view

Table 1. Evaluation board voltage and interface domains

Pin	Name	Function
1	AOUTL	Duty cycle encoded signal (low-side)
2	VSUP	Power input (+12 V)
3	CSBL	Chip select bar (low-side)
4	VDD	5.0 V power

Pin	Name	Function
5	PWML	PWM input (low-side)
6	INTBL	Interrupt bar (low-side)
7	MOSIL	Master out slave in (low-side)
8	SCLK	Serial clock input
9	MISOL	Master in slave out (low-side)
11	FSSTATEL	Fail-safe state (low-side)
12	GND	Ground
13	FSENB	Fail-safe enable (high-side and low-side)
14	MISOH	Master in slave out
15	n.c.	not connected
16	MOSIH	Master out slave in
17	n.c.	not connected
18	CSBH	Chip select bar (high-side)
19	n.c.	not connected
20	AOUTH	Duty cycle encoded signal (high-side)
21	PWMH	PWM input (high-side)
22	FSSTATEH	Fail-safe state (high-side)
23	GND	Ground
24	INTBH	Interrupt bar (high-side)

4.2 Featured components

4.2.1 Advanced IGBT gate driver

4.2.1.1 General description

The GD3100 is an advanced single channel gate driver for IGBTs. Integrated Galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage and rail-to-rail gate voltage control.

Current and temperature sense minimizes IGBT stress during faults. Accurate and configurable under voltage lockout (UVLO) provides protection while ensuring sufficient gate drive voltage headroom.

The GD3100 autonomously manages severe faults and reports faults and status via INTB pin and a SPI interface. It is capable of directly driving gates of most IGBTs. Self test, control and protection functions are included for design of high reliability systems (ASIL C/D). It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

4.2.1.2 Features

- Compatible with current sense and temp sense IGBTs
- Fast short-circuit protection for IGBTs with current sense feedback
- Compliant with ASIL D ISO 26262 functional safety requirements
- SPI interface for safety monitoring, programmability and flexibility
- Integrated Galvanic signal isolation

- Integrated gate drive power stage capable of 15 A peak source and sink
- Interrupt pin for fast response to faults
- Compatible with negative gate supply
- Compatible with 200 V to 1700 V IGBTs, power range > 125 kW
- AEC-Q100 grade 1 qualified

4.2.2 Test points

All test points are clearly marked on the evaluation board. The following figure shows the location of various test points.

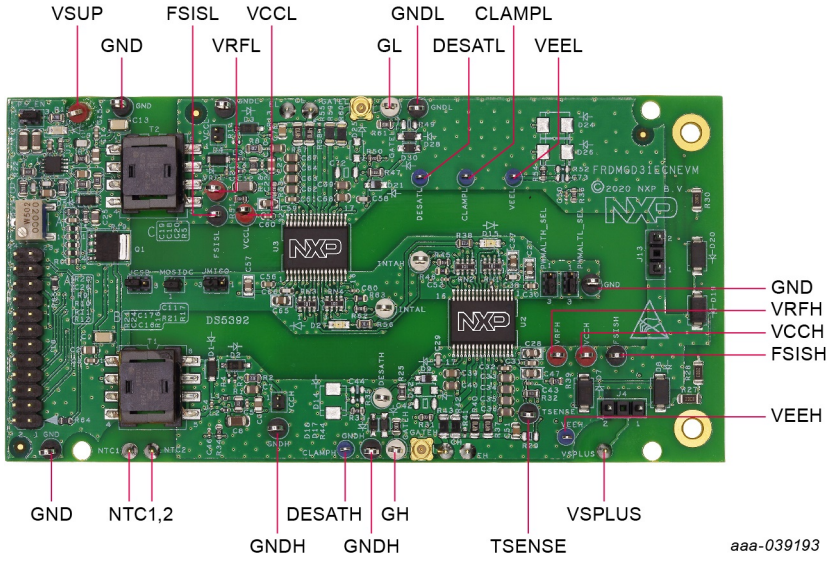


Figure 4. Evaluation board test points

Table 2. Evaluation board test point descriptions

Name	Definitions
Low voltage domain	
GND1, GND2, GND3	Grounding points for low voltage domain
VSUP	Primary power supply for low voltage domain compatible with 12 V automotive battery
Low-side driver domain	
VCCL	Positive voltage supply test point for isolated circuitry and low-side driver gate of IGBT
GNDL2, GNDL3	Low-side driver ground point
FSISL	LV domain FSISO pin test point that controls Fail-safe state
GL	IGBT gate test point on low-side driver domain which is the charging pin of IGBT gate
DESATL	V_{DS} desaturation test point connected to low-side driver DESAT pin and circuitry
VRFL	Internally regulated reference voltage test point for HV domain (5.0 V). For analog ADC and logic.
VEEL	Negative gate supply test point
High-side driver domain	

Name	Definitions
VCCH	Positive voltage supply test point for isolated circuitry and high-side driver gate of IGBT
GNDH2, GNDH3	High-side driver ground point
FSISH	HV domain FSISO pin test point that controls Fail-safe state
GH	IGBT gate test point on high-side driver domain which is the charging pin of IGBT gate
DESATH	V_{DS} desaturation test point connected to high-side driver DESAT pin and circuitry
VRFH	Internally regulated reference voltage test point for HV domain (5.0 V). For analog ADC and logic.
VEEH	Negative gate supply test point

4.2.3 Power supply and jumper configurations

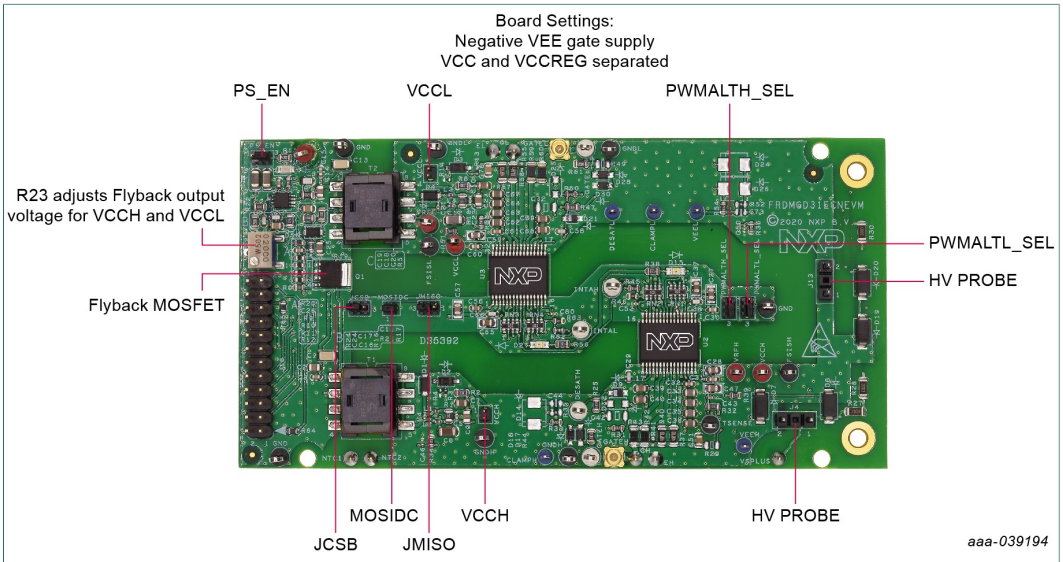


Figure 5. Evaluation board jumper locations

Table 3. Evaluation board jumper descriptions

Jumper	Position	Function
JCSB	1-2	SPI communicates to HS/LS GD3100 individually
	2-3	SPI in Daisy chain mode (shared CSB signal)
MOSIDC	OPEN	Daisy chain operation
	Shorted	Normal operation
JMISO	1-2	Daisy chain operation
	2-3	Normal operation
PWMALTL_SEL	1-2	Enables dead time fault protection
	2-3	Disables dead time fault protection (use for short-circuit testing)
PWMALTH_SEL	1-2	Enables dead time fault protection
	2-3	Disables dead time fault protection (use for short-circuit testing)

4.2.4 LED interrupt indicators

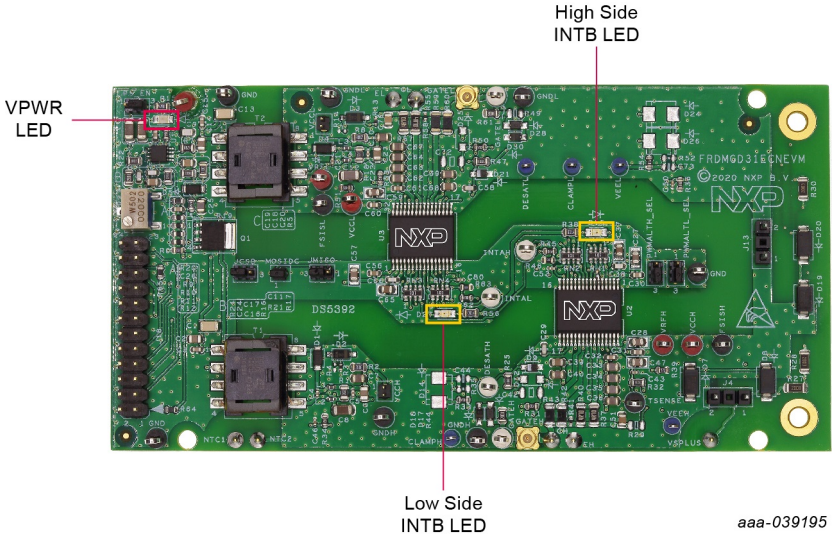


Figure 6. Evaluation board indicator locations

Table 4. Evaluation board indicator descriptions

LED	Description
Low-side INTB	Connected to the INTB output pin of low-side driver indicating reported fault status when On (active low)
High-side INTB	Connected to the INTB interrupt output pin of high-side driver indicating reported fault status when On (active low)

4.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the FRDMGD31ECNEVM evaluation board are available at http://www.nxp.com/FRDMGD31ECNEVM.

4.4 Kinetis KL25Z freedom board

The Freedom KL25Z is an ultra-low-cost development platform for Kinetis® L Series KL1x (KL14/15) and KL2x (KL24/25) MCUs built on Arm® Cortex®-M0+ processor.

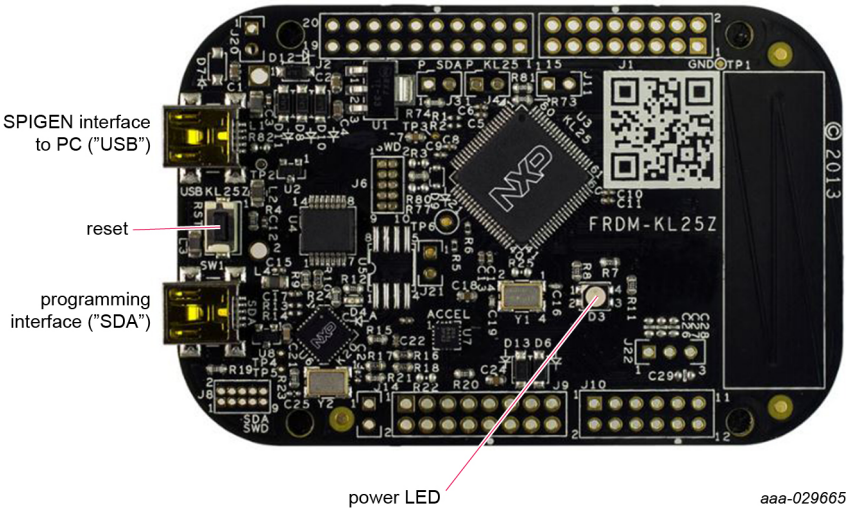


Figure 7. Freedom Development Platform

4.5 3.3 V to 5.0 V translator board

GD3100 translator enables level shifting of signals from 3.3 V to 5.0 V SPI communication.

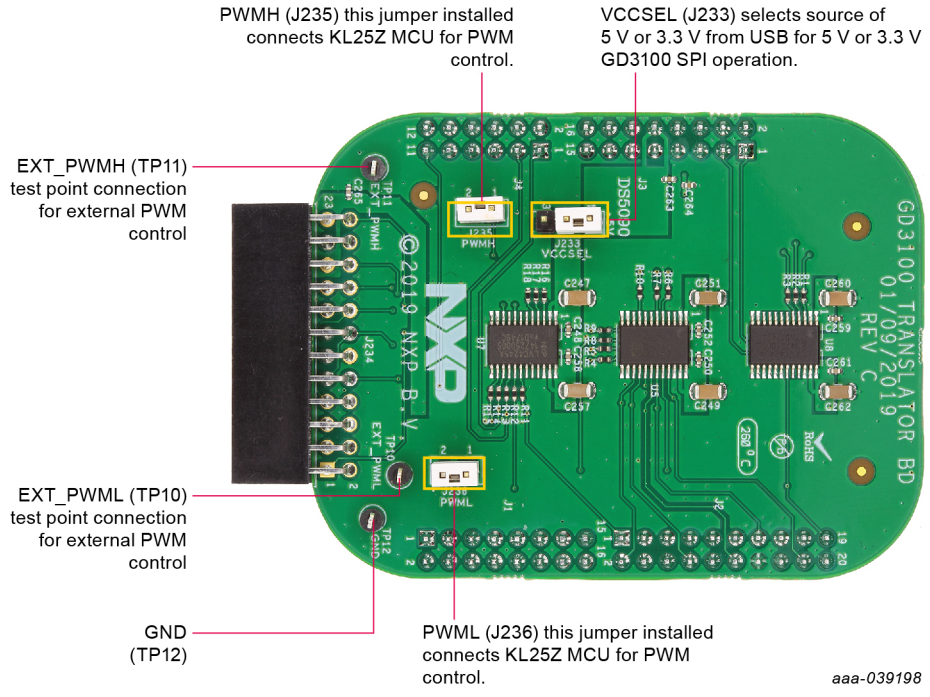


Figure 8. Translator board

5 Configuring the hardware for startup

Figure 9 presents a typical hardware configuration.

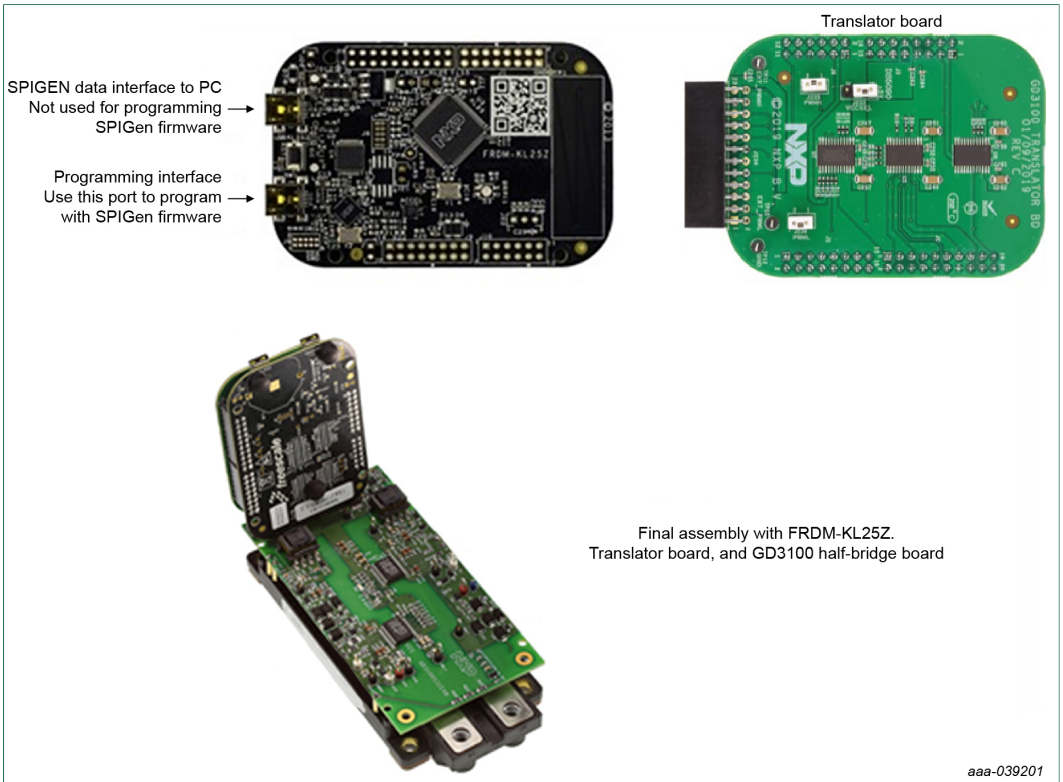


Figure 9. Typical configuration

To configure the hardware and workstation, complete the following procedure:

1. Connect FRDM-KL25Z and translator board with FRDMGD31ECNEVM half-bridge evaluation board (see Figure 9) by attaching to the 24-pin header in the correct orientation.
2. Attach the FRDMGD31ECNEVM to an IGBT module as desired with socket pins firmly on the module pin connections.
   Half-bridge board jumpers will be pre-installed from the factory and configured for SPI communication in a non-daisy chain SPI configuration. If SPI daisy chain communication is desired, see Section 4.2.3 "Power supply and jumper configurations".
3. Attach 12 V DC power supply to VPWR connection on half-bridge board and low voltage domain GND test point connection on half-bridge board.
   Note: Be sure to ground to low voltage domain for VPWR connection (see Figure 2).
4. Connect USB cable from USBKL25Z USB mini connection to Windows based PC USB port. KL25Z will be pre-installed with firmware from factory. Follow steps in Section 6 "Preparing graphical user interface operating environment" for downloading and installing SPIGEN SPI generator software from http://www.nxp.com.
5. With SPIGEN GUI installed and application running on Window based PC re-connect USB cable. A pop-up should appear indicating connection to the FRDM-KL25Z board.
6. Enable the 12 V DC power supply to the VPWR low voltage domain. The SPIGEN GUI, enables you to READ and WRITE registers on each GD3100 gate driver on either SPI0 (low-side) or SPI1 (high-side). Follow examples in Section 7.1 "Configuration register" for details.
7. Observe VCCL and VCCH voltage levels on the low-side and high-side high voltage domains respectively. These are set to provide the gate drive high levels from the fly-

back transformers and are isolated from the low voltage domain and from each other and have isolated grounds. VCCL (low-side) and VCCH (high-side) will be at ~17 V with VEE set to ~−3.3 V which will be the swing levels of the gate driver PWM signals.

8. With a DC link voltage supplied and an inductive load connected to the IGBT module, double pulse and short-circuit testing can be performed utilizing the SPIGEN pulse test functions in conjunction with the FRDMGD31ECNEVM half-bridge evaluation board. Use test points to observe desired signals.

Note: *For double pulse and short-circuit tests, ensure J235 and J236 are populated on translator board (see Figure 8). These jumpers need to be open if supplying PWM signal externally.*

6 Preparing graphical user interface operating environment

1. Install the firmware and MCU code.
   - The kit ships with KL25Z MCU firmware already installed. If for any reason the KL25Z MCU firmware needs to be re-installed follow this procedure. Hold down the reset button on the KL25Z board and connect a mini USB B cable from the PC to the Programming interface SDA USB port. Release the reset button. The PC shows a drive called **E:/BOOTLOADER** or something similar. Copy the SDA file (*MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA*) to the **E:/BOOTLOADER** drive.
   - Unplug and re-plug the USB cable to the same location to restart and activate the new firmware (do not hold the reset button this time). The drive name changes to **E:/FRDM-KL25Z** or something similar. Copy the file *UsbSpiDongleKL25Z_GD3100_545.srec* to the **E:/FRDM-KL25Z** drive. Unplug USB cable. Firmware files are available with SPIGEN install which can be downloaded from NXP.com and can be found in SPIGEN install directory folder.
2. Run *SPIGEN SPI generator software installer* to install SPIGEN on PC.
3. Run SPIGEN with KL25Z board connected.
   - Connect the PC to the mini USB B cable into the “USBKL25Z” USB port on the KL25Z board.
   - Open the SPIGen software on the PC. At the bottom of the page you should see *SPI dongle Firmware Ver. 5.4.7 or later.*

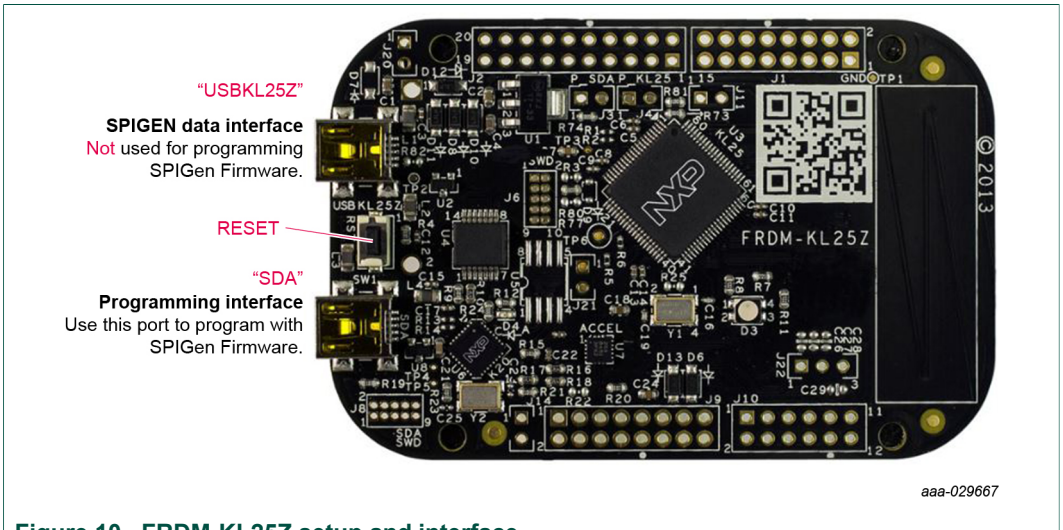
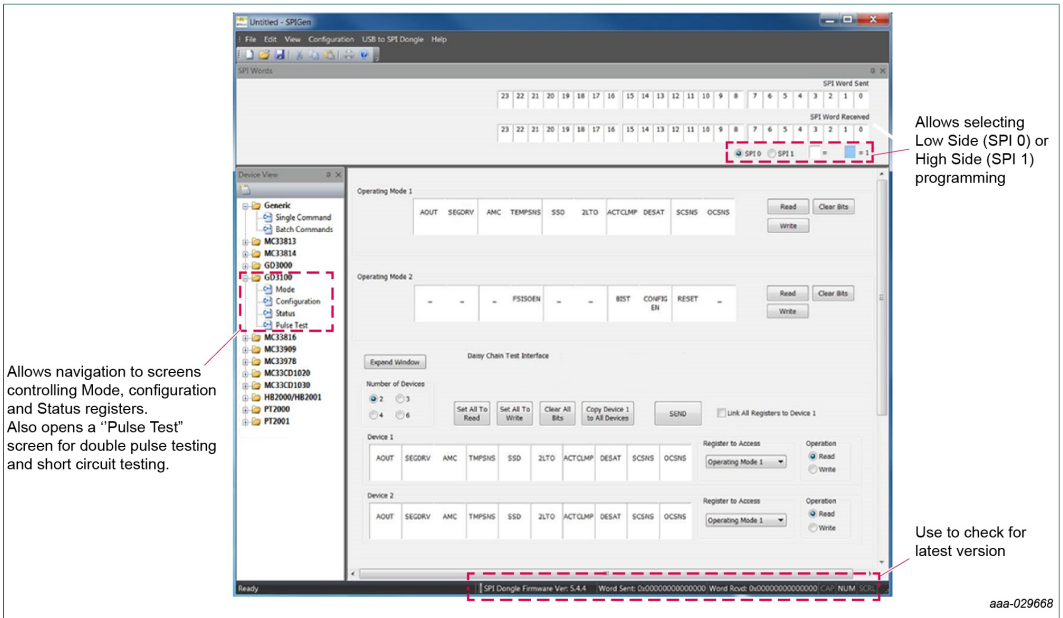


Figure 10. FRDM-KL25Z setup and interface

7 Using SPIGEN GUI

See Figure 11 for SPIGEN Graphical User Interface for GD3100 internal register read and write access. It also includes the daisy chain read and write access when configured for daisy chain operation on certain GD3100 registers.



1. **Device View**
2. **Command View**
3. **SPI Words**

Figure 11. SPIGEN GUI

1. **Device View**: The **Device View** contains folders for SPIGen-supported devices. Each device folder contains device-specific functions and commands.
2. **Command View**: The **Command View** provides the interaction interface to the selected functions or commands, as selected in the **Device View**.
3. **SPI Words**: The **SPI Words** section displays the latest SPI word sent and latest SPI word received. The SPI words are displayed in RAW format (32-bit).

7.1 Configuration register

See GD3100 data sheet for SPI configuration register descriptions.

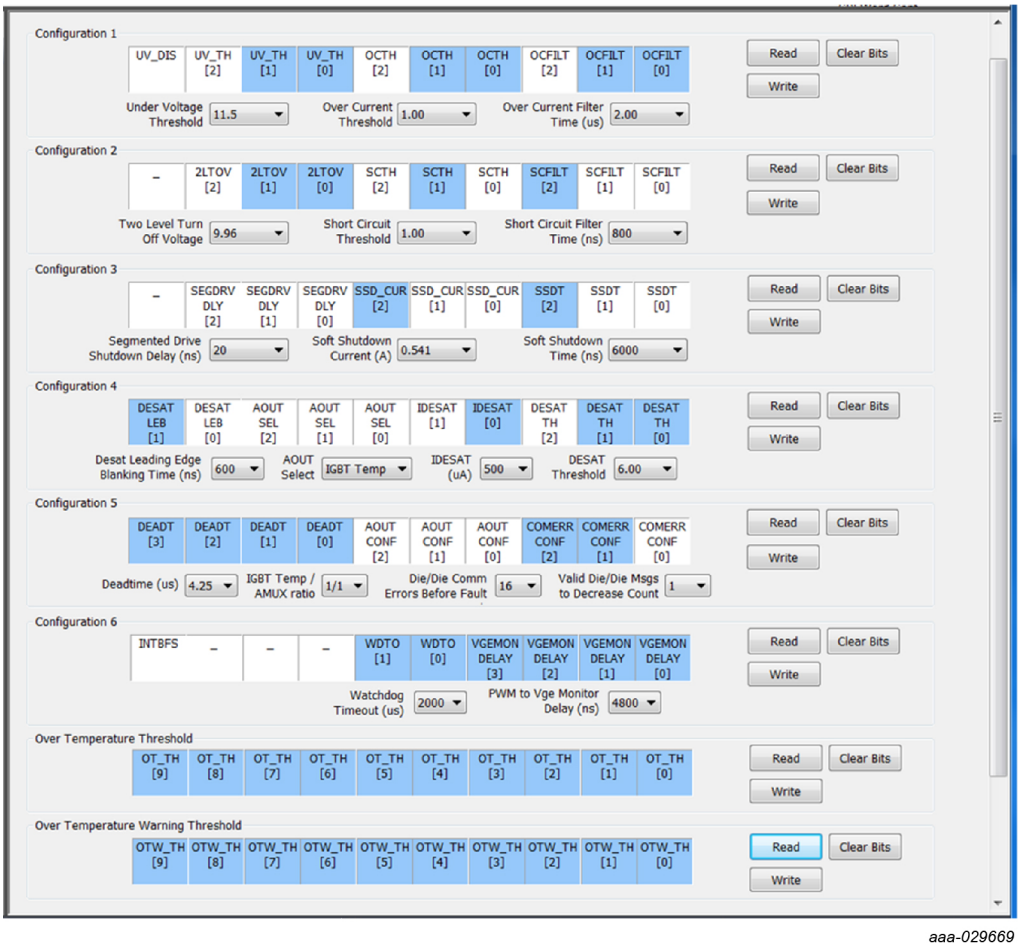


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Figure 12. Configuration register window

7.2 Status and mask register

See GD3100 data sheet for SPI configuration register descriptions.

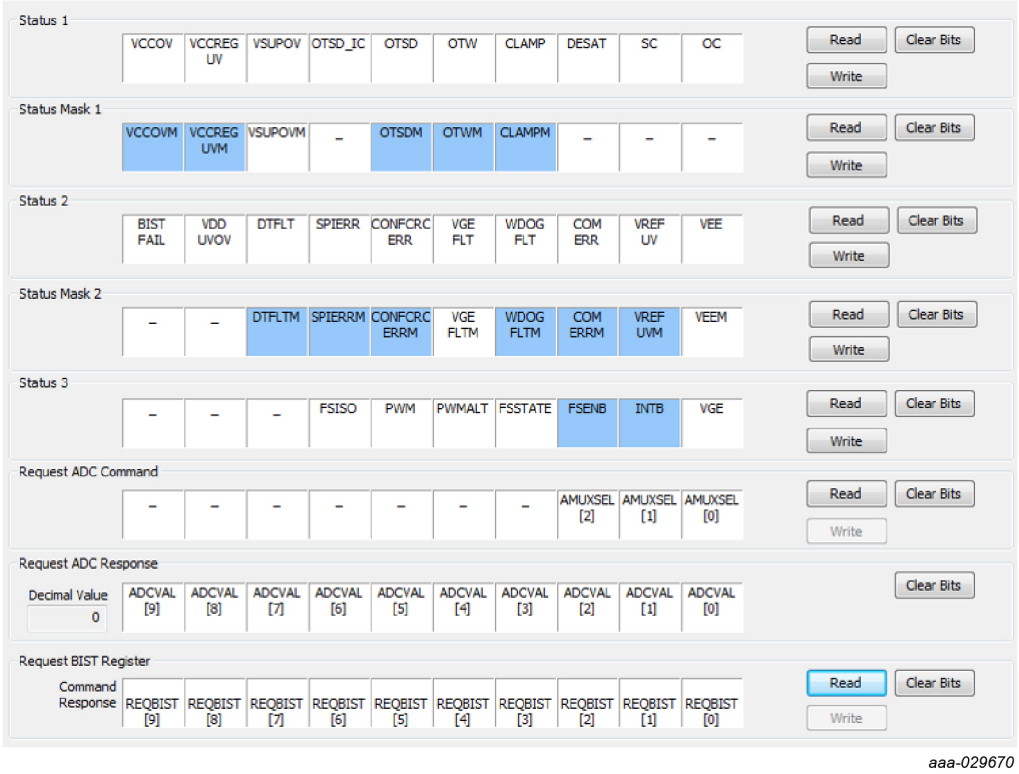

Figure 13. Status and mask register window

8 References

[1] **FRDMGD31ECNEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/FRDMGD31ECNEVM

[2] **GD3100** — product information on Advanced single-channel gate driver for Insulated Gate Bipolar Transistors (IGBTs)
http://www.nxp.com/GD3100

9 Revision history

Revision history

Rev	Date	Description
v.1	20201120	Initial version

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