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NTAG I²C *plus* Explorer Kit Peek and Poke

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User manual
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Document information

Info	Content
Keywords	NTAG I²C *plus*, Explorer Kit, PC, NFC Tag, Peek and Poke
Abstract	This User Manual aims at describing the functionalities and how to use the Peek and Poke GUI together with the NTAG I²C *plus* Explorer Kit.

Revision history

Rev	Date	Description
2.1	20170925	Updated documentation with new features included in version 3.0 of Peek and Poke
2.0	20170315	Completely revised version
1.0	20151215	First version.

Contact information

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1. Object

Fig 1. NTAG I²C *plus* – First Officially Certified NFC Forum Type 2 Tag with I²C Interface

NTAG I²C *plus* Explorer kit is the first officially certified NFC Forum Type 2 Tag with I²C interface. It is an all-in-one demonstration and development resource to demonstrate the unique properties of the NTAG I²C *plus* tag chip. By including a full complement of hardware and software tools, users can not only investigate the capabilities of the chip through the various demonstrations, but also develop and test their own applications.

This User Manual explains how to use the Peek and Poke application for the new product of the NTAG family: NTAG I²C *plus*, which adds new features like password protection and originality signature.

Technical aspects related to the IC functioning (i.e. the configuration registers) are beyond the scope of this document. In order to get further technical details, please consult the dedicated Datasheet “NTAG I²C *plus*, NFC Forum Type 2 Tag compliant IC with I²C interface”.

2. NTAG I²C *plus* introduction

The NTAG I²C *plus* is offering both contactless and contact interfaces. In addition to the passive NFC Forum compliant RF interface, the NTAG I²C *plus* product provides an I²C

interface that allows the IC to communicate with the microcontroller when the chip is powered by an external device, i.e. a mobile phone.

NTAG I²C *plus* operating in energy harvesting mode provides the possibility to supply external low power devices (e.g. microcontrollers) with the energy generated from the RF field of the external NFC device.

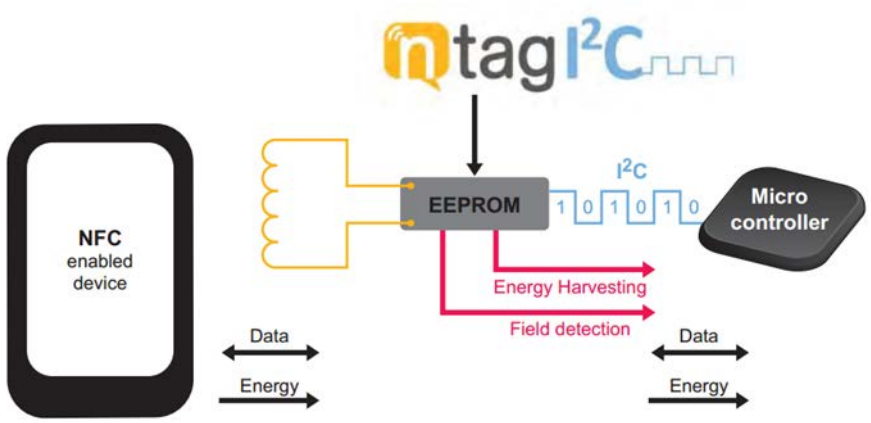

Fig 2. NTAG I²C *plus*

The NTAG I²C *plus* product has two types of memories:

1. EEPROM memory compliant with the NFC Forum Type 2 Tag implementation.
2. 64-byte SRAM memory, which is mapped with the EEPROM memory and is externally powered.

The NTAG I²C *plus* features a Pass-Through mode that allows fast download and upload of data from the RF interface to the I²C interface and vice versa. This functionality makes use of the SRAM memory that allows fast data transfer between interfaces without the EEPROM performance limitations.

In addition to the I²C interface functionality, the NTAG I²C *plus* product features an Event Detection Pin for waking up the host-connected devices or synchronizing the data transfer between the two interfaces.

The new NTAG I²C *plus* improves the last NTAG I²C version with some features such as FAST_WRITE command and memory protection. The configuration of this memory protection field is explained in more detail in subsequent sections.

3. NTAG I²C *plus* Explorer kit contents

The NTAG I²C *plus* Explorer kit (NEK) consists of hardware and software tools that developers can use to understand the NXP NTAG I²C *plus* tag chip functionality and demonstrate its potential for other applications.

3.1 Hardware components

3.1.1 NTAG I²C *plus* Explorer board

A hardware board based on the NXP LPC 11U24 32-bit ARM Cortex-M0 microcontroller, with on-board LCD display, NXP LM75B temperature sensor, voltage monitors, I²C serial bus connector, JTAG/SWD debug connector, RGB LED, micro USB connector and five push button controls.

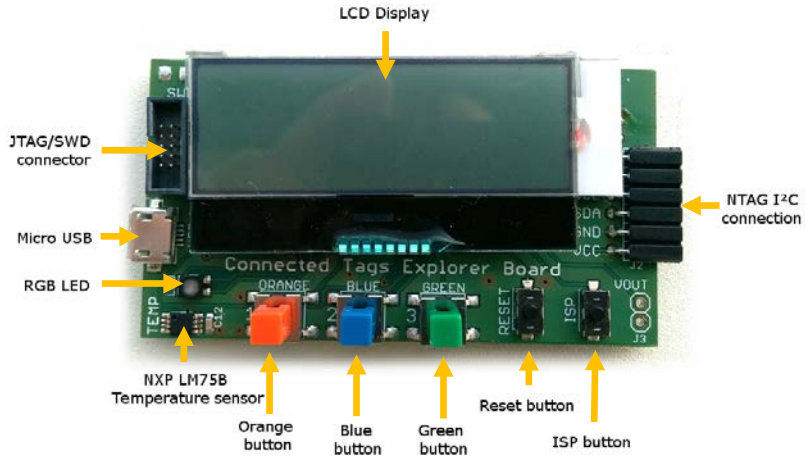

Fig 3. NTAG I²C *plus* Explorer Board

3.1.2 Antenna board

The antenna board carries the NTAG I²C *plus* 2k version itself and provides two interfaces:

I. The RF interface to an NFC reader

II. The I²C interface to the NTAG I²C *plus* Explorer board

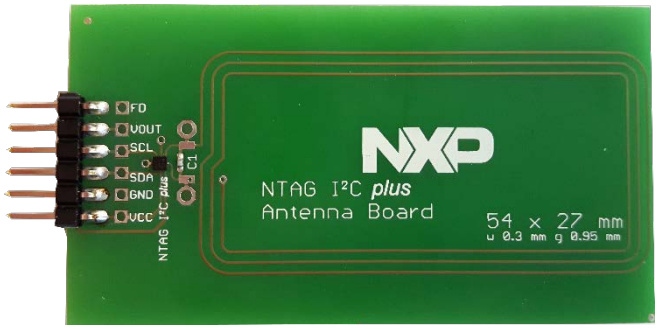

Fig 4. Antenna Board

3.2 Peek and Poke GUI

The Peek and Poke GUI is a Windows application that can be used to examine the detailed memory contents of the NTAG I²C *plus* EEPROM via I²C interface. This software component is available as a download from the public NXP website.

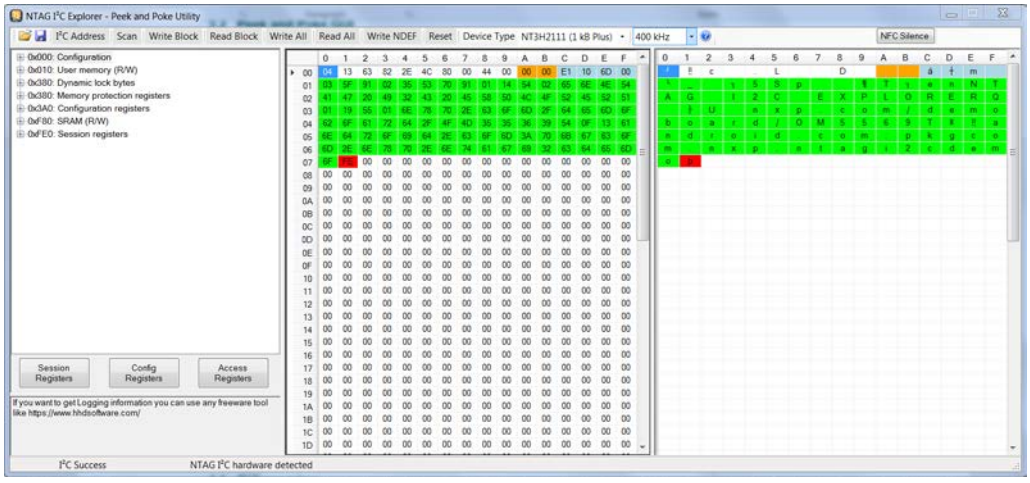

Fig 5. Peek and Poke GUI

4. NTAG I²C *plus* Peek and Poke GUI

The Peek and Poke application is a PC-based NTAG I²C and NTAG I²C *plus* exploration software tool with a graphical user interface. This software allows users to read from and write to the memory in the NTAG I²C *plus* chip via the I²C serial bus interface, as well as control the Session and Configuration registers.

Before working with the Peek and Poke GUI make sure your NTAG I²C Explorer Board is connected to your PC via USB.

4.1 GUI overview

Upon the start-up, the GUI overview is shown in Fig 6. Each region of the GUI is labeled for an easier reference. Each of these parts are the following:

1. The top bar contains most of the GUI controls.
2. The left column lists the NTAG I²C *plus* memory locations for each region indicated with the hexadecimal address.
3. The center grid displays the contents of those addresses in hexadecimal format.
4. The right column displays the ASCII representation of the data listed in the center column.

5. The bar at the bottom of the GUI indicates presence or absence of any connected NTAG I²C *plus* hardware and the status of the operations.

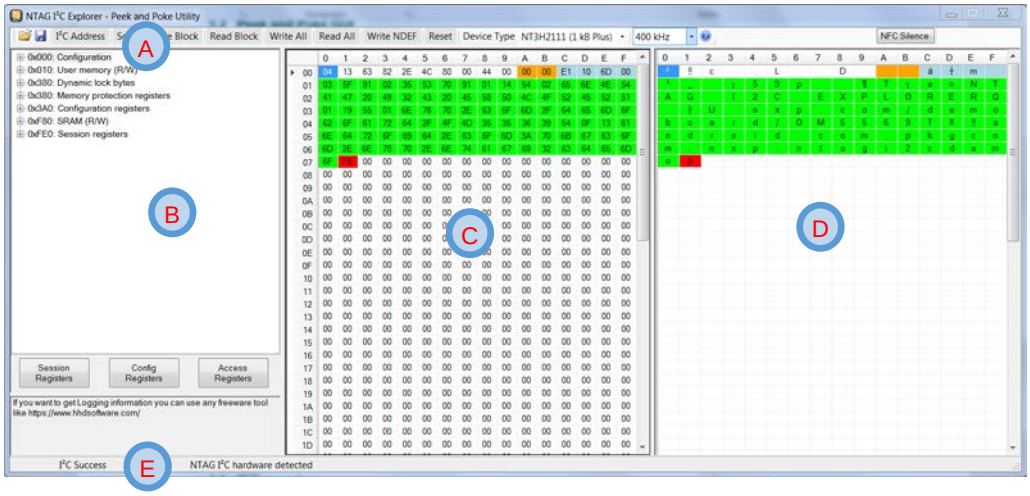

Fig 6. Peek and Poke GUI Overview

4.2 GUI top control bar details

This section details each of the controls of the navigation bar on the top. See it depicted in Fig 7. The actions offered on this bar are: exporting and importing memory contents from or to a file, read and write to the memory, reset the memory to a default value, select the type of the device connected, scan for connected devices, setting of the device address and the selection of the speed of the bus for the communication. In addition, there is an information button about the application.

Version 3.0 of Peek and Poke includes 'NFC Silence' button, which implements NFC Silence feature for NTAG I²C *plus*. This button is described in more detail in a subsequent section.

Fig 7. Peek and Poke Navigation Bar

4.2.1 Export / import memory contents

At the beginning of the navigation bar there are two icons to export and import the memory contents. They are shown in Fig 8, highlighted in red. The first folder icon is to open an HEX file containing a memory data and import it. The second icon, a disk, allows the user to export the data of the tables it into an HEX file.

Fig 8. Peek and Poke import and export memory contents controls

4.2.2 Read and write controls

Read and write control buttons can be found at the top of the initial screen. Fig 9 shows the controls.

- *Write Block* button: Writes 16 bytes of data from the selected grid block into the tag.
- *Read Block* button: Reads 16 bytes of data and displays the contents on the grid.
- *Write All* button: Writes the entire EEPROM memory with the data on the grid into the tag.
- *Read All* button: Reads the entire EEPROM memory and displays it on the grid.

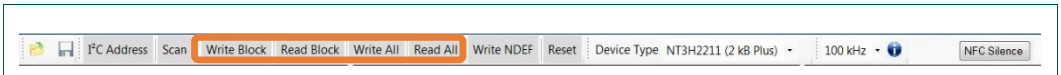

Fig 9. Peek and Poke Read and Write controls

4.2.3 Write NDEF message

The control *Write NDEF* opens a form with the option to enter a text and write it as an NDEF message or to write a default NDEF message. Fig 10 shows the control.

The default NDEF message is an NDEF SmartPoster composed of a Text message and a URI record (Text record: NTAG I2C Explorer, an AAR: android.com:pkgcom.nxp.ntagi2cdemo_dev, and URI record: www.nxp.com/demoboard/OM5569).

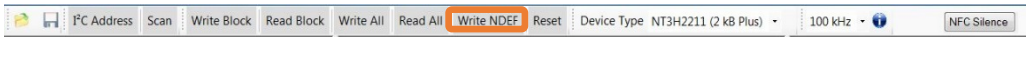

Fig 10. Peek and Poke Write NDEF message control

Fig 11 shows the form with the two options to write a message and the tables with the message written and highlighted.

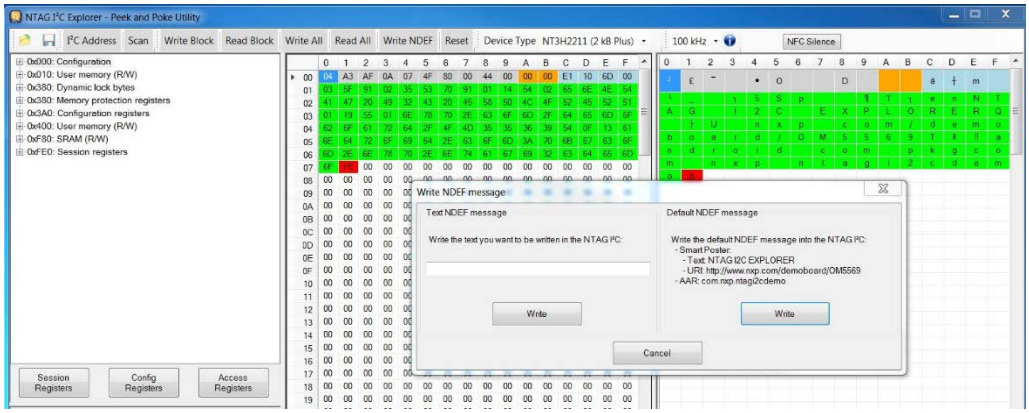

Fig 11. Peek and Poke Write NDEF form and tables showing the message

4.2.4 Reset tag memory

The reset button sets the NTAG I²C tag memory to the default value and displays it in the grid. The default tag memory value corresponds to a default NDEF message on the user memory (see structure in 4.2.3), and the default session and configuration register settings as defined in the NTAG I²C product datasheet. Fig 12 shows the control.

Fig 12. Peek and Poke Reset tag control

4.2.5 Device selection

The device selection allows us to change the device type. There are four possibilities here: the **NT3H1101** or **NT3H1201** (NTAG I²C, 1K and 2K) for the old NTAG I²C and **NT3H2111** or **NT3H2211** (NTAG I²C *plus* 1K and 2K) for NTAG I²C *plus*. The first and third options refer to the devices that have up to 1 kB of memory size, and the second and fourth ones refer to the 2 kB memory size. This is important because it will show a different grid depending on the memory size. Fig 13 shows the control.

In version 3.0, auto detection of tag is implemented. When the application detects that a new tag has been connected via USB, it automatically changes the device type and shows the corresponding memory map.

Fig 13. Peek and Poke Device selection

4.2.6 I²C device address and scanning

It is possible to change the I²C address of the NTAG I²C *plus* IC. Fig 14 shows the control. To change the default I²C address, a new value is needed in the text box. After click on the I²C Address button; once the button is clicked a new window will be prompted. This window will show the current I²C Address and a Textbox to insert the new Address. When the new address is written, it is necessary to click on 'OK' and then the new I²C address value is automatically written in the device. The default I²C serial bus address of the NTAG I²C tag chips is 0x55. I²C address is 7-bit. LSB bit designates the I²C Action – Read or Write to that address. While updating the 7 bit I²C address to block 0 byte 0 we have to left shift it by 1 bit and then write in Peek and Poke text box. For example, if we want an I²C address for NTAG to be 0x55h, value of 0xAAh which is (0x55 << 1) to the block 0 byte 0 needs to be written.

The Scan button will scan the entire range of possible addresses until it finds the device I²C address.

Fig 14. Peek and Poke Address and scanning

4.2.7 I²C clock frequency

The I²C serial bus clock frequency can be changed by selecting a data rate from the drop-down. The maximum data rate supported by the tag is 400 KHz. Fig 15 shows the control.

Fig 15. Peek and Poke I²C Clock frequency control

4.2.8 NFC Silence

When 'NFC Silence' button is active, the NFC silence feature is activated in the session registers of the NTAG I²C *plus*. This means that while the button is enabled it won't be possible to communicate with the tag via NFC. As it is only changed in the session registry, once the device is powered off the value will be reset.

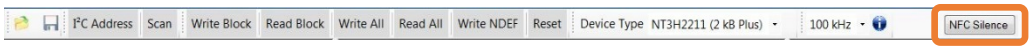

Fig 16. Peek and Poke NFC Silence control

4.3 Memory block selection

Another useful functionality of the Peek and Poke utility is given by its fluent and intuitive graphical exploration of the tag memory. As it was introduced in section 4.1, the application consists of three main panels. The left panel helps the user by selecting the memory sectors by the type of information they contain. This is done through a scroll tree menu allowing the user to explore a specific block or register. The center panel shows a grid structure that represents the hexadecimal content of the memory divided in blocks of 16 bytes. For the sake of a better understanding, the right panel displays the ASCII representation of the memory with the same structure.

Version 3.0 of Peek and Poke adds a more intuitive way to write values in the data grids. It is now possible to copy/paste 16 bytes (an entire row) of data, navigate to previous cells using the back-space key on the keyboard, or jump automatically to the next cell when a correct hex value is added in a cell.

When the user selects an item on the left menu, the specific sector is highlighted on the center and right panels to clearly identify the bytes devoted for that purpose. The content of a certain byte can be changed by modifying its value in the center panel and pressing either *Write Block* or *Write All*.

In the following subsections, the description of each node in the left panel is addressed.

4.3.1 Configuration

The *Configuration* node in the left panel will highlight the first block of the memoryThe *I²C address* byte can be changed through the dedicated button. (Section 4.2.6).

Expanding the *Configuration* node will show the five sections included in this block, allowing the user to identify the specific location for each of them.

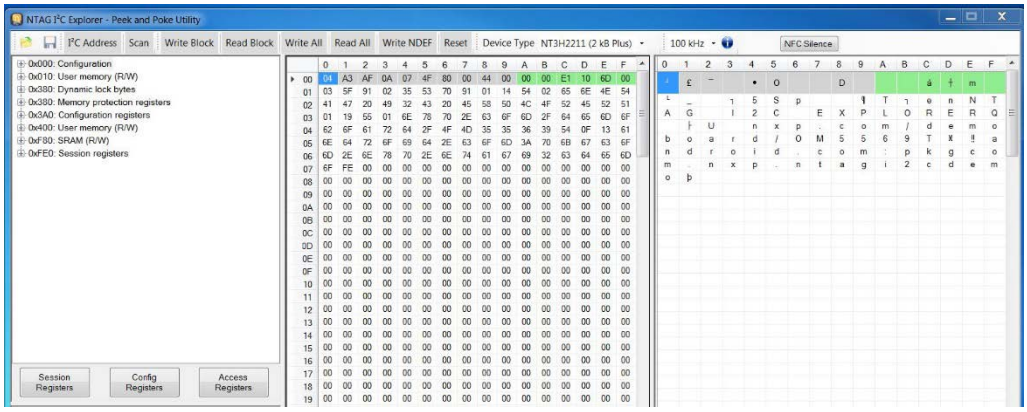

Fig 17. Memory block selection - Configuration

4.3.2 User memory

The *User Memory* node shows the content of the tag user memory in the central and right panels. The tree structure in this case allows the user to locate a specific block of the user memory. All this content is completely editable through the center panel interface.

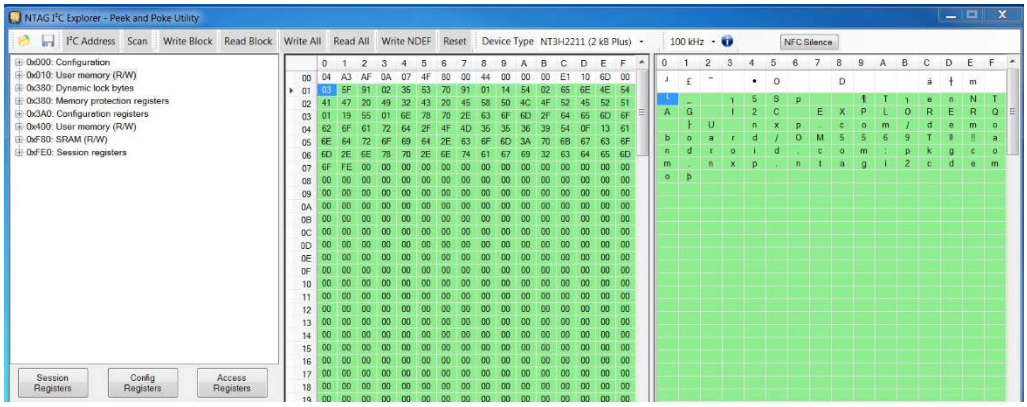

Fig 18. Memory block selection – User memory unprotected

With the new features of the NTAG I²C *plus*, it is possible to protect some parts of the memory against I²C (not only NFC). Fig 19 displays the reading of the user memory with this protection active. The protected area is shown in orange and the unprotected in green.

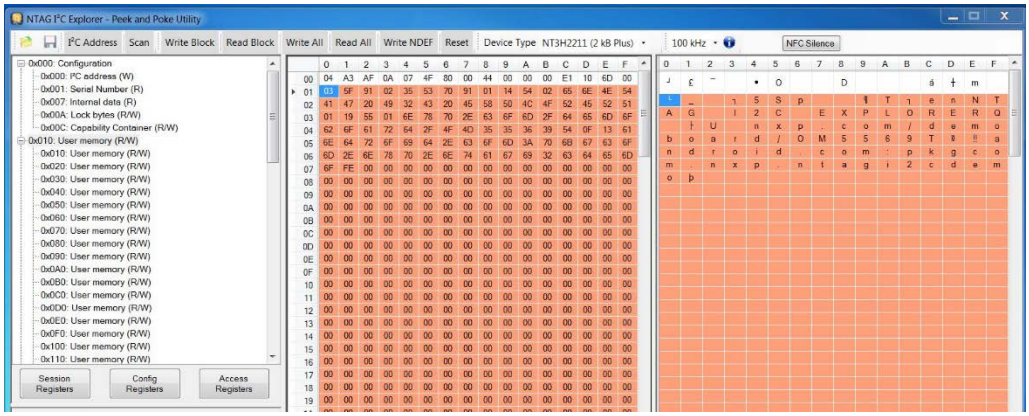

Fig 19. Memory block selection – User memory partially protected

4.3.3 Dynamic lock bytes

In order to observe the dynamic lock bytes, click on *Dynamic lock bytes* in the left panel. In the middle and right panel, one block highlighted in green should appear, which shows the memory position of the dynamic lock bytes.

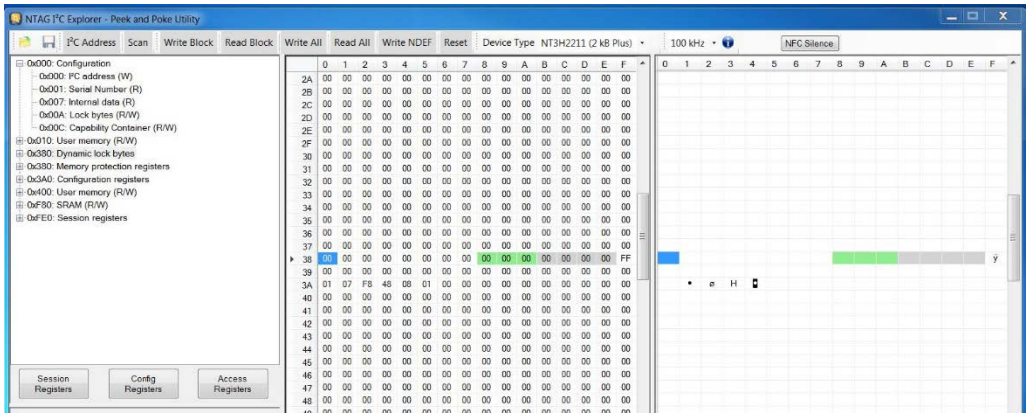

Fig 20. Memory block selection – Dynamic lock bytes

4.3.4 Memory protection registers

This field is introduced in the NTAG I²C *plus* release. It will display all options of the access registers. Fig 21 shows this new feature. In the left panel the main registers are defined and by clicking on any of them, the middle and right panel should highlight the corresponding block.

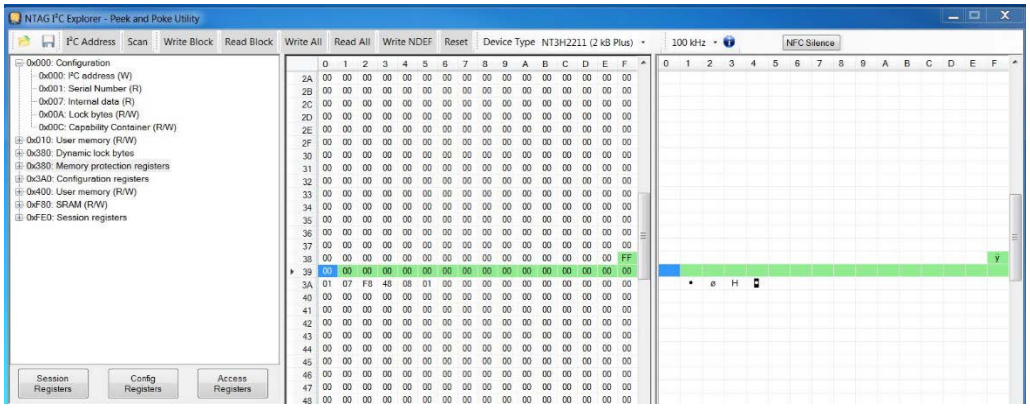

Fig 21. Memory block selection – Access registers

4.3.5 Configuration registers

You can also observe the configuration registers by clicking on *Configuration registers* in the left panel. In the middle and right panel, one block highlighted in green should appear, which shows the memory position of the configuration registers.

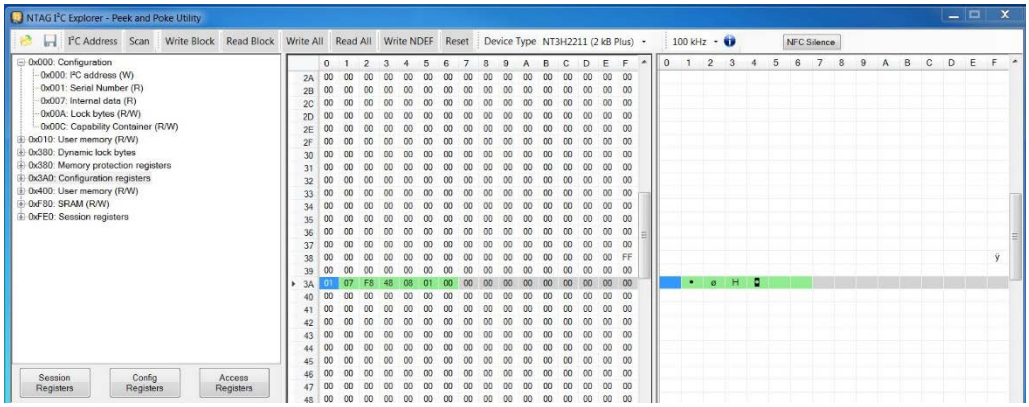

Fig 22. Memory block selection – Configuration registers

4.3.6 SRAM

To see the SRAM bytes you have to click on *SRAM* in the left panel. The middle and right panel several blocks highlighted in green should appear, which show the memory positions of the SRAM.

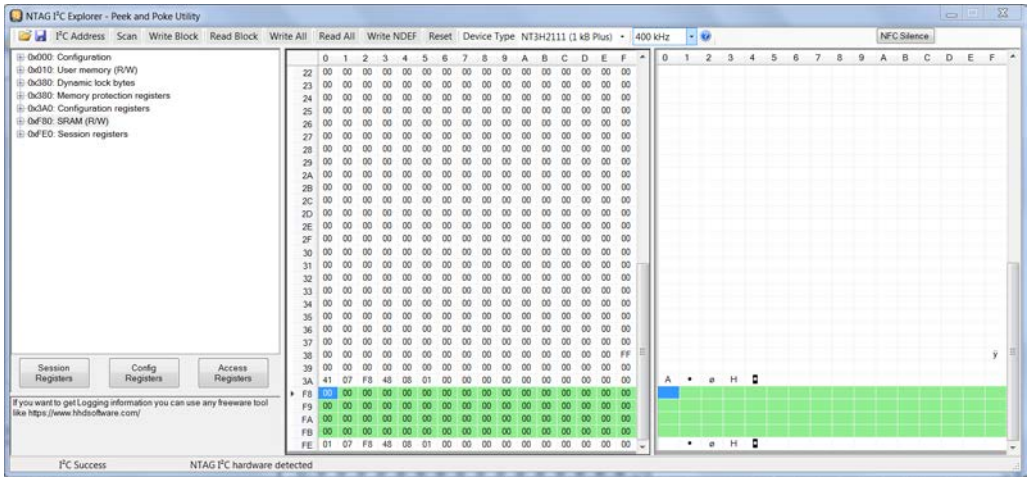

Fig 23. Memory block selection - SRAM

4.3.7 Session registers

In order to observe the session registers you can click on *Session registers* in the left panel. In the middle and right panel, the last block highlighted in green should appear, which shows the memory position of the session registers. There is also special access button which opens special window to configure Session registers, described in 4.4.2 Session registers.

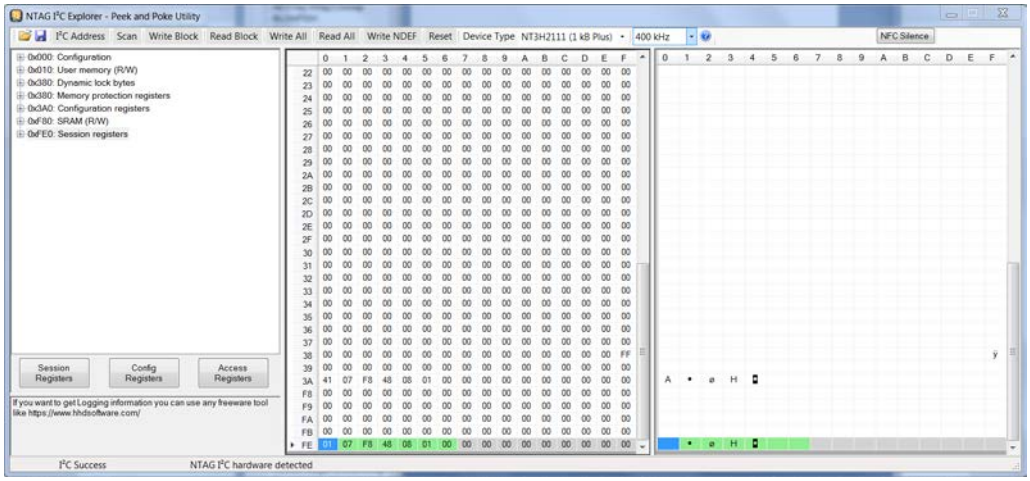

Fig 24. Memory block selection – Session registers

4.4 GUI bottom control bar details

4.4.1 USB data logging

The data that is transmitted over the USB connection can be tracked. Any freeware tool available online shall suffice.

Note: USB data logging affects the amount of time required to read / write.

4.4.2 Session registers

The user can check and edit the session registers by clicking the address 0xFE or the *Session Register* button. For a quick explanation for any of the registers listed under the session and configuration register screens, click on the small blue information (*i)* icon. This action will bring up a help screen describing the register in a bit more detail.

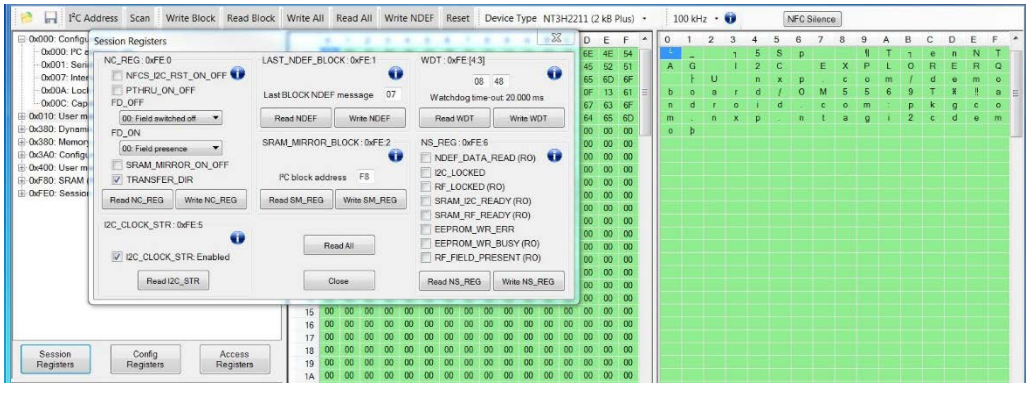

Fig 25. Peek and Poke Session Registers configuration menu

For more information on the session registers, please go to the NTAG I²C *plus* datasheet.

4.4.3 Configuration registers

The user can check and edit the configuration registers. Press the configuration register button at the bottom left of the screen or click on the grid at memory block 0x3A for NTAG I²C 1K or 0x7A for NTAG I²C 2K. For a quick explanation of a session or configuration register, click on the small blue information (*i*) icon. This action will bring up a help screen describing the register in a bit more detail.

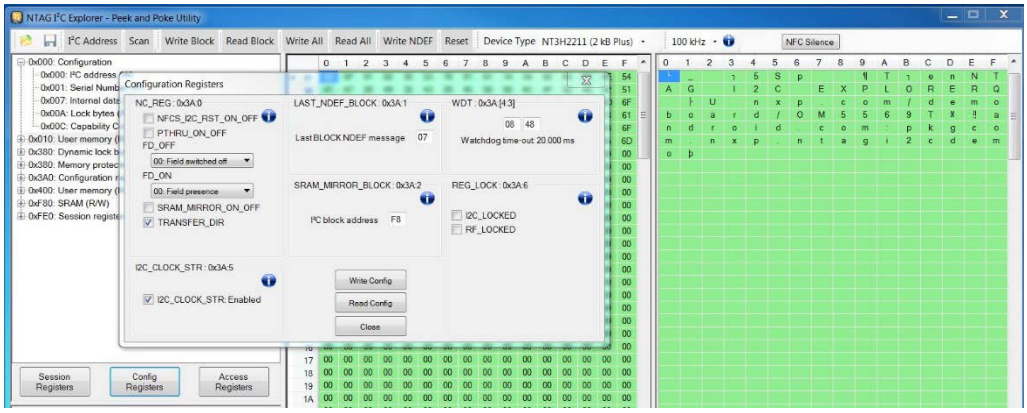

Fig 26. Peek and Poke Configuration Registers configuration menu

For more information about the configuration registers, please go to the NTAG I²C *plus* datasheet.

4.4.4 Access configuration registers

It is possible to read and write the new access registers introduced in the NTAG I²C *plus*. Pressing the Access registers button at the bottom left of the screen will display the window where it is possible to read and write these values. For a quick explanation of a session or configuration register, click on the small blue information (*i*) icon. This action will bring up a help screen describing the register in a bit more detail.

Note the warning text is highlighted in red. This warning concerns the writing and reading PWD and PACK fields. When these fields are read, it won't show the real value. These fields will be read as all zeros (00000000 for PWD and 0000 for PACK).

When writing these fields, it is important to keep in mind that the values shown in the text boxes will be written (the configuration shown in the Fig 27 will write 00000000 as PWD), so if the tag is going to become protected it is important to realize that this tag is going to be protected with that password. Note, that PC and Android app use as default password SUN = 0xFFFFFFFF, STAR = 0x55555555 and MOON = 0xAAAAAAAA.

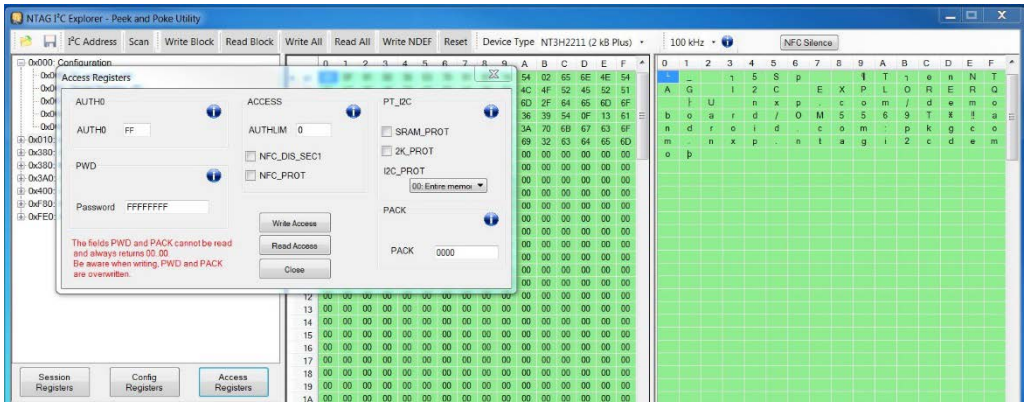

Fig 27. Peek and Poke Access Registers configuration menu

For more information about the configuration registers, please go to the NTAG I²C Datasheet.

4.5 HID Library EULA

As this application uses an external library for HID devices, the corresponding End User License Agreement is added below:

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6. List of figures

7. Contents

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