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# TWR-AUDIO-SGTL Audio Module

# User's Guide

Rev. 1.0

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## Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.0 | November 7, 2013 | Initial Release |

# 1 TWR-AUDIO-SGTL Overview

The TWR-AUDIO-SGTL is a peripheral module compatible with the Freescale Tower System (Figure 1). The TWR-AUDIO-SGTL peripheral module features the SGTL5000 audio codec and provides an audio interface for the Freescale Tower System. The SGTL5000 is a low-power stereo codec that includes a headphone amplifier and is designed to provide a comprehensive audio solution for portable products that require line-in, microphone-in, line-out, headphone-out and digital I/O. As part of the Freescale Tower System, the TWR-AUDIO-SGTL module may be used with a wide range of Tower System MCU/MPU, peripheral, sensor and communication modules.

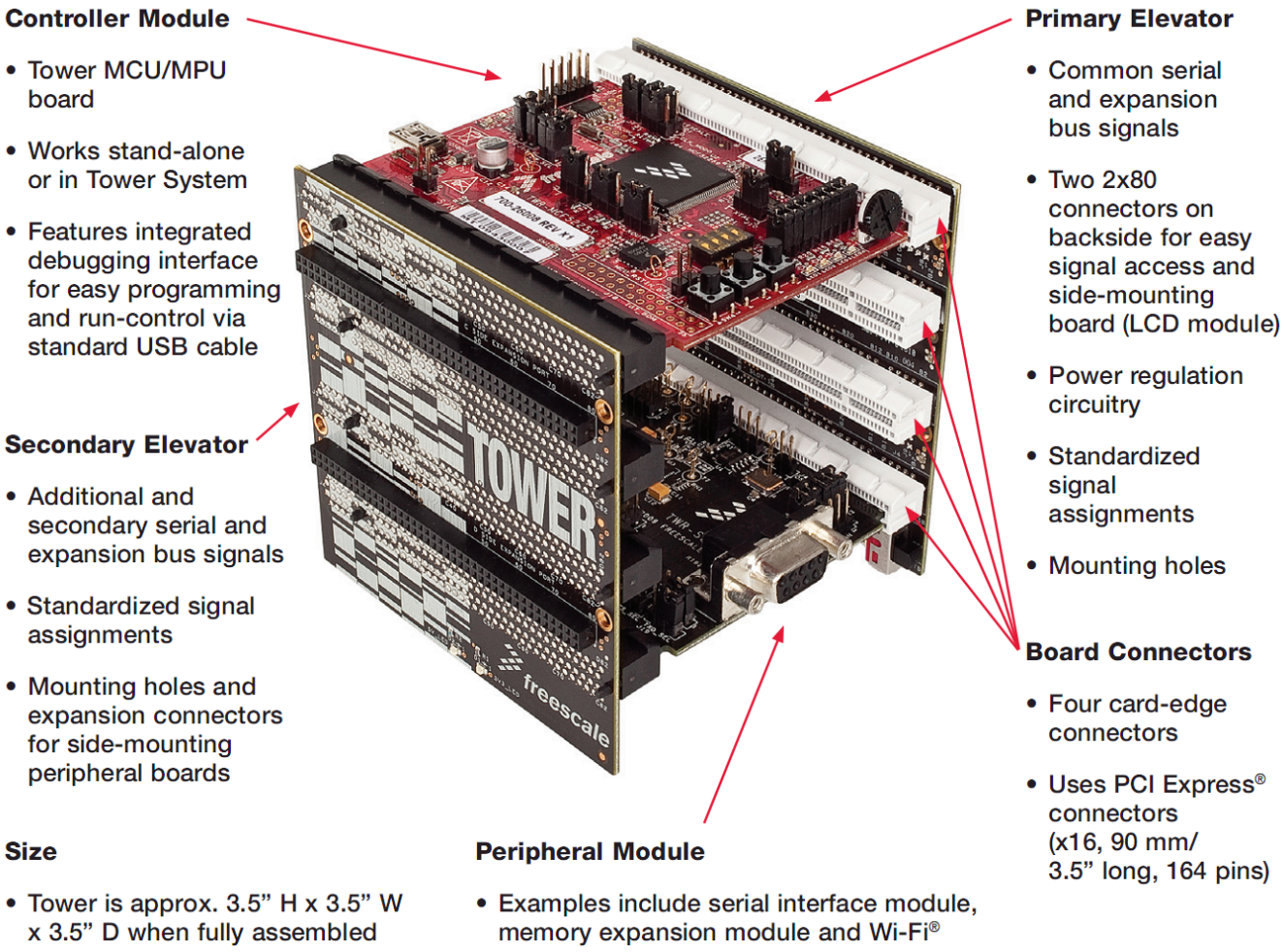


Figure 1. Freescale Tower System overview

The features of the TWR-AUDIO-SGTL peripheral module as shown in Figure 2 are:

- SGTL5000 low-power stereo codec with headphone amplifier
- Tunable clock generator
- Stereo line-in on 3.5 mm jack
- Stereo line-out on 3.5 mm jack
- Headphone output on 3.5 mm jack
- Capacitor-less headphone output on 3.5 mm jack
- Smartphone compatible headset (headphone output/microphone input) on 3.5 mm jack

- Microphone input on 3.5mm jack
- Space provided on board to mount an electret microphone
- Compatible with Tower System processor modules using Kinetis, Kinetis L, Vybrid and ColdFire+ microcontrollers


Figure 2. Callouts on top side of the TWR-AUDIO-SGTL

## 1.1 Getting started

The TWR-AUDIO-SGTL is a peripheral module for the Freescale Tower System that operates under the control of a Tower System processor module. See Section 1.3 for more information about using TWR-AUDIO-SGTL in a Tower System. There is also a lab guide available on the tool support page for the TWR-AUDIO-SGTL at the Freescale Tower System web page: *www.freescale.com/tower*

## 1.2 Reference documents

The documents and links listed below should be referenced for more information on the TWR-AUDIO-SGTL and the Tower System:

- *Freescale Tower System: www.freescale.com/tower*
- *TWR-AUDIO-SGTL-QSG: Quick Start Guide*
- *TWR-AUDIO-SGTL-SCH: Schematics*
- *TWR-AUDIO-SGTL-PWB: Design Package*
- *TWR-AUDIO-SGTL-HWER: Hardware errata*

## 1.3 Assembling the TWR-AUDIO-SGTL module

The Tower System Elevator cards have four slots available to accommodate Tower System processor and peripheral modules. An assembled Tower System can only contain one processor (MCU/MPU) module, up to 3 peripheral modules, and one side-mounting peripheral module. It is recommended that the TWR-AUDIO-SGTL peripheral module be physically located in an Elevator slot adjacent to that of the Tower Processor module. The slot, and the order of the modules in the slot, is not important,

just their adjacent location. Ensure that the TWR-AUDIO-SGTL peripheral module edge connector with the white strip is inserted in a slot of the Primary Elevator card (the one with white connectors).

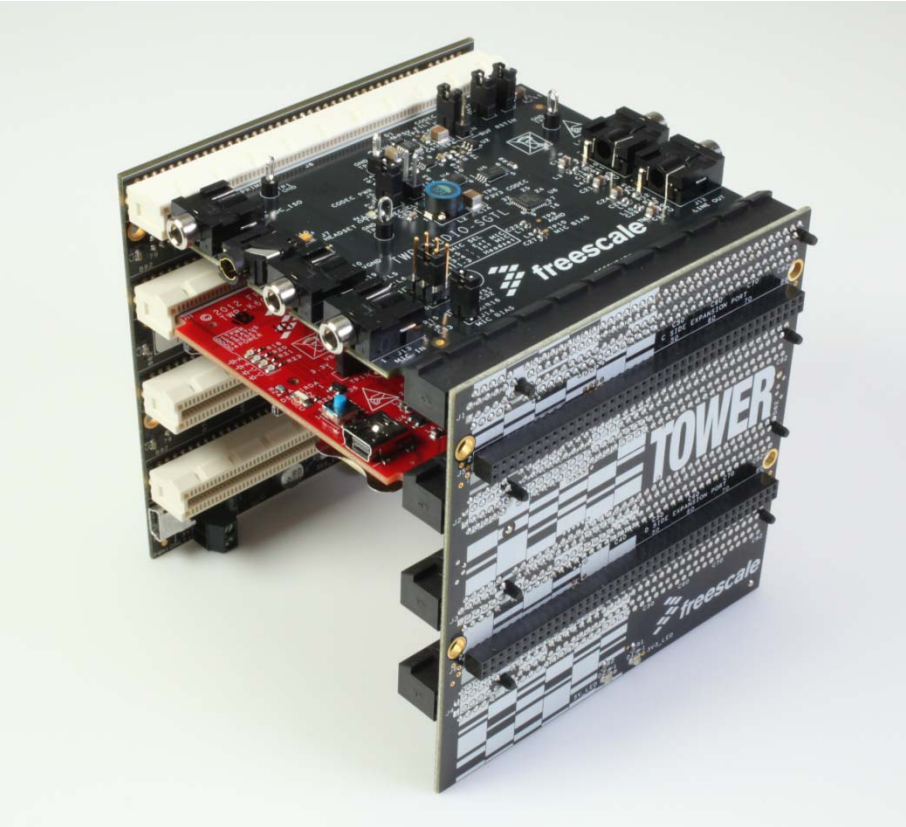


Figure 3. Assembled Tower System with TWR-AUDIO-SGTL module (in black) located in adjacent slot to processor module (in red)

# 2 TWR-AUDIO-SGTL Hardware Description

The TWR-AUDIO-SGTL is a Tower System peripheral module featuring the SGTL5000 audio codec chip. The following sections describe the hardware in more detail. This document refers to the TWR-AUDIO-SGTL Revision D and later; it is not applicable to previous schematics revisions. Compatibility with previous schematics revisions is discussed in section 2.4.1.

## 2.1 SGTL5000 Audio Codec

The SGTL5000 audio codec connects to the Tower System processor over I2C serial communication for control, and over I2S for digital audio data.

The default I2C addresses for the SGTL5000 audio codec are:

1) Write address: 0x14
2) Read address: 0x15

The maximum I2C clock rate for the SGTL5000 is 400 kHz. However, due to Tower System configuration, capacitive loading and I2C pull-up resistor values, the I2C communication may need to operate at a lower clock frequency. Jumpers J1 and J2 may be used to add 4.7k Ohm resistors to I2C SDA and SCL signal lines, to allow higher clock frequency.

Digital audio data is transported between the SGTL5000 and the processor over I2S data lines. The master/slave configuration is defined by software drivers. Note master clock requirements of the SGTL5000 for appropriate configuration.

## 2.2 Si5351A Clock Generator

The Si5351A tunable clock generator connects to the Tower System processor over I2C serial communication for control. Its default output frequency is 24.576MHz. The output frequency can be changed by programming its internal registers over I2C communication.

The I2C addresses for the Si5351A tunable clock generator are:

1. Write address: 0xDE
2. Read address: 0xDF

## 2.3 Harware Reset Considerations

The SGTL5000 chip has internal power-on hardware reset, but no external hardware reset input. Optionally, in a development environment, the power to the TWR-AUDIO-SGTL can be forced to cycle through power off/on when the Tower System processor module asserts the hardware reset signal.

Jumper J3 allows selection of the hardware reset functionality:

1) For J3 in position 1-2: Tower System processor module hardware reset does not cycle the TWR-AUDIO-SGTL power.
2) For J3 in position 2-3: Tower System processor module hardware reset will initiate a power off/power up cycle of the TWR-AUDIO-SGTL circuitry. The power off state will last approximately 20 msec.

## 2.4 Master Clock Source Selection

There is a choice of two master clock sources for the SGTL5000 in the TWR-AUDIO-SGTL module. The selection is done with jumper J6:

1) J6 off: Local Si5351A tunable clock generator (24.576MHz default frequency)
2) J6 on: Master clock from the Tower processor module I2S port

### 2.4.1 Master Clock Compatibility With Previous Module Revisions

The TWR-AUDIO-SGTL Rev D module can replace previous module revisions after proper selection of the master clock source. To replace a Rev B module, ensure that jumper J6 is on (inserted in position 1-2), to select the master clock from the Tower processor module. To replace a Rev B1 module, ensure that jumper J6 is off (not inserted in position 1-2), to select the master clock from the on-board clock generator.

## 2.5 I2S Interface

The I2S interface has a serial data input, a serial data output, a frame sync clock (also called left/right clock) and a serial bit clock. The two clock lines are used to clock both data lines. The I2S signals are connected to the Tower System processor module I2S port.

## 2.6 I/O connectors

All the input and output connectors on the TWR-AUDIO-SGTL are described in the following sections.

### 2.6.1 Analog audio line level stereo output

The analog audio line level stereo output is available at the stereo 3.5mm connector J12. These outputs support loads of 10k Ohm or more.

### 2.6.2 Analog audio line level stereo input

The analog audio line level stereo input is available at the stereo 3.5mm connector J9.

### 2.6.3 Analog audio stereo headphone outputs

The analog audio stereo headphone outputs are available as follows:

1) At the 3.5mm connectors J4 and J7 – through DC blocking capacitors
2) At the 3.5mm connector J10 – using virtual headphone ground and no DC blocking capacitors

The SGTL5000 audio codec can drive a single headphone load, so only one of connectors J4, J7 or J10 may be used at a time.

Note that the capacitor-less headphone output at connector J10 must be used only with stereo headphones. This output should not be used to connect to amplifiers, or to headsets with microphones, otherwise the virtual headphone ground may be short-circuited.

Recommended headphone impedance is in the range of 16 to 32 Ohms.

### 2.6.4 Analog audio mono microphone inputs

There are three options for microphone input to the SGTL5000:

1) Board mounted microphone P1 – the TWR-AUDIO- SGTL module ships without the P1 microphone on the board. If desired, P1 can be soldered at its location on the board. Recommended P1 microphone is the Panasonic part WM-64PCT or equivalent. Microphone bias must be supplied by ensuring that jumper J14 is in position 1-2. This input is selected when jumper J11 is in position 3-4.
2) External microphone input 3.5mm connector J13 – a microphone from a PC headset can be plugged into the J13 connector. Microphone bias is supplied from a 3.3V source through a 10k Ohm resistor. This input is selected when jumper J11 is in position 3-5.
3) Smartphone headset input 3.5mm connector J7 – a Smartphone headset with headphones and microphone can be plugged into the J7 connector. Microphone bias must be supplied by ensuring that jumper J14 is in position 1-2. The iPhone® headset is compatible with the J7 connector. This input is selected when jumper J11 is in position 1-3.

Note that not all Smartphone headsets are compatible with the signals at the J7 connector. Ensure that the headset 3.5mm plug has the correct signal connectivity as shown below:

1) Tip: Headphone Left Channel Output
2) Ring: Headphone Right Channel Output
3) Ring: Ground
4) Sleeve: Microphone Input

## 2.7 Jumper table

There are several jumpers on the TWR-AUDIO-SGTL that provide configuration selection. Figure 4 shows the locations of the jumpers, with the default positions in red. Refer to Table 1 for details. The **default** installed jumper settings are shown in **bold** in the table.

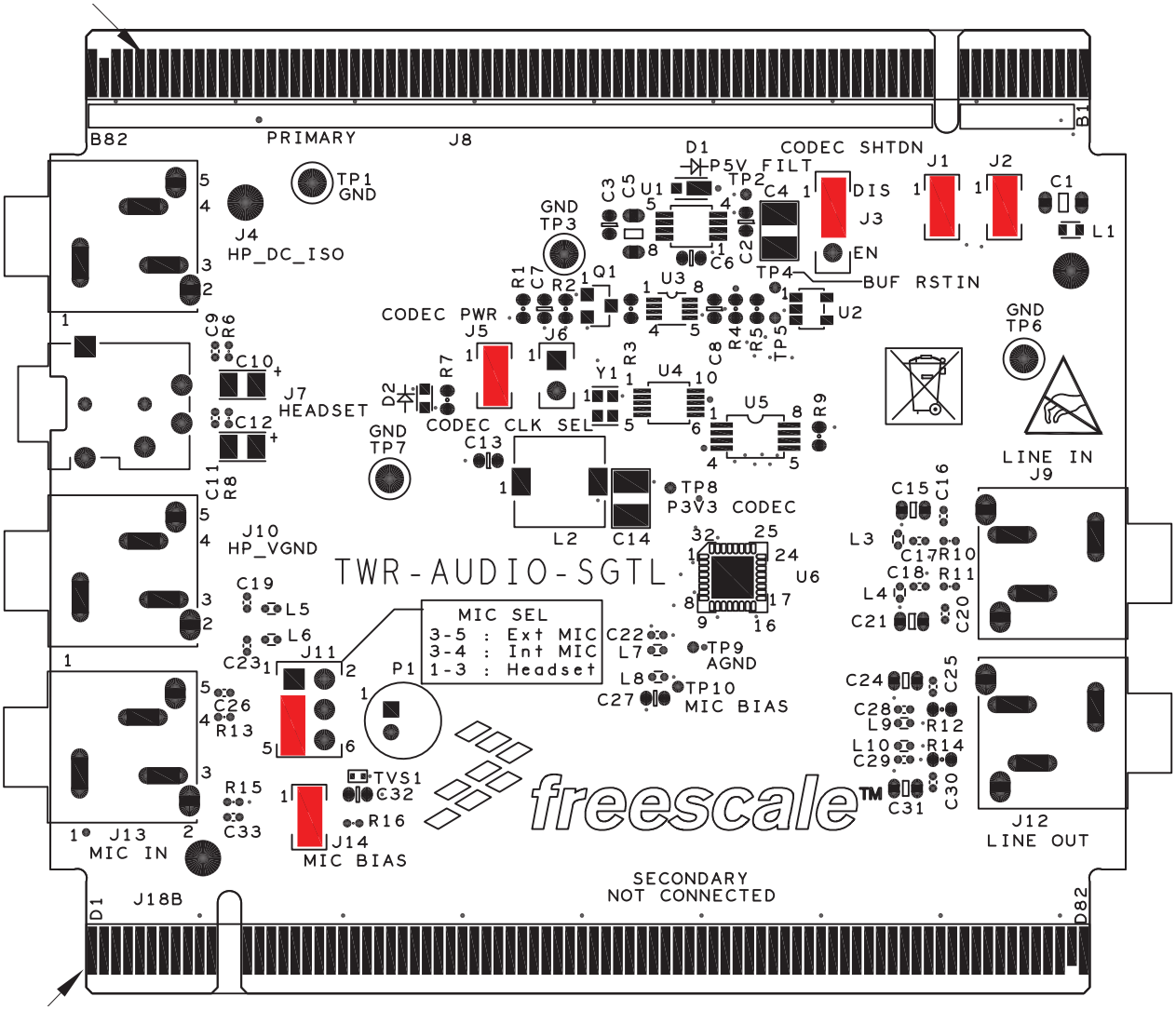


Figure 4. Location of TWR-AUDIO-SGTL jumpers

Table 1. TWR-AUDIO-SGTL jumpers

| Jumper | Option | Setting | Description |
|---|---|---|---|
| J1 | Adds 4.7k Ohm pull-up resistor to I2C SDA data line | **ON** | Pull-up added |
| | | OFF | Resistor disconnected |
| J2 | Adds 4.7k Ohm pull-up resistor to I2C SCL data line | **ON** | Pull-up added |
| | | OFF | Resistor disconnected |
| J3 | Reset shutdown selection | **1-2** | No shutdown |
| | | 2-3 | Hardware Reset causes shutdown cycle |
| J5 | Disable audio codec | **ON** | Audio codec enabled |
| | | OFF | Audio codec disabled |
| J6 | Master clock source selection | **OFF** | Si5351A (24.576MHz default) |
| | | ON | MCLK from processor module |
| J11 | Microphone input selection | **3-5** | External microphone |
| | | 3-4 | Internal microphone |
| | | 1-3 | Smartphone headset |
| J14 | Microphone bias | **1-2** | Microphone bias applied |
| | | OFF | Microphone bias not applied |

## 2.8 Tower Elevator connections

The TWR-AUDIO-SGTL features two expansion card-edge connectors that interface to the Primary and Secondary Elevator boards in a Tower System. The Primary Elevator connector, comprised of sides A (bottom) and B (top), is used by the TWR-AUDIO-SGTL. The Secondary Elevator connector, comprised of sides C (bottom) and D (top), have no connections. Table 2 provides the pinout for the Primary Elevator connector. An **x** in the Used column indicates that a connection is made to that pin on the connector. An **x** in the Jmp column indicates that a jumper is provided to configure the connection.

Table 2. TWR-AUDIO-SGTL Primary Elevator connector pinout

| TWR-AUDIO-SGTL Primary Elevator connector | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin # | Side B | | | | Pin # | Side A | | | |
| | Name | Usage | Used | Jmp | | Name | Usage | Used | Jmp |
| B1 | **5V** | **5.0V Power** | **X** | | A1 | **5V** | **5.0V Power** | **X** | |
| B2 | **GND** | **Ground** | **X** | | A2 | **GND** | **Ground** | **X** | |
| B3 | **3.3V** | **3.3V Power** | **X** | | A3 | **3.3V** | **3.3V Power** | **X** | |
| B4 | ELE_PS_SENSE | Power Sense | | | A4 | **3.3V** | **3.3V Power** | **X** | |
| B5 | **GND** | **Ground** | **X** | | A5 | **GND** | **Ground** | **X** | |
| B6 | **GND** | **Ground** | **X** | | A6 | **GND** | **Ground** | **X** | |
| B7 | SDHC_CLK / SPI1_CLK | | | | A7 | I2C0_SCL | I2C0_SCL | **X** | |
| B8 | SDHC_D3 / SPI1_CS1_b | | | | A8 | I2C0_SDA | I2C0_SDA | **X** | |
| B9 | SDHC_D3 / SPI1_CS0_b | | | | A9 | GPIO9 / CTS1 | | | |
| B10 | SDHC_CMD / SPI1_MOSI | | | | A10 | GPIO8 / SDHC_D2 | | | |
| B11 | SDHC_D0 / SPI1_MISO | | | | A11 | GPIO7 / SD_WP_DET | | | |
| B12 | ETH_COL | | | | A12 | ETH_CRS | | | |
| B13 | ETH_RXER | | | | A13 | ETH_MDC | | | |
| B14 | ETH_TXCLK | | | | A14 | ETH_MDIO | | | |

| TWR-AUDIO-SGTL Primary Elevator connector | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin # | Side B | | | | Pin # | Side A | | | |
| | Name | Usage | Used | Jmp | | Name | Usage | Used | Jmp |
| B15 | ETH_TXEN | | | | A15 | ETH_RXCLK | | | |
| B16 | ETH_TXER | | | | A16 | ETH_RXDV | | | |
| B17 | ETH_TXD3 | | | | A17 | ETH_RXD3 | | | |
| B18 | ETH_TXD2 | | | | A18 | ETH_RXD2 | | | |
| B19 | ETH_TXD1 | | | | A19 | ETH_RXD1 | | | |
| B20 | ETH_TXD0 | | | | A20 | ETH_RXD0 | | | |
| B21 | GPIO1 / RTS1 | | | | A21 | I2S0_MCLK | I2S0_MCLK | X | |
| B22 | GPIO2 / SDHC_D1 | | | | A22 | I2S0_DOUT_SCK | I2S0_SCLK | X | |
| B23 | GPIO3 | | | | A23 | I2S0_DOUT_WS | I2S0_LRCLK | X | |
| B24 | CLKIN0 | | | | A24 | I2S0_DIN0 | I2S0_DOUT | X | |
| B25 | CLKOUT1 | | | | A25 | I2S0_DOUT0 | I2S0_DIN | X | |
| B26 | **GND** | **Ground** | X | | A26 | **GND** | **Ground** | X | |
| B27 | AN7 | | | | A27 | AN3 | | | |
| B28 | AN6 | | | | A28 | AN2 | | | |
| B29 | AN5 | | | | A29 | AN1 | | | |
| B30 | AN4 | | | | A30 | AN0 | | | |
| B31 | **GND** | **Ground** | X | | A31 | **GND** | **Ground** | X | |
| B32 | DAC1 | | | | A32 | DAC0 | | | |
| B33 | TMR3 | | | | A33 | TMR1 | | | |
| B34 | TMR2 | | | | A34 | TMR0 | | | |
| B35 | GPIO4 | | | | A35 | GPIO6 | | | |
| B36 | **3.3V** | **3.3V Power** | X | | A36 | **3.3V** | **3.3V Power** | X | |
| B37 | PWM7 | | | | A37 | PWM3 | | | |
| B38 | PWM6 | | | | A38 | PWM2 | | | |
| B39 | PWM5 | | | | A39 | PWM1 | | | |
| B40 | PWM4 | | | | A40 | PWM0 | | | |
| B41 | CANRX0 | | | | A41 | RXD0 | | | |
| B42 | CANTX0 | | | | A42 | TXD0 | | | |
| B43 | 1WIRE | | | | A43 | RXD1 | | | |
| B44 | SPI0_MISO | | | | A44 | TXD1 | | | |
| B45 | SPI0_MOSI | | | | A45 | VSS | | | |
| B46 | SPI0_CS0_b | | | | A46 | VDDA | | | |
| B47 | SPI0_CS1_b | | | | A47 | VREFA1 | | | |
| B48 | SPI0_CLK | | | | A48 | VREFA2 | | | |
| B49 | **GND** | **Ground** | X | | A49 | **GND** | **Ground** | X | |
| B50 | SCL1 | | | | A50 | GPIO14 | | | |
| B51 | SDA1 | | | | A51 | GPIO15 | | | |
| B52 | GPIO5 / SD_CARD_DET | | | | A52 | GPIO16 | | | |
| B53 | USB0_DP_PDOWN | | | | A53 | GPIO17 | | | |
| B54 | USB0_DM_PDOWN | | | | A54 | USB0_DM | | | |
| B55 | IRQ_H | | | | A55 | USB0_DP | | | |
| B56 | IRQ_G | | | | A56 | USB0_ID | | | |
| B57 | IRQ_F | | | | A57 | USB0_VBUS | | | |
| B58 | IRQ_E | | | | A58 | TMR7 | | | |
| B59 | IRQ_D | | | | A59 | TMR6 | | | |
| B60 | IRQ_C | | | | A60 | TMR5 | | | |
| B61 | IRQ_B | | | | A61 | TMR4 | | | |
| B62 | IRQ_A | | | | A62 | RSTIN_b | RSTIN_B | X | X |

| TWR-AUDIO-SGTL Primary Elevator connector | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin # | Side B | | | | Pin # | Side A | | | |
| | Name | Usage | Used | Jmp | | Name | Usage | Used | Jmp |
| B63 | EBI_ALE / EBI_CS1_b | | | | A63 | RSTOUT_b | | | |
| B64 | EBI_CS0_b | | | | A64 | CLKOUT0 | | | |
| B65 | **GND** | **Ground** | **X** | | A65 | **GND** | **Ground** | **X** | |
| B66 | EBI_AD15 | | | | A66 | EBI_AD14 | | | |
| B67 | EBI_AD16 | | | | A67 | EBI_AD13 | | | |
| B68 | EBI_AD17 | | | | A68 | EBI_AD12 | | | |
| B69 | EBI_AD18 | | | | A69 | EBI_AD11 | | | |
| B70 | EBI_AD19 | | | | A70 | EBI_AD10 | | | |
| B71 | EBI_R/W_b | | | | A71 | EBI_AD9 | | | |
| B72 | EBI_OE_b | | | | A72 | EBI_AD8 | | | |
| B73 | EBI_D7 | | | | A73 | EBI_AD7 | | | |
| B74 | EBI_D6 | | | | A74 | EBI_AD6 | | | |
| B75 | EBI_D5 | | | | A75 | EBI_AD5 | | | |
| B76 | EBI_D4 | | | | A76 | EBI_AD4 | | | |
| B77 | EBI_D3 | | | | A77 | EBI_AD3 | | | |
| B78 | EBI_D2 | | | | A78 | EBI_AD2 | | | |
| B79 | EBI_D1 | | | | A79 | EBI_AD1 | | | |
| B80 | EBI_D0 | | | | A80 | EBI_AD0 | | | |
| B81 | **GND** | **Ground** | **X** | | A81 | **GND** | **Ground** | **X** | |
| B82 | **3.3V** | **3.3V Power** | **X** | | A82 | **3.3V** | **3.3V Power** | **X** | |

FCC CLASS A DEVICE: "This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation."

CE EMC Directive: This device complies with European Union EMC Directive and the Low Voltage Safety Directive (LVD) *[Product exhibits some anomalous behavior observed over the frequency range of 125 MHz-350 MHz during Immunity testing]*

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