RD-K358BMU User Guide

by: NXP Semiconductors

1. Introduction

The RD-K358BMU is the third version of NXP's reference Battery Management Unit (BMU) for evaluation and development purposes. It is ideal for rapid prototyping of a high voltage battery management System (HVBMS) hardware and software. In order to achieve the HVBMS goals the board contains: S32K358, FS2613, HB2000, TJA1145A, TJA1057, PCA2131, NBP8 or MC40XS6500 devices. Together with RD33774CNT3EVB it allows the user to connect lithium battery in wide variety of cell configuration.

Contents

l.	Introduction	1
2.	Caution	2
3.	System Description	4
1.	Board Description	5
5.	Power Supply	7
5.	SBC Debug Mode	10
7.	Connectors	12
3.	Communication Interfaces	16
).	Auxiliary Circuits	20
10.	Board Accessories	27
11.	Tips and Recommendations	29
12.	MCU Pinout	



Figure 1. RD-K358BMU board



2. Caution

NXP provides the enclosed product(s) under the following conditions:

This reference design is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This reference design may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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Should this reference design not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

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WARNING

• This development tool set may operate in an environment that includes dangerous voltages that can result in electrical shock, fire hazard, and personal injury if not properly handled or applied. You must use this development tool with necessary caution and

appropriate safeguards to avoid personal injury or property damage.

- Only qualified persons familiar with the risks associated with handling high voltage electrical systems and subsystems can manipulate this evaluation board.
- You should operate this evaluation board in a lab environment only. The evaluation board is not a finished end-product fit for general consumer use.

3. System Description

3.1. System block diagram

The RD-K358BMU board is intended but not limited to work in system as described below. The proposed system has the following three parts:

- 1. The battery junction box (BJB) is taking care of current measurement, high voltage measurements and isolation monitoring. For details about the BJB, refer to the BJB user manual.
- 2. The cell monitoring unit (CMU) is intended to be connected directly to battery cells. It takes care of the cell voltage measurement, temperature measurement, bus bar monitoring and cell balancing. In proposed system twelve analog front end (AFE) controllers are distributed over four PCBs. AFEs are connected in two daisy chains distributed into four clusters in so called half-distributed configuration. As a given example, the system can monitors 190 cells + busbars for NMC chemistry using 12 AFEs or 216 cells + busbars monitoring for LFP chemistry using 14 AFEs, in total. These are just a typical examples and not a system limitations. By adding more AFE into daisy chain, system can monitor more cells if required. The communication protocol supports up to 62 nodes which mean more than 1000 cells. For more detail about CMU, refer to the CMU user manual or AN13233.
- 3. The battery management unit (BMU) is based on S32K358 MCU. It is responsible for collecting all data communicated to vehicle control unit (VCU) and makes important safety decisions. Detailed functionality of this unit will be described in this document.

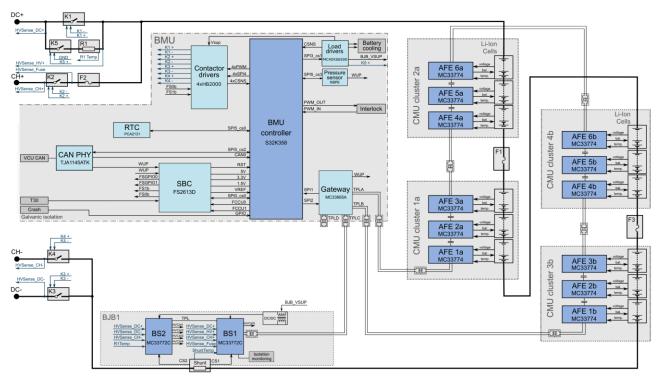


Figure 2. 800V HVBMS system configuration example for NMC chemistry RD-K358BMU User Guide, User Guide, Rev. 0, 04/2023

4. Board Description

4.1. Chipset features

The RD-K358BMU board is equipped with the latest NXP chipset. The base of the BMU board is micro controller unit (MCU) from S32K3xx family and system basis chip (SBC) FS2613. These components have been especially designed for ASIL-D systems, like for example a battery management system.

S32K358 MCU key features:

- 1x LS Arm[®] Cortex-M7[®] + 1x Cortex-M7 @ 240 MHz, 8 MB Flash , 1152 KB SRAM
- Fault collection and control unit, watchdog, clock/power monitor
- 8x CAN-FD, 6xLPSPI, 32ch FlexIO
- 3x 24 16bit EMIOS timer, 3x 24ch 12-bit ADC
- HSE security engine
- MAXQFP172 package reduces footprint by up to 55 %

FS2613 SBC key features:

- Configurable PMIC, 3rd generation of NXP safety SBCs
- Support system low power modes (Standby and LPOFF) with long duration timer
- 2x LDO configurable 3.3 V or 5.0 V, up to 300 mA
- 2x 125 mA trackers for external sensors supply redundancy
- Voltage reference
- Dual fail safe outputs with delay for increased fail safe system behavior
- Front boost converter for HEV

4.2. Board features

Interfaces:

- 3x CAN-FD interfaces, one with partial networking
- 4x TPL interface (loopback mode supported)
- 4x Contactor drivers with PWM economization and current monitoring
- 2x short circuit protected outputs for battery cooling/heating valves
- Short circuit and reverse polarity protected output for battery junction box power supply

Advanced features:

- On board pressure sensor for thermal runaway detection
- PWM based interlock pilot loop

Power Supply

• MCU independent real time clock source

Wake up sources:

- SBC periodic wake up
- VCU CAN partial networking wake up
- CMU CAN wake up from CMU
- ETPL wake up from CMU
- Pressure sensor thermal runaway event wake up

4.3. Connectors and integrated circuit location

The following figure shows distribution of connector and integrated circuit on the board. For detailed connector pinout, refer to Connectors.

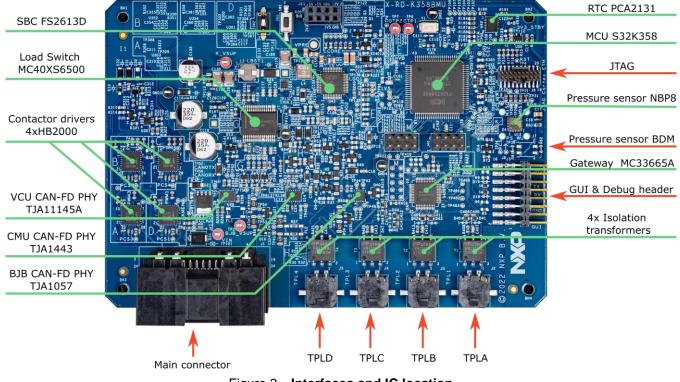


Figure 3. Interfaces and IC location

5. Power Supply

5.1. BMU power supply input

Board is supplied from main connector J1 pins 1 and 3 for GND and pins 2 and 4 for +12 V. This board have built-in polarity protection and power supply input filtering. All standby functions at this board are enabled by default. To optimize current consumption in standby mode, user can disable functions which are not used in application. This may be done by removing zero ohm resistor (R107 – VCU CAN, R422 – TPL, R62 – CMU CAN, R4 - RTC and pressure sensor).

Parameter	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input voltage	V _{T30}	6.0	12	20	V
Input voltage in degraded mode ^{*1}	V _{T30}	3.3			V
Run current consumption	IRUN		120		mA
Input current in LPOFF mode	I LPOFF		30		μA
Standby current with minimal configuration	ISTBYMIN		46 ^{*2}		μA
Standby current adder for VCU CAN (partial networking)	ISTBYVCU		76		μA
Standby current adder for TPL	ISTBYTPL		4		μA
Standby current adder for CMU CAN	Ізтвусми		6		μA
Standby current adder for RTC + pressure sensor	ISTBYRTCPS		23		μA
Standby current with all standby functions enabled	I _{STBY}		155 ^{*3}		μA

Table 1. Board input power supply specification

* all values measured at 23 °C, $V_{T30} = 12$ V, unless stated otherwise, LPOFF and standby current measured at T30 input terminals.

 Proper power supply of MCU and on-board low voltage circuitry is ensured by integrated SBC boost pre-regulator! It does not guarantee proper functionality of other 12V circuits e.g. contactor circuits, interlock pilot loop, heating/cooling solenoids or BJB power supply.

- 2) Enabled standby functions: SBC, Load drivers.
- 3) Enabled standby functions: SBC, CMU CAN, battery gateway, VCU CAN with partial networking, Pressure sensor, RTC, Load drivers.

Internal power supplies are managed by the FS2613 system basis chip (SBC). The FS26 is a family of automotive Safety SBC devices with multiple power supplies designed to support entry and mid-range safety micro controllers like S32K3. The SBC switch mode power supply is also active in standby mode. It ensures higher efficiency and lower standby current in comparison to a conventional approach with LDOs.

The FS26 features multiple switch mode regulators as well as two LDO voltage regulators to supply the microcontroller, sensors, peripheral ICs and communication interfaces. It offers a high precision voltage reference available to the system as well as reference voltage for two independent voltage tracking regulators.

5.2. On-board power distribution

On-board system basis chip the FS2613 ensures voltage regulation, over voltage, under voltage and overcurrent protections for low voltage rails present on this board. Loads across power rails are distributed as shown in the following figure and table. For more information about power supply distribution in standby mode please refer to Power modes and wake up.

Power Supply

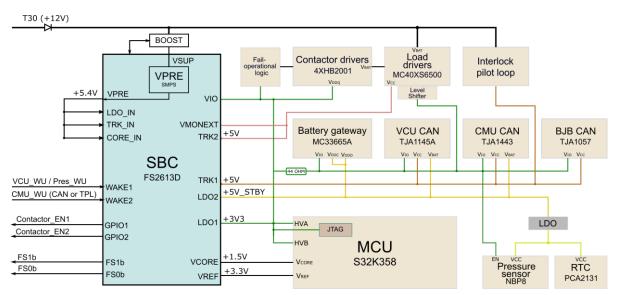


Figure 4. Power supply distribution in RUN mode

SBC output	Loads	Net alias	Availability	Voltage [V]	Max. out current [mA]
VPRE	LDO1, LDO2, TRK1, TRK2, VCORE	FS26_VPRE	RUN, STANDBY	5.5	1500
VCORE	MCU Core	V15_MCU	RUN	1.5	800
LDO1	MCU HVA, HVB, Contactor drivers, Vio, JTAG	+3V3_LDO1	RUN	3.3	300
LDO2	CMU CAN, VCU CAN, Battery gateway, RTC, Pressure sensor ^{*1}	+5V_LDO2	RUN, STANDBY	5.0	300
TRK1	CAN's Vcc	+5V_TRK1	RUN	5.0	125
TRK2	Load drivers	+5V_TRK2	RUN	5.0	125
VREF	MCU ADC reference	VREF	RUN	3.3	10

1) RTC and pressure sensor connected using external LDO to regulate voltage to 3.3V from V_{LDO2} voltage.

5.3. Power modes and wake up

5.3.1. BMU power modes

BMU board can be operated in at least four power modes:

- Run
- Run with low input voltage
- Standby
- LPOFF

In run mode, all on-board devices are supplied, and system have access to full BMU functionality. Power supply distribution and voltage levels are shown in Figure 4.

In run mode with low input voltage, the SBC boost pre-regulator ensure correct and stable power supply of its output rails even with low supply voltage. This guarantees correct operation of all ICs supplied from SBC, however it does not guarantee proper functionality of 12 V circuits e.g. contactor circuits, interlock pilot loop, heating/cooling solenoids or BJB power supply. See Table 1 for supply voltage range specification.

In standby mode board current consumption is reduced. Only necessary ICs are supplied, most of SBC power rails including MCU power supply are switched off. Switching from run into standby mode is done by a go to standby SPI request coming from MCU to SBC. If all conditions described in SBC datasheet are met, SBC enters standby mode. Power supply distribution is shown in the figure below.

In LPOFF mode board have minimal power consumption, however most of the functionality is disabled including most of the wake-up sources. During LPOFF LDO2 output is disabled, which mean only possible wake up source is SBC. (e.g. SBC LDT).

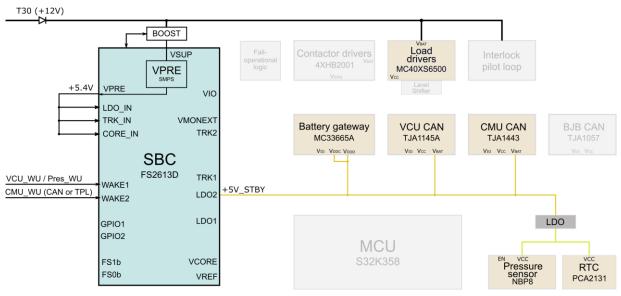


Figure 5. Power supply rails in stand-by mode

5.3.2. BMU wake up sources

Board has five possible wake-up sources:

- Internal SBC event (e.g. Long Duration Timer (LDT))
- VCU CAN (TJA1145A) available at SBC WAKE1 input. (partial networking capable)
- Pressure sensor event available at SBC WAKE1 input.
- CMU ETLP wake available at SBC WAKE2.
- CMU CAN wake available at SBC WAKE2.

6. SBC Debug Mode

6.1. MCU firmware debugging in SBC debug mode

To continuously check the activity of the microcontroller software and its ability to perform basic computing, a challenger watchdog is implemented through the SPI bus. The verification is performed by the FS26 while waiting for a specific response from the microcontroller during a predefined period called window.

If the watchdog is not properly refreshed, SBC safety outputs FSxB and RSTB are asserted and SBC tries to recover MCU functionality by resetting its power. This process is accompanied with blinking orange LED D26. Loading firmware over JTAG at this mode is not supported.

Periodic power supply resetting, or issue with firmware loading typically happens in the following cases:

- Missing SBC WD refresh routine
- Loading new BMU firmware via JTAG without activating debug mode
- Using code breakpoints during debugging without activating debug mode
- Missing or wrong BMU firmware

WARNING

- MCU firmware update in SBC normal mode will not work. To be able to flash new firmware or do software debugging, SBC debug mode must be activated.
- Entering SBC debug mode is described in section Entering SBC debug mode.

6.1.1. Entering SBC debug mode

Debug circuit is intended for development purposes only and must be removed for production.

There are two options to enter debug mode, it is recommended to use first option:

- 1. Press and hold SW1 (or set SW2 to ON position) while connecting T30 power supply and release SW1 after the T30 connected. Make sure D26 is solid ON afterwards.
- 2. FS2613 debug pin is accessible at connector J11 pin 4. Applying a voltage between 2.5 V and 6 V to this pin, before the board power supply is connected, ensures debug mode.

Make sure T30 power supply is in range from +11 V to +14 V while entering debug mode. Power supply current limit must be at least 2 A to meet sufficient input voltage steepness for debug mode entering. In case of slow input voltage ramp-up, debug mode may not be activated. This may typically happen when power supply with soft start function is used. Therefore, it is recommended to make/brake power supply at 12 V DC side and not at 230 AC side.

Blinking D26 indicates MCU power supply is being reset, which means debug mode was not successfully activated.

6.1.2. Leave debug mode

Due to safety reasons, FSxB safety outputs functionality is limited in debug mode. To enable full board functionality (e.g. contactor control) debug mode must be left. The following are the options to leave debug mode. Make sure SW2 is in OFF position.

- 1. To leave debug mode BMU power supply (T30) must be disconnected and connected again. Actual SBC state can be checked in FS_STATES register via SPI.
- 2. Request to leave debug mode can be entered into SBC FS_STATES register via SPI.

WARNING

Avoid immediate and unconditional "leave debug mode" command in MCU firmware. Such a command may cause "dead lock", where loading of new MCU firmware through JTAG may be not possible as SBC is always switched to normal mode right after startup in such a case.

7. Connectors

7.1. Vehicle connector

J1 is the main BMU connector and provides access to functionalities described in Table 4. Connector part number specification can be found in Table 3.

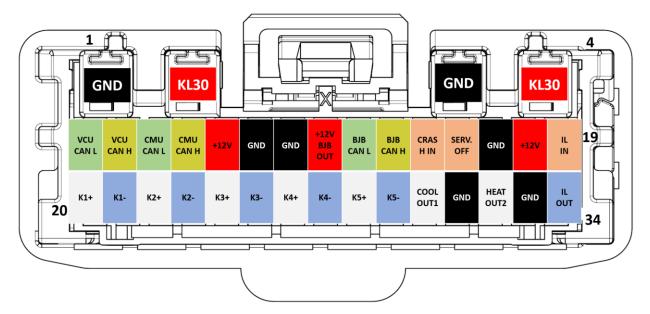


Figure 6. Main connector pinout (wire side)

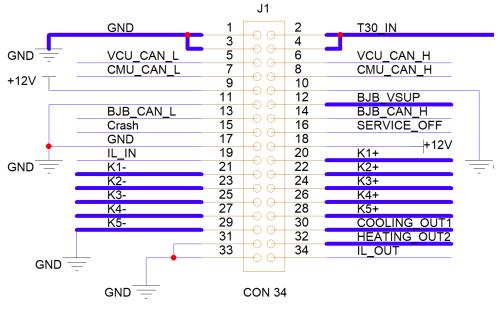


Figure 7. Vehicle connector pinout (schematic view)

0349590340

Table 5. Venicle connector FN specification				
Location	Describtion	PN.		
PCB side	Mini50 Unsealed Right-Angle Hybrid Header, 3 Rows, 34 Circuits, Polarization Option A, Black,	0349610340		

Mini50 Unsealed Receptacle, 3 Rows, with CPA, 34 Circuits, Polarization

Table 3. Vehicle connector PN specification

Purpose	Signal name	PIN #	Wire color
-	GND	1	NC
_	KL30	2	NC
Power supply	GND	3	Black
	KL30	4	Red
	VCU CAN_L	5	Green
Vehicle CAN FD port	VCU CAN_H	6	Yellow
	CMU CAN_L	7	Green
	CMU CAN_H	8	Yellow
CMU CAN	12V	9	Red
	GND	10	Black
	GND	11	Black
BJB CAN	12V BJB OUT	12	Red
	BJB CAN_L	13	Green
	BJB CAN_H	14	Yellow
Crash signal input	Crash in	15	Brown/Pink
Service disconnect	Serv off	16	Brown/Pink
GND	GND	17	Black
12V	12V	18	Red
Interlock pilot loop input	IL_IN	19	Brown/Pink
Contactor K1	K1+	20	White
	K1-	21	Blue
Contactor K2	K2+	22	White
	K2-	23	Blue
Contactor K3	K3+	24	White
	K3-	25	Blue
Contactor K4	K4+	26	White
	K4-	27	Blue
Contactor K5	K5+	28	White
	K5-	29	Blue
Cooling valve output	CLO1 +	30	White
	GND	31	Black
Heating valve output	HTO2+	32	White
	GND	33	Black
Interlock pilot loop output	IL_OUT	34	Blue

Table 4. Main connector pinout.

RD-K358BMU User Guide, User Guide, Rev. 0, 04/2023

Wire side

Option A, Black

Connectors

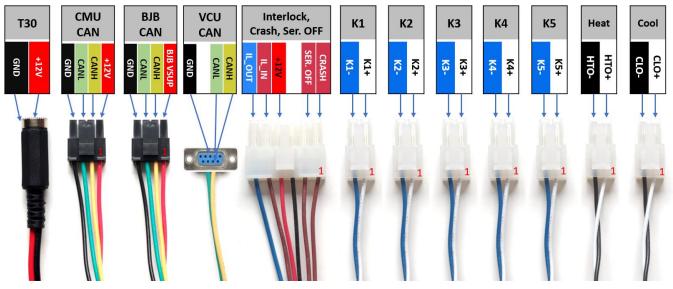


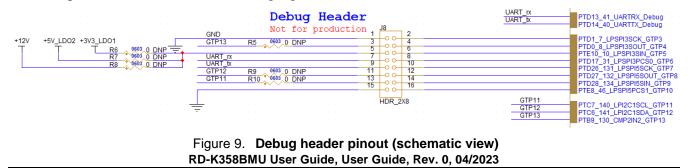
Figure 8. Wire harness connectors pinout

Table 5.	. Wire harness	connector F	PN s	pecification
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Function	Description	Wire side connector PN	Matching cnnector PN
Т30	Barrel connector 5.5*2.1mm	PE000032	
CMU CAN	Micro-Fit 3.0 Receptacle Housing, Single Row, 4 Circuits	436450400	436500413
BJB CAN	Micro-Fit 3.0 Receptacle Housing, Single Row, 4 Circuits	436450400	436500413
VCU CAN	DB9 DSUB Female 9Pin	61800925123	-
Interlock, Crash, Ser. Off	Mini-Fit Jr. Receptacle Housing, Single Row, 6 Circuits	39014060	39014063
K1	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656
K2	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656
К3	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656
K4	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656
K5	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656
Heating valve	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656
Cooling Valve	Mini-Fit Jr. Receptacle Housing, Single Row, 2 Circuits	39014020	469990656

7.2. GUI and debug header

J8 is the debug header and provids accessibility to several MCU pins with I2C, SPI, FlexIO or UART capabilities. This is intended for HW/SW debugging only and not intended for production HW version. Detailed pinout is shown in the following figure.

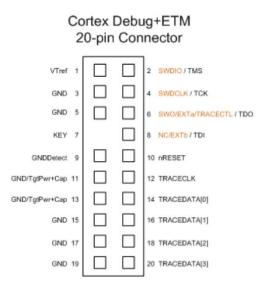


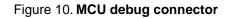
Board supports connection to a graphical user interface (GUI) over the JTAG debug probe or over the serial line. If the serial interface on J8 header is used, it is necessary to use a 3.3V USB to UART adapter to connect to computer. (adapter included in board package). Refer to paragraph 8.3 for more information regarding UART connection.

7.3. JTAG interface

Board is equipped by 20-pin 1.27MM ARM Cortex Debug + ETM connector (Samtec FTSH-110). This interface supports JTAG, SWD and tracing for on-board S32K358 MCU. When the Serial debug protocol is used, the TDO signal can be used for serial wire viewer output for trace capture. The connector also provides a 4-bit wide trace port for capturing of trace that require a higher trace bandwidth (e.g., when ETM trace is enabled).

Reference designator for this connector is J6. Pinout is shown in the following figure.





7.4. Pressure sensor BDM connector

The programing interface for intelligent pressure sensor is available at connector J7. Refer to pressure sensor datasheet for more information about connection and programming of the pressure sensor.

8. Communication Interfaces

8.1. ETPL ports

This reference design board may use either CAN or electrical transport protocol link (ETPL) communication between BJB, CMU and BMU. For use cases with ETPL, the board contains four isolated TPL ports available at connectors J2 (TPL A), J3 (TPL B), J4 (TPL C) and J5 (TPL D). Protocol supporting up to 62 nodes per TPL chain. Transmitting data though these ports can be done through battery gateway MC33665A. Board support either single or dual SPI mode.

Dual SPI mode is the default mode for this board. Dual SPI mode can be used to have independent data flows for requests and responses. In this setup, requests to MC33665A are feed through request port and responses from the MC33665A are pushed via the response SPI master to the MCU.

In Single SPI mode both MC33665A SPIs are connected to a single MCU SPI, reducing the number of MCU resources used. The MCU works as single master for the SPI communication with MC33665A. Response data is transferred in parallel to request data. To enable this mode R414, R416 and R417 must be populated on the PCB.

For more details about single and dual SPI modes, refer to the MC33665A datasheet.

Battery gateway Vdd is supplied even when the BMU is in stand-by mode and MC33665A active high wake-up output is connected to SBC wake2. This ensures BMU unit can wake up when TPL wake up frame is received.

TPL ports connection and peripheral chip select assignment is showed in Figure 11. The following table summarizes pinout between battery gateway and MCU.

Table o Battery gateway pinout assignment					
Port	Signal	SPI	MCU port		
se	SCLK_RSP		PTB14		
Response port	SDAT_RSP	LPSPI1 PCS3	PTB15		
Re	CSN_RSP	1055	PTB17		
4	SDAT_REQ		PTB27		
Request port	SCLK_REQ	LPSPI2	PTC15		
seque	CSN_REQ	PCS0	PTB25		
1	SIN_RSP (for single SPI mode only)		PTB28		

Table 6 Battery	v gateway	ninout	assignment
	y galoway	pillout	assignment

Communication Interfaces

SPI 1 PTB14_114_LPSP115CK_665_RSP PTB15_113_LPSP11SIN_665_RSP PTB17_110_LPSP11PCS3_665_RSP	SCLK RSP SDAT_RSP CSN_RSP	TPL_PHY SCLK_RSP SDAT_RSP_TXD CSN_RSP TPLORDTXN	TPL	Interface A 1 2 1 2 1 0 CON_1X2 J2
PTB16_112_LPSPI1SOUT_665_RSP	TP3	TPL1RDTXP	TPL	Interface B
PTB27_75_LPSPI2SOUT_665_REQ PTC15_68_LPSPI2SCK_665_REQ PTB25_72_LPSPI2PCS0_665_REQ	SDAT_REQ SCLK_REQ CSN_REQ	TPL1RDTXN SDAT_REQ_RXD SCLK_REQ CSN_REQ		² ^{CON_1X2} J3 Interface C
PTB28_76_LPSPI2SIN_665_RSP	SIN_RSP	SIN_RSP TPL2RDTXP TPL2RDTXN		1 2 2
PTD23_122_EIRQ28_665_GPI00 PTD22_118_EIRQ27_665_GPI01 PTA8_172_EIRQ16_665_GPI02 PTA9_171_EIRQ17_665_GPI03	GPI00 GPI01 GPI02 GPI03 GPI04	GPIO0 GPIO1 GPIO2 GPIO3	TPL	Interface D
PTC28_96_12C1SCL_665_6PIO4 PTC29_99_12C1SDA_665_6PIO5 PTD24_125_EIRQ29_665_6PIO6 PTB11_126_EIRQ25_665_6PIO7	GPI05 GPI06 GPI07	GPIO4 TPL3RDTXP GPIO5 TPL3RDTXN GPIO6 GPIO7 TPL_VIO_IN	+3V3_VIO +5V_LDO2	2 1 2 2 CON_1X2 J5
PTD4_119_665_RST PTE0_163_665_AUTOWAKE	QPHY_RST AUTOWAKE	QPHY_RESET TPL_GND_IN AUTO_WAKE TPL WAKE	TPL_WAKE	· · · · · · · · · · · · · · · · · · ·
		15 TPL_QPHY	GŇD	

Figure 11. TPL ports connections

TPL ports are intended to use for communication with CMU and BJB units. These ports can be used as four separated daisy chains ports or daisy chains with loopback mode. Loopback mode provides additional safety, ensuring full functionality even if the daisy chain wire is interrupted at one point.

Location	Describtion	PN.
PCB side	Micro-Fit 3.0 Right-Angle Header, 3.00mm Pitch, Single Row, 2 Circuits, with Solder Tab, Gold, Glow-Wire Capable, Black,	436500214
Wire side	Micro-Fit 3.0 Receptacle Housing, Single Row, 2 Circuits, UL 94V-0, Low-Halogen, Black	436450200

Table 7. TPL port connector specification

8.2. CAN buses

There are three CAN-FD capable ports with on-board transceiver available on the BMU board. All CAN interfaces are connected to main connector J1.

8.2.1. VCU CAN

Vehicle control unit CAN (VCU CAN) is the main CAN interface equipped with high-speed TJA1145ATK/FD partial networking transceiver. This transceiver supports CAN partial networking by means of a selective wake-up function. The transceiver inhibit pin is connected to the SBC wake1 signal, which wakes up the system when the wake-up command is received on the VCU CAN port. To configure VCU CAN transceiver, use LPSPI5 PCS2.

8.2.2. CMU CAN bus

For communication with CAN-based CMUs, the board is equipped with high-speed CAN transceiver TJA1443ATK. This transceiver is supplied in standby mode and can be used as a BMU wake up source, connected to SBC wake2 input. During run mode, the transceiver can be put into standby mode to save power. Stand-by pin is active low, therefore, to activate stand-by for CMU CAN, clear pin PTA7.

8.2.3. BJB CAN bus

For communication with CAN-based BJB, the board is equipped with high-speed CAN transceiver TJA1057GTK/3Z. This transceiver is not supplied in standby mode, so it cannot wake up the BMU. In run mode the transceiver can be switched to silent mode to save power. To activate stand-by for BJB CAN set pin PTC3.

8.3. UART for GUI

Serial UART interface is available at J8 Debug header. Note this is directly connected to MCU without any transceiver or protection circuit. To communicate with PC the TTL to USB converter should be used (e.g. FTDI TTL-232R-3V3). Port is intended for communication with graphical user interface (GUI) or to use for terminal output. The following figure shows correct connection of USB to UART adapter and Table 8 shows connection of signals.

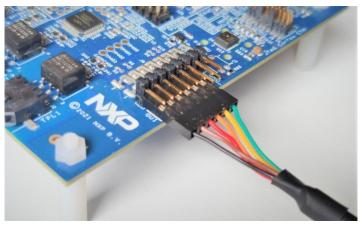


Figure 12. Connection of USB to UART converter for GUI

· • • • • • • • • • • • • • • • • • • •								
Signal	Pin	MCU port						
GND	J8.1	-						
UART - Rx	J8.7	PTD13						
UART - Tx	J8.9	PTD14						

Table	8.	Serial	interface	pinout

8.4. On-board SPI

There are 11 serial peripheral interface (SPI) nodes at this BMU board. Assignment of peripheral chip select (PCS) and SPI instances is as shown in the following table.

Auxiliary Circuits

Node name	IC reference	SPI Instance	Peripheral chip selects	Max CLK speed [MHz]
SBC (FS2613D)	U43	LPSPI0	PCS0	10
TPL Response	U400	LPSPI1	PCS3	10
TPL Request	U400	LPSPI2	PCS0	10
Load drivers	U40	LPSPI3	PCS1	1
HB2000 Contactor drivers	U301, U303, U352, U354	LPSPI4	PCS0,1,2,3	10
Real time clock (RTC)	U42	LPSPI5	PCS0	5
Pressure sensor (NBP8)	U12	LPSPI5	PCS3	10
VCU CAN TJA1145A	U20	LPSPI5	PCS2	2.5

Table 9 On board SPI nodes

9. Auxiliary Circuits

9.1. Contactor drivers

The BMU board allows the user to control four contactors (two for DC link and two for the charger circuit) with maximal coil pick-up current up to 4A for 1sec then 0.8A holding current per channel. The BMU also supports a DC bus capacitor precharge contactor with a maximum coil current of 1 A. The DC link and charger contactor circuitry implements an H-bridge driver to be able to control the two coil terminals separately, support economizer PWM with active current recirculation, fast turn off, and high side current monitoring. Each H-bridge driver is SPI-configurable, receives a 20 kHz PWM from the MCU's PWM generator, and sends the coil current feedback signal back to the MCU's ADC. Such a configuration enables closed-loop current control, ensuring an effective PWM economizer function for the contactors.

Contactors that require external economizer circuits typically have a limited amount of time to support a full 12 V supply, otherwise the coil may be damaged. To prevent overheating the coil, the duty cycle should be lowered to within few hundred milliseconds according to contactor datasheet (e.g. 200 ms). Always make sure that the coil current is maintained at the hold current recommended by contactor manufacturer after the predefined duration of the pick-up pulse. This ensures reliable contactor closed state and optimal efficiency even if the input voltage is changed or the coil resistance varies with temperature.

The contactors circuits also support fast drop off (FDO) functionality, which ensures fast coil current decay to not to limit the contactor mechanical performance when the contactor is opening. This help to minimize contactor wearing and prevent from contacts welding during contactor operation.

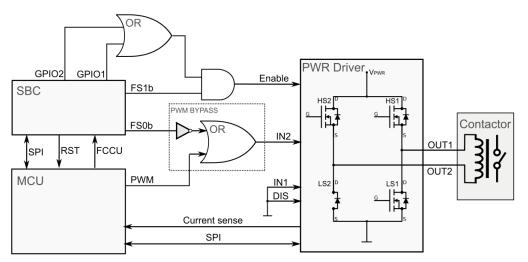


Figure 13. DC-link contactor driver circuit block diagram (single instance)

Since there are different requirements for DC link and charger contactors there are differences in the circuits and their control. The main difference is due to the fail operational function which is part of the DC link contactor drivers only. DC link contactor circuitry includes a fail operational circuit as shown in the figure above and its control is described in sections Contactors fail operational circuit and DC-link

contactors close procedure. The charger contactors circuit is shown in the following figure and its control is described in the section Charger contactors close procedure and Charger contactor open procedure.

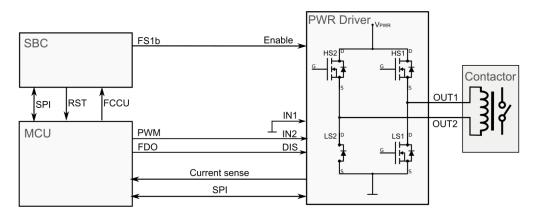


Figure 14. Charger contactor driver circuit block diagram (single instance)

It is intended that each contactor driver will operate in three current conduction modes, depending on the driver inputs. All modes are illustrated in the figure below. Starting from the left in the figure below, the first mode is while the PWM input in high state. In this mode, contactor coil is connected to T30 voltage through, HS2 and LS1 switches which means that the coil current is rising. After the PWM goes to OFF state (middle picture), the LS1 switch is OFF and HS1 is ON, which leads to active current recirculation. The contactor coil current recirculates through HS2 and HS1. The contactor coil current is decreasing slowly, but due to low R_{DSON} , power losses are minimized in comparison to the conventional freewheeling approach. In case the contactor is requested to open, (see right picture) to decrease contactor coil current as soon as possible. During this mode coil current is discharged back to power supply through the HS1 and LS2 body diodes, causing the contactor to open quickly, known as fast drop out (FDO).

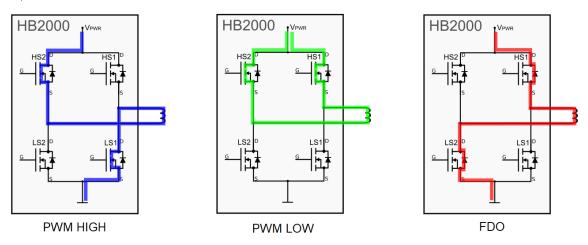


Figure 15. Contactor drivers current conduction modes

To ensure normal operation of the contactors, the SBC must be in normal mode with proper watchdog refreshes. To enter normal mode, see Leave debug mode. Both safety outputs FS0B and FS1B must be

released, so they must be in high state. Normal operation of the contactors in SBC debug mode or without releasing the safety outputs is not possible.

9.1.1. Contactors fail operational circuit

The fail operational circuit ensures DC link contactors state can be maintained even in case of software error, MCU reset or temporary unavailability of the MCU for a short period of time, shorter than the minimum fault detection time interval (FDTI) identified by the battery management system (BMS) safety analysis. The battery cannot be kept connected to a vehicle's bus for longer than the FDTI if the MCU is not available.

In the event of a MCU of software fault, the fault status is detected over the SPI communication between the MCU and the SBC or indicated on the pins of the fault control and correction unit (FCCU). Upon detection of the fault, the SBC asserts the FS0b pin to ground, causing PWM economizer function to be bypassed by an OR gate and the contactors to be driven with duty cycle of 100% during the recovery period. From this moment, the SBC is taking full control over the contactors driving circuit to keep them in an unchanged state and none of the MCU pins (including PWM) can affect the contactors behavior. After asserting the FS0B, the SBC can trigger a reset on the MCU or the MCU can self-trigger a power on reset (POR) to start the recovery phase.

Upon successful recovery within the predefined timeout (e.g. 1 second), the MCU requests again for the FS0b to be released to take over the contactors control including the economizer functionality, without the need to open the contactors and to disconnect the battery from the DC Link bus.

Upon unsuccessful recovery within the predefined timeout (normally equal to the shortest FDTI linked to the battery management system), the SBC asserts the FS1b safety output, and leads the system to a safe state by disabling the contactors driving circuits and opening the DC link contactors to disconnect the battery from the DC Link bus.

The system solution uses the SBC GPIO outputs, which act as a memory to preserve the contactor state during the MCU recovery period. The system uses two GPIO outputs together with an OR gate to prevent single point of failure (SPF) at the SBC GPIO output. In this configuration, the contactors' driving circuit enable pin is driven by both GPIO1 and GPIO2 connected through an OR gate. The redundant GPIO output configuration in the SBC improves the single point fault metric (SPFM) in the safety analysis and improves the reliability on the circuit memory.

9.1.2. Contactor coil current measurement diagnostic

For safety reasons, the contactor coil current measurement is done by two ADCs as primary and secondary measurement. To improve diagnostic coverage, the current sense resistor is divided into two resistors (R332 and R301 for K1), where one ADC measures the midpoint of the resistor divider, while the second ADC measures the total voltage drop across both resistors. The secondary measurement should always indicate half the value of the primary measurement. If it does not, it may indicate a drift in the current sensing resistor, so the software can take appropriate action. The current measurement circuit is shown in the following figure:

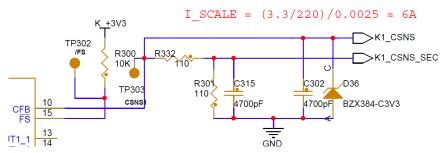


Figure 16. Contactor coil current measurement and diagnostic

The connection of the driver current feedback signals to the appropriate MCU pins is described in the following table.

Contactor	ADC channel	Port
K1 DC-link+ (primary ADC)	ADC2_P3	PTE21
K1 DC-link+ (secondary ADC)	ADC1_P5	PTE2
K2 Charger+ (primary ADC)	ADC2_P7	PTE25
K2 Charger+ (secondary ADC)	ADC1_P4	PTA14
K3 DC-link - (primary ADC)	ADC2_P5	PTE23
K3 DC-link- (secondary ADC)	ADC1_P3	PTE1
K4 Charger- (primary ADC)	ADC2_P4	PTE22
K4 Charger- (secondary ADC)	ADC1_P0	PTA12

 Table 10 Contactor current sense channel assignment

9.1.3. HB2000 recommended settings

The MC33HB2000 is a monolithic H-Bridge power IC, enhanced with SPI configurability and diagnostic capabilities. To ensure required functionality required for RD-K358BMU, specific register settings must be applied. Special attention should paid to slew rate settings as HB2000 have eight selectable slew rates from 0.25 V/ μ s to over 16 V/ μ s for EMI and thermal performance optimization. Operation of HB2000 with default register settings will impact the board thermal behavior and may cause an overtemperature shutdown.

HB2000 settings depend on contactor types, required EMI performance and other factors. The following table shows the settings which has been used during board validation. In this configuration, the device is in H-bridge mode with fast slew rate.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	CL	тм	AL	ILM1	ILM0	SR2	SR1	SR0	EN	MODE	Input	VIN2	VIN1
Write	1	1	1	0	1	1	0	1	0	0	1	1	1	0	0	0

Table 11 HB2000 "Configuration and Control" register example settings

9.1.4. DC link contactors closing procedure

DC-link contactor control circuits include a fail operation circuit and an economizer circuit. Therefore special attention must be paid to ensure proper control of the driver circuit. Note that in default state, the HB2000 drivers are disabled and no communication via the SPI interface is possible with these devices.

To enable communication and to close dc link contactors the following sequence must be followed:

- 1. Make sure the SBC is in normal mode.
- 2. Set the PWM to 0% duty cycle.
- 3. Make sure U40 OUT #3 is active and provides power supply for contactor drivers.
- 4. Release the SBC FS1B and FS0B outputs.
- 5. Set the SBC GPIO1 and GPIO2 pins high, to enable the contactor drivers.
- 6. Send the HB2000 configuration through SPI and check device status.
- 7. Set PWM to 100% duty cycle.
- 8. Wait until the pick-up pulse is long enough to meet the contactor manufacturer's requirements.
- 9. Start close loop current control, to regulate current to hold the current setpoint.

9.1.5. DC link contactor opening procedure

To open DC link contactors the following sequence must be followed:

- 1. Clear the SBC GPIO1 and GPIO2 pins to disable contactor drivers.
- 2. Set PWM duty cycle to 0%.

9.1.6. Charger contactors closing procedure

The charger contactors control circuits do not include fail operation circuits, therefore the procedure for closing these contactors is slightly different than for the DC link contactors.

To close the charger contactors, the following sequence must be followed:

- 1. Make sure the SBC is in normal mode.
- 2. Set PWM to 0% duty cycle.
- 3. Make sure U40 OUT #3 is active and provides power supply for contactor drivers.
- 4. Release the SBC FS1B and FS0B outputs.
- 5. Clear K2_FDO and K4_FDO signals to enable the contactor drivers.
- 6. Send the HB2000 configuration through SPI and check device status.
- 7. Set PWM to 100% duty cycle.
- 8. Wait until the pick-up pulse is long enough to meet the contactor manufacturer's requirements.
- 9. Start close loop current control, to regulate current to hold the current setpoint.

9.1.7. Charger contactor opening procedure

To open the charger contactors, the following sequence must be followed:

- 1. Set K2_FDO and K4_FDO signals high to disable the contactor drivers.
- 2. Set PWM duty cycle to 0%.

9.2. Load drivers

The board is equipped with five outputs to drive 12 V loads. These outputs are protected against short circuit and reverse polarity. All outputs comes from the load switch (U40). Outputs are controlled through SPI bus unless, U40 is switched to fail mode (e.g. SPI malfunction) where outputs are switched to their predefined state which can be found in the table below.

The output current can be measured through MCU port PTE6 ADC1P6. To measure the current of respective output, the internal multiplexer of U40 must be properly configured via SPI.

The list of outputs and their current capacity are summarized in the following table.

n.	Name	Description	Max. current rating [A]	Fail state
1.	OUT1	System cooling solenoid valve	1	OFF
2.	OUT2	System heating solenoid valve	1	OFF
3.	OUT3	Contactor driver power supply	2 (8A for 1sec)	ON
4.	OUT4	BJB power supply	0.5	ON
5.	OUT5	Pre-charge contactor	1	OFF

Table 12. Load switch outputs

9.3. High voltage interlock pilot loop

The high voltage interlock loop (HVIL) is a loop which monitors disconnection or tampering of all high voltage components (e.g. on-board charger, power inverter, connectors, etc..). This BMU board is equipped with PWM-based interlock which can detect loop interruption, loop short to ground or short to T30. The interlock consists of two parts: transmitter and receiver. The impedance of the correctly operating loop between transmitter and receiver shall be below 500 ohms.

The transmitter provides a 12 V PWM signal with a frequency of 33 Hz supplied by an internal PWM modulator of the S32K358 MCU. The signal is protected against short to T30 and short to ground by a current limiting circuit. The loop current is limited to 20 mA.

The receiver scales signal amplitude and feed PWM signal into S32K358 input capture module. The MCU can check if the period, frequency and phase of the signal from the interlock loop are correct. Receiving a signal with the same period, frequency and phase, mean the loop is closed and operates correctly. Measuring a constant high level indicate short to T30, and measuring constant low level indicates short to ground or a high impedance of the interlock loop.

9.4. AMUX analog value monitoring.

By using the SBC internal analog multiplexer, the MCU have access to the SBC internal and external voltage and temperature values. The voltage channels delivered to the AMUX pin can be selected using SPI. The AMUX output is connected to MCU ADC1P1 PTA13. The analog multiplexer can be used by the system to monitor various parameters from the FS26 and the application.

The typical use case is T30 voltage measurement. The channel selection list and divider ratios can be found in FS26 datasheet.

9.5. Crash and Service disconnect inputs

The crash input is an input dedicated for connecting a 12 V signal indicating vehicle crash, coming from an external ECU. This signal is connected to the main connector (J1) on pin 15. This signal is active low and is equipped with diagnostic. To read this input, the MCU pin PTA1 must be set high, otherwise the input will always be read as low. The crash signal is available on the MCU pin PTB12.

The service disconnect is an input dedicated for connecting a 12 V signal indicating the vehicle is being repaired and therefore the battery must be disconnected. This signal is connected to the main connector (J1) on pin 16. This signal is active low, and it is equipped with diagnostic. To read this input, the MCU pin PTD6 must be set high, otherwise the input will always be read as low. The signal is available on the MCU pin PTD5.

10. Board Accessories

10.1. Included accessories

The BMU board comes with cable harness, one ETPL cable, a 12 V/4 A power supply and a USB to serial converter (see the BMU package content in the following figure). Other cables or accessories are not part of the BMU board package. The list of recommended accessories can be found in Table 13.

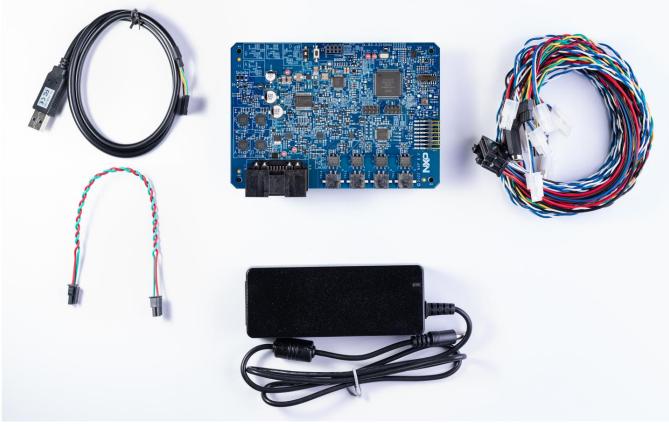


Figure 17. BMU board package content

10.2. Recommended accessories

To make full use of the board's features, additional accessories are needed. The following figure shows a typical system interconnection and Table 13 provides list of recommended accessories for the RD-K358BMU board.

Board Accessories

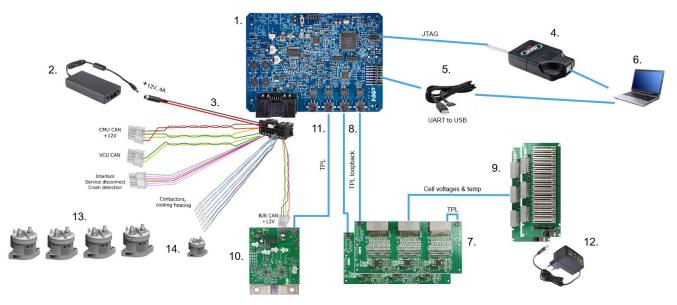


Figure 18. Typical HVBMS system setup

n.	Name	QTY	Туре	Optional /	Purpose
				Mandatory	
1	BMU board (included)	1		Mandatory	
2	Power supply (included)	1	12V DC, 4A	Mandatory	BMU power supply
3	Main cable harness (included)	1	Custom cable included in BMU package	Mandatory	
4	Debugger	1	PEmicro MULTILINK or Lauterbach PowerDebug	Mandatory	Flashing firmware on S32K358 MCU
5	USB to UART adapter	1	e.g. TTL-232R-3V3	Optional	Communication to GUI
6	PC	1	PC with 3 USB ports	Mandatory	
7	Cell Monitoring Unit (CMU)	1 or more	RD33774CNT3EVB	Mandatory	Li-ion cell monitoring based on MC33774
8	CMU ETPL twisted pair cable	1	Included in CMU package	Mandatory	Communication with the CMU unit
9	18-Cell Battery Pack Emulator	1	BATT-18CEMULATOR	Optional	Emulate a multi-cell battery pack
10	Battery Junction Box (BJB)	1	RD772BJBTPL8EVB	Optional	Current, voltage and isolation measurement
11	BJB ETPL twisted pair cable	1	Included in the BJB package	Optional	Communication with the BJB unit
12	Emulator power supply	1	12V	Optional	BATT-14CEMULATOR supply
13	Battery contactors	4	e.g.: EVC 500-A1ANAM	Optional	Battery and Charging terminal control
14	Pre-charge contactor	1	e.g.: EVC 135-5ANGA	Optional	Inverter capacitor pre-charge.

Table 13. Recommended accessories

11. Tips and Recommendations

11.1. Recommendation for capacitors

It is recommended to use soft termination or fail open capacitor in critical functions to improve board reliability (e.g. C312).

11.2. Vmonext usage

Vmonext is the signal for internal/external voltage monitoring. In the current schematic, this signal monitors TRK2 output to increase the diagnostic coverage. However, monitoring this signal is not required by the safety analysis. Therefore, customers can use the Vmonext signal for other purposes as required by the final application.

If the signal is not being used, make sure this functionality is disabled in FS2613 OTP configuration, or make sure Vmontext is supplied with a 0.8 V (e.g. use voltage divider from Vcore). A wrong Vmonext voltage will cause FS2613 to assert MCU reset low, and the system will not be able to start .

11.3. JTAG adapters

The BMU board is equipped with a small 20-pin 1.27MM ARM Cortex Debug + ETM connector (Samtec FTSH-110) (see section: 7.3 JTAG interface, for details). Various debug probes come with different connectors and adapter set, therefore it is important to check whether your debug probe is compatible with the BMU JTAG interface. If this is not the case, appropriate adapter for your probe is necessary. There are several adapters available in the market. Select appropriate adapters according your debug probe type. Here are some examples:

- A) Lauterbach LA-3770 Converter Arm-20 to MIPI-10/20/34
- B) JTAG_SWD_Adapter Cyclone MAX Adapter for ARM processors
- C) 8.06.00 J-LINK 19PIN CMADAPTER

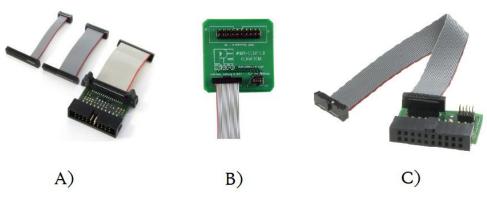
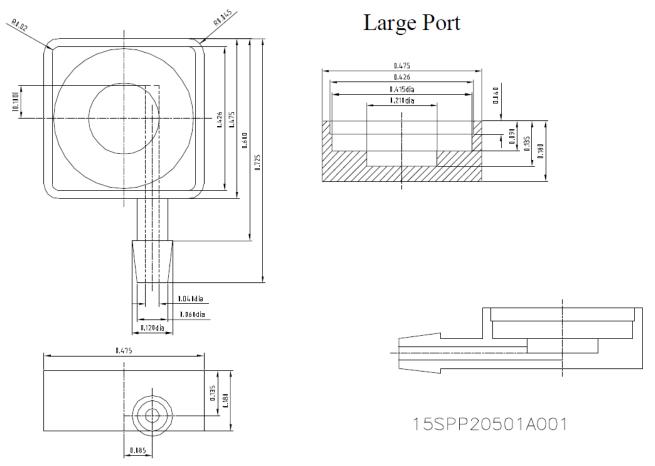
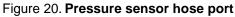


Figure 19. JTAG adapters

11.4. Pressure sensor hose port

RD-K358BMU is equipped with a pressure sensor for thermal runaway events detection. In the default configuration, the sensor is populated directly on the PCB without possibility of connecting it through a hose. This configuration is only suitable for systems in which the BMU is located in a sealed housing together with battery cells. If the BMU is located outside of the sealed housing, it is necessary to connect this sensor via a hose. In this case pressure sensor must be equipped with a plastic port that allows hose connection. There are several hose ports available in the market, an example is shown in the picture below.





MCU Pinout

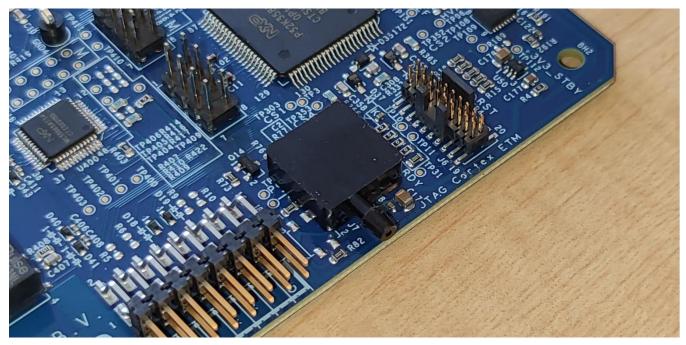


Figure 21. Hose port mounted on PCB

12. MCU Pinout

The following table shows S32K358 MAXQFP172 pinout and signal distribution for the BMU.

S32K344_172mqfp	Pin Name	Functionality Required	Purpose in BMS ref design	Pin Type
1	PTA18	GPIO PTA18	RTC TS1	OUT
2	PTA19			NC
3	PTA20	TRGMUX_IN14	PWM IL IN	IN/PWM
4	PTE16	FCCU_ERR_IN1	FCCU_IN2	OUT/FCCU
5	PTE15	FCCU_ERR_INO	FCCU_IN1	OUT/FCCU
6	PTA21	GPIO_PTA21	LED_RED	OUT
7	PTD1	LPSPI3 SCK	GTP3	BI
8	PTD0	LPSPI3 SOUT	GTP4	BI
9	PTE11			NC
10	PTE10	LPSPI3 SIN	GTP5	BI
10	PTE13			NC
12	PTE5			NC
				SPI
13	PTE4	LPSPI0_PCS0	LPSPIOPCS0_SBC	
14	PTA24	GPIO_PTA24	GTP2	DBG
15	PTA25	OSC32K_EXTAL	OSC32K	CLK
16	VREFH	PWR		PWR
17	VREFL	PWR		PWR
18	VDD_HV_A	PWR		PWR
19	V25	PWR		PWR
20	V15	PWR		PWR
21	V11	PWR		PWR
22	VSS	PWR		PWR
23	EXTAL	EXTAL		CLK
24	VSS	VSS		PWR
25	XTAL	XTAL		CLK
26	VSS_DCDC			PWR
27	PMOS_CTRL			PWR
28	VDD_DCDC			PWR
29	PTE12	GPIO_PTE12 + IRQ11	SBC INTB	IN
30	PTA28	eMIOS_1_CH[11]_H	K3_PWM_FB	IN/PWM
31	PTD17	LPSPI3_PCS0	GTP6	BI
32	PTA29	GPIO PTA29	FS1B	IN
33	PTA30	LPSPIO SOUT	LPSPIOSOUT_SBC	SPI
34	PTD16	LPSPIO_SIN	LPSPI0_SIN_SBC	SPI
35	PTD15	LPSPI0_SCK	LPSPI0_SCK_SBC	SPI
36	V15	PWR		PWR
37	VSS	PWR		PWR
38	VDD_HV_B	PWR		PWR
39	PTA31	GPIO_PTA31	GTP2	BI
40	PTA31 PTD14	LPUART1_TX	FMSTR_UART_TX	UART
40	PTD14 PTD13	LPUART1_TX LPUART1_RX	FMSTR_UART_RX	UART
41 42	PTD13 PTB18	eMIOS_1_CH[15]_H	K1_PWM_FB	IN/PWM
43	PTB19			NC
44	PTB20		500	NC
45	PTB21	GPIO_PTB21 + IRQ	FSOB	IN
46	PTE8	LPSPI5_PCS1	GTP10	BI
47	PTB5	TP8 CLK_RUN	TP8	CLK
48	PTB4			NC
49	PTC3	GPIO_PTC3	BJB_CAN_STB	OUT
50	PTC2			NC
51	PTD7			NC
52	PTD6	GPIO_PTD6	SEROFF_DIAG	OUT
53	PTD5	eMIOS_0_ch2	SEROFF_IN	IN
54	PTD12			NC

S32K344_172mqfp	Pin Name	Functionality Required	Purpose in BMS ref design	Pin Type
55	PTD11			NC
56	PTD10			NC
57	VDD_HV_B	PWR		PWR
58	VSS	PWR		PWR
59	V11	PWR		PWR
60	V15	PWR		PWR
61	PTC1			NC
62	PTC0	GPIO_PTC0 + IRQ	RTC_INTA	IN
63	PTD9			NC
64	PTD8			NC
65	PTC17	CAN2_TX	BJB_CAN	CAN
66	PTC16	CAN2_RX	BJB_CAN	CAN
67	PTB22			NC
68	PTC15	LPSPI2_SCK	LPSPI2SCK_MC33665_REQ	SPI
69	PTB23			ENET
70	PTB24			ENET
71	PTC14			ENET
72	PTB25	LPSPI2 PCS0	LPSPI2PCS0 MC33665 REQ	SPI
73	PTB26			ENET
74	PTB3	GPIO_PTB3	MCU_K_EN	OUT
75	PTB27	LPSPI2_SOUT	MC33665_REQ_SOUT	SPI
76	PTB28	LPSPI2_SIN	MC33665_RSP_SIN	SPI
77	VDD_HV_B	PWR		PWR
78	VSS	PWR		PWR
79	V15	PWR		PWR
80	PTB29	eMIOS_2_ch11	K1 PWM	OUT/PWM
81	PTC13	GPIO PTC13	K2 FDO	OUT
82	PTC18	eMIOS 2 ch12	K2 PWM	OUT/PWM
83	PTC12	GPIO_PTC12	K4 FDO	OUT
84	PTC19	eMIOS_2_ch13	K3 PWM	OUT/PWM
85	PTC20	eMIOS_2_ch14	K4 PWM	OUT/PWM
86	PTC21	GPIO_PTC21	LED GRN	OUT
87	PTC23			NC
88	PTC24			NC
89	PTC25	LPSPI4_PCS1	LPSPI4PCS1 K3	SPI
90	PTC11	LPSPI4 SOUT	LPSPI4SOUT_K	SPI
91	PTC26	LPSPI4 SIN	LPSPI4SIN K	SPI
92	PTC10	LPSPI4 PCS0	LPSPI4PCS0_K1	SPI
93	PTC27	LPSPI4_SCK	LPSPI4SCK K	SPI
94	PTB1	CANO TX	CANOTX_VCUCAN	CAN
95	PTBO	CANO RX	CANORX VCUCAN	CAN
96	PTC28	12C1_SCL	MC33665_GPIO4	DBG
97	PTC9			NC
98	PTC8			NC
99	PTC29	I2C1 SDA	MC33665 GPI05	DBG
100	PTA7	GPIO PTA6	CMUCAN STB	OUT
100	PTC30	CAN4_TX	CMU CAN	CAN
101	PTA6	LPSPI3 PCS1	LPSPI3PCS1 LOADSW	SPI
102	PTC31	CAN4 RX	CMU CAN	CAN
104	PTE7	LPSPI3_SCK	LPSPI3SCK LOADSW	SPI
105	V15	PWR		PWR
105	V11	PWR		PWR
107	VSS	PWR		PWR
108	VDD HV A	PWR		PWR
109	PTA17	LPSPI3 SOUT	LPSPI3SOUT LOADSW	SPI
110	PTB17	LPSPI1 PCS3	LPSPI1PCS3 MC33665 RSP	SPI
110	PTD20	LPSPI3 SIN	LPSPI3SIN LOADSW	SPI
112	PTB16	LPSPI1 SOUT	LPSPI1SOUT MC33665 RSP	SPI
112	PTB15	LPSPI1 SIN	LPSPI1SIN MC33665 RSP	SPI
113	PTB14	LPSPI1 SCK	LPSPI1SCK MC33665 RSP	SPI
T	PTD21	GPIO_PTD21	LOADSW RST	OUT

S32K344_172mqfp	Pin Name	Functionality Required	Purpose in BMS ref design	Pin Type
116	PTB13	eMIOS_0_ch1	PWM IL OUT	OUT/PWM
117	PTB12	GPIO PTB12 EIRQ	CRASH IN	IN
118	PTD22	GPIO_PTD22_EIRQ27	MC33665 GPIO1	BI
119	PTD4	GPIO_PTD4	MC33665 RST	OUT
120	PTD3	NMI	NMI	IN
120	PTD2	LPSPI5 SOUT	LPSPI5SOUT VCU RTC PS	SPI
121	PTD23	GPIO PTD23 EIRQ28	MC33665 GPIO0	BI
122	PTA3	LPSPI5_SCK	LPSPI5SCK VCU RTC PS	SPI
123	PTA3 PTA2	LPSPI5_SIN	LPSPISSCK_VCU_RTC_PS	SPI
124	PTA2 PTD24			BI
		GPIO_PTD24_EIRQ29	MC33665_GPI06	
126	PTB11	GPIO_PTB11_EIRQ25	MC33665_GPIO7	BI
127	VSS	PWR		PWR
128	VDD_HV_A	PWR		PWR
129	PTB10	GPIO_PTB10	PS_READY	IN
130	PTB9	CMP2_IN2	GTP13	BI
131	PTD26	LPSPI5_SCK	GTP7	BI
132	PTD27	LPSPI5_SOUT	GTP8	BI
133	PTB8			NC
134	PTD28	LPSPI5_SIN	GTP9	BI
135	PTA1	GPIO_PTA1	CRASH_IN_DIAG	OUT
136	PTD29	LPSPI5 PCS2	LPSPI5PCS2 VCU	SPI
137	PTA0	LPSPI4 PCS2	LPSPI4PCS2 K2	SPI
138	PTD30	LPSPI5 PCS3	LPSPI5PCS3 PS	SPI
139	PTD31			NC
140	PTC7	LPI2C1_SCL	GTP11	BI
140	PTC6	LPI2C1 SDA	GTP12	BI
141	PTE17		61112	NC
142	PTA16	LPSPI4 PCS3	LPSPI4PCS3 K4	SPI
143	PTE18	LP3P14_PC35	LF3FI4FC35_K4	NC
145	PTA15	LPSPI5_PCS0	LPSPI5PCS0_RTC	SPI
146	PTE6	ADC1_P6	LOADSW_CSNS	IN/ANA
147	PTE2	ADC1_P5	K1_CSNS_SEC	IN/ANA
148	V15	PWR		PWR
149	V11	PWR		PWR
150	VSS	PWR		PWR
151	VDD_HV_A	PWR		PWR
152	PTA14	ADC1_P4	K2_CSNS_SEC	IN/ANA
153	PTE21	ADC2_P3	K1_CSNS	IN/ANA
154	PTE22	ADC2_P4	K4_CSNS	IN/ANA
155	PTA13	ADC1_P1	SBC_AMUX_IN	IN/ANA
156	PTE23	ADC2_P5	K3_CSNS	IN/ANA
157	PTE24			NC
158	PTE25	ADC2_P7	K2_CSNS	IN/ANA
159	PTA12	ADC1_P0	K4_CSNS_SEC	IN/ANA
160	PTA11			NC
161	PTA10	JTAG TDO/TRACEnoETM SWO	JTAG / Trace	DBG
162	PTE1	ADC1 P3	K3 CSNS SEC	IN/ANA
163	PTEO	GPIO PTEO	MC33665 AUTOWAKE	DBG
164	PTE26			NC
164	PTC5		JTAG	DBG
		JTAG_TDI		
166	PTC4	JTAG_TCK / SWD_CLK	JTAG/SWD	DBG
167	PTA5	Reset_b	Reset	BI
168	VSS	PWR		PWR
169	VDD_HV_A	PWR		PWR
170	PTA4	JTAG_TMS / SWD_DIO	JTAG/SWD	DBG
171	PTA9	GPIO PTA9 IRQ17	MC33665_GPIO3	DBG
172	PTA8	GPIO PTA8 IRQ16	MC33665_GPIO2	DBG

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