MPC567XADAT416

Demonstration Module Hardware User Guide

Applies to Freescale
MPC5674F & MPC5676R
Microcontrollers

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CONTENTS

FIGURES

REVISION

Date	Rev	Comments
November 3, 2008	A	Initial Release – Applies to Rev A only.
October 12, 2009	B	Updated for Rev B. Updated page and figure numbers
January 22, 2010	C	Corrected XTAL frequency, updated 1st page footer
March 16, 2011	D	Updated to include support for MPC5676R (Cobra) MCU. Added device orientation diagram. Updated development port description
March 17, 2011	E	Corrected NEXUS Port connector pin-out. Updated MDO Option Header section.

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the MPC5561EVB board:

   a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

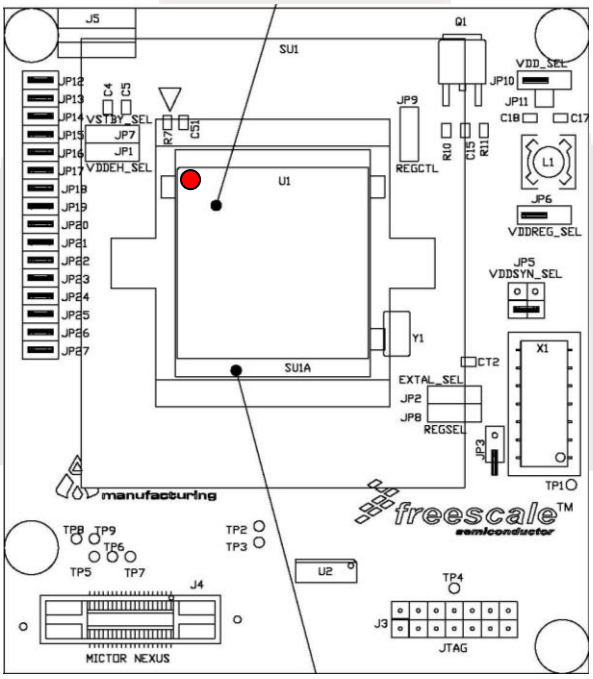
OVERVIEW

The MPC567XADAT416 (ADAT416) supports the MPC5674F and the MPC5676R microcontrollers in the 416BGA package. The ADAT416 is a daughter-card type module which is designed to mount directly to the MPC567XEVBMB (EVBMB) via 4, low-profile stack headers. An open-top, zero insertion force socket allows easy insertion and removal of the target device. This document details the hardware configuration for the ADAT416. Refer to the target device Reference Manual for details on use and configuration of the target device with the MPC567XADAT416 module

DEVICE ORIENTATION

The ADAT416 module applies an open-top socket to allow the target device to be installed and removed easily. However, the socket obscures the pin 1 marking showing device orientation. Although present, the pin 1 marking on the socket is not readily visible. The figure below illustrates the correct device orientation. The solid circle marks the target device pin 1 location.

Figure 1: Device Orientation



POWER SUPPLY

Primary power to the ADAT416 is provided through the stack headers. Alternate power input may be applied through the power input at location J5. Location J5 is designed to accept 3.5mm terminal block. This terminal block is not installed in the default configuration.

Alternate power input allows the ADAT416 to be used as a stand-alone development module.

The MPC5674 VDD input is generated on-board using either a linear pass transistor at Q1 or a switch-mode power supply regulator at Q2. Option header at JP9, REGCTL selects either the linear regulator or the switch-mode regulator.

CAUTION: Power to the EVBMB must be disconnected prior to installing the ADAT416. Damage to the ADAT416 and EVBMB may otherwise occur.

ANALOG Supplies

Analog voltage (+5VA) to the ADAT416 is provided from the EVBMB via the 4 board stack headers. This voltage is not generated on the ADAT416 module. The VRH_EN option header selects +5VA by default. A cut-trace enables this option by default and the jumper is not installed in default configurations.

Analog voltage, +5VA, is not available with the module powered as a stand-alone module.

OPTION JUMPERS

On the Rev A, ADAT416 board, only the JP3 option jumper is populated. The remaining option jumpers are configured for default operation by cut-traces between pin positions. The option jumper is not installed in default configuration.

VDDEH_SEL – JP1

The VDDEH_SEL option jumper selects the high-voltage input applied to the target MCU. All target MCU VDDEH inputs are supplied by this option jumper. This option jumper is configured for +5V operation in default configuration.

EXTAL_SEL– JP2

The EXTAL_SEL option jumper selects between the on-board, 40 MHz XTAL and the oscillator socket at X1 as timing input to the target MCU. This option jumper is configured for XTAL input in default configuration.

JP3

The JP3 option jumper applies +3.3V power to the OSC socket at X1.

VRH_EN– JP4

The VRH_EN option jumper applies +5VA to the VRH input on the target MCU. This option jumper is configured connected in default configuration.

VDDSYN_EN– JP5

The VDDSYN_EN option jumper allows the end-user to configure VDD33 and VDDSYN to the target MCU. By default, this option jumper is configured to connect the VDDSYN output to the VDD33 input on the target MCU. This option jumper is not installed in default configurations.

VDDREG_SEL– JP6

The VDDREG_SEL option jumper connects either +5V or +3.3V to the VDDREG input on the target MCU. By default, the option jumper is configured to connect +5V to the VDDREG input.

VSTBY_SEL– JP7

The VSTBY_SEL option jumper enables or disables internal memory stand-by voltage to the target MCU. By default, the option jumper is configured to disable the VSTBY input.

REGSEL– JP8

The REGSEL option jumper enables either the on-chip linear regulator controller or the on-chip switch-mode power supply controller.

REGCTL– JP9

The REGCTL option jumper selects between the on-board linear regulator and the on-board switch-mode power supply. This option jumper is configured to select the linear regulator by default.

MDO Option Header – JP12 thru JP27

Option headers JP12 – JP27 provide access to Message Data Out signals, MDO[15:0]. MDO signals are associated with the Nexus Development Interface (NDI) and are used to upload Nexus messages on the rising edge of MCKO. Refer to the target device Reference Manual (RM) for details on configuration and use of these signals.

This option header enables and disables MDOx signal connection to the board stack connector at P1 only. MDOx signal connections to the NEXUS Port connector are always active.

DEVELOPMENT PORTS

The ADAT416 applies 1 NEXUS and 1 JTAG development ports. Several signals are shared by both development ports; therefore, only 1 type of development cable should be applied during any given development session. A CBTLV3861 device buffers development port input and power signals protecting the target MCU from damage by transient input. This buffer provides 5 ohms, series resistance on the development signals when connected. The buffer also provides signal isolation when disconnected.

To ensure proper communications, the ADAT416 and development cable must be powered in the proper sequence. Use the following power sequence to connect a development cable.

The power sequence shown below should be used when connecting a development cable to the ADAT416. This sequence should be used if the ADAT416 is mated to the EVBMB or used in a stand-alone configuration.

ADAT416 Power Sequence

1) Ensure power is switched OFF
2) Connect development port cable to the desired development port
3) Apply power to the target board.
4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

NEXUS Port

The device microcontroller contains multiple Nexus clients that communicate over a single IEEE-ISTO 5001™-2003 Nexus class 3 combined JTAG IEEE 1149.1/auxiliary out interface. Combined, all of the Nexus clients are referred to as the Nexus development interface (NDI). Class 3 Nexus allows for program, data, and ownership trace of the microcontroller execution without access to the external data and address buses.

The MDO Option Header is also associated with the NDI (see above). Refer to the target device Reference Manual for details on configuration and use of the NDI. The development tool port consists of an AMP 38-pin Mictor connector (pn 767053-1). The figure below details the pin-out for the Nexus development tool connector.

Figure 2: NEXUS Port

Signal			Signal
MDO12	1	2	MDO13
MDO14	3	4	MDO15
MDO9	5	6	ENGCLK
BOOTCFG1	7	8	MDO8
B_RESET*	9	10	B_EVTI*
TDO	11	12	B_+3.3V
MDO10	13	14	B_RDY*
B_TCK	15	16	MDO7
B_TMS	17	18	MDO6
B_TDI	19	20	MDO5
B_JCOMP	21	22	MDO4
MDO11	23	24	MDO3
RSTOUT*	25	26	MDO2
NXS27(2)	27	28	MDO1
NXS29(2)	29	30	MDO0
+V	31	32	EVTO*
+V	33	34	MCKO
NXS35(3)	35	36	MSEO1*
B_VSTBY	37	38	MSEO0*

Notes:
1) B_… signals are buffered, bi-directional IO
2) NXSxx signals connect to a test pad adjacent to the NEXUS port connector
3) Signal names followed by a “*” symbol are active logic low.

JTAG Port

The JTAG port provides a standard 1149.1-2001 JTAG connection to the target MCU. The connector is a standard 2x7, 0.1" space, keyed box header. Example compatible cables include the OCDEMON™ NP-JTAG OnCE "Wiggler" and the P&E Microcomputer Systems CABPPCNEXUS. Host software supporting each cable must be used.

The figure below details the pin-out for the JTAG development tool connector.

Figure 3: JTAG Port Connector

Signal			Signal
B_TDI	1	2	GND
TDO	3	4	GND
B-TCK	5	6	GND
B_EVTI*	7	8	JTG8 TP
B-RESET*	9	10	B_TMS
B_+3.3V	11	12	GND
B_RDY*	13	14	B_JCOMP

Notes:
1. B_… signals are buffered.
2. JTG8 TP signal is not connected to the target MCU. This pin connects to a test pad on the board.
3. All development cables may not support the B_EVTI* signal. Option CT5 cut will isolate this signal if not supported by the development cable.
4. Signals followed by a "*" symbol are active- low logic.