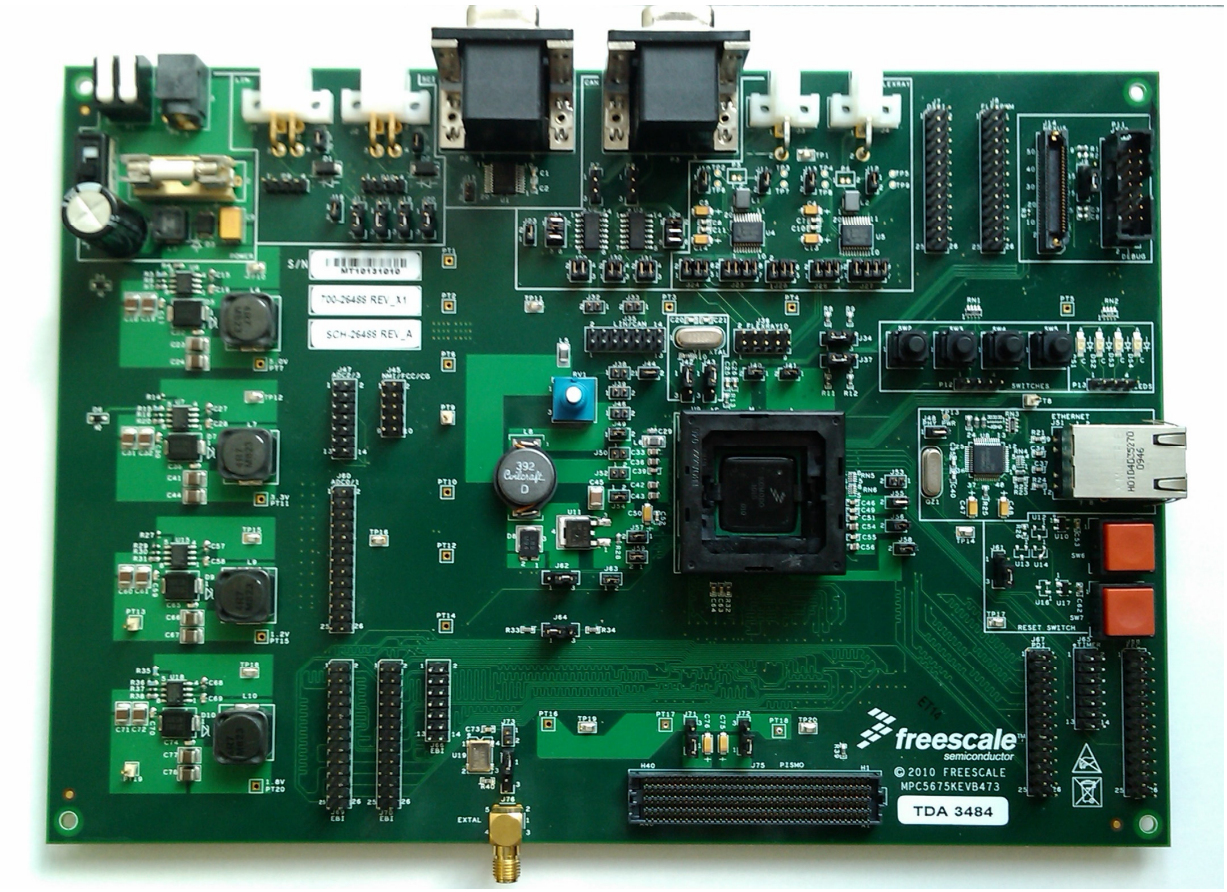

MPC5675EVB Users Manual
257 BGA Rev B

Revision 2.0

August 2010

Revision History:

Revision	Date	Author	Comment
0.1	April 2010	A. Robertson	Initial Release, RevA PCB's only.
1.2	May 2010	A. Robertson	Updated with known bugs list
2.0	August 2010	A. Robertson	Updated for new EVB Rev B

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Index of Figures and Tables

1. Introduction

This user's manual details the setup and configuration of the Freescale Semiconductor MPC5675K (Komodo/Golddust) Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the MPC5675K family of microprocessors, and to facilitate hardware and software development.

At the time of writing this document, the MPC5675K family is offered in a 257MAPBGA and 473MAPBGA package. Both the 473MAPBGA and 257BGA packages support Nexus debug for development purposes. For the latest product information, please speak to your Freescale representative or consult the MPC5675K web pages at www.freescale.com

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

This manual is written for the 257BGA jumper number change between EVB's so please check correct schematic. The main difference is the DDR PISMO connector has been removed from the 257BGA and the jumper numbering is different.

2. EVB Features

The EVB provides the following key features:

- MCU Socket supporting the 257 BGA production package.
- Single 12V external power supply input with on-board regulators to provide all of the necessary EVB and MCU voltages. Power may be supplied to the EVB via a 2.1mm barrel style power jack or a 2-way level connector. 12V operation allows in-car use if desired.
- Flexible on-board power supply configuration with the option to bypass the internal MCU regulators if desired.
- Master power switch and regulator status LED's
- User reset switch with reset status LED's
- Control of the BOOTCFG status via a dedicated jumper.
- Flexible MCU clocking options:
  - 40MHz Oscillator Crystal
  - SMA connector to allow external clock support
  - 8Mhz Oscillator circuit.
- SMA connector on MCU-CLKOUT signal for easy access.
- Standard 14-pin ONCE JTAG debug connector and the new 50-pin Samtec ERF8 NEXUS connectors for 16MDO channels.
- All MCU signals are accessible on port-ordered groups of 0.1" pitch headers.
- SCI channels A and B can be routed to a standard DB9 female connector (PC RS-232 compliant) via a Maxim physical interface.
- FlexCAN channels A and B can be routed to 0.1" headers and DB9 connector via a NXP high speed CAN transceiver which supports both 3.3v and 5v inputs.
- FlexCAN channels are routed to the prototyping area with DB9 connectors to allow additions CAN physical interfaces to be easily integrated.
- User prototyping area consisting of a 0,1" grid of through hole pads with easy access to the EVB ground and power supply rails.
- Ethernet signals routed to a National Semiconductor physical interface and Pulsejack RJ45 connector with integrated magnetics.
- LINFLEX Molex Connector and 0.1" 4 pin header are available.
- FLEXRAY CON PLUG Connector is available.
- 4 active low LED's and 4 pushbutton switches for development purposes.
- Jumper selectable variable resistor connected to ADC channel 0, driving between VRH and VRL.
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB.

IMPORTANT

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board.

Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

3. Configuration

This section details the configuration of each of the EVB functional blocks.

Throughout this document, all of the default jumper and switch settings are clearly marked with "**(D)**" and are shown in blue text. This should allow a more rapid return to the default state of the EVB if required. Note that the default configuration for 3-way jumpers is a header fitted between pins 1 and 2. On the EVB, 2-way and 3-way jumpers have been aligned such that Pin 1 is either to the top or to the left of the jumper. On 2-way jumpers, the source of the signal is connected to Pin 1.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

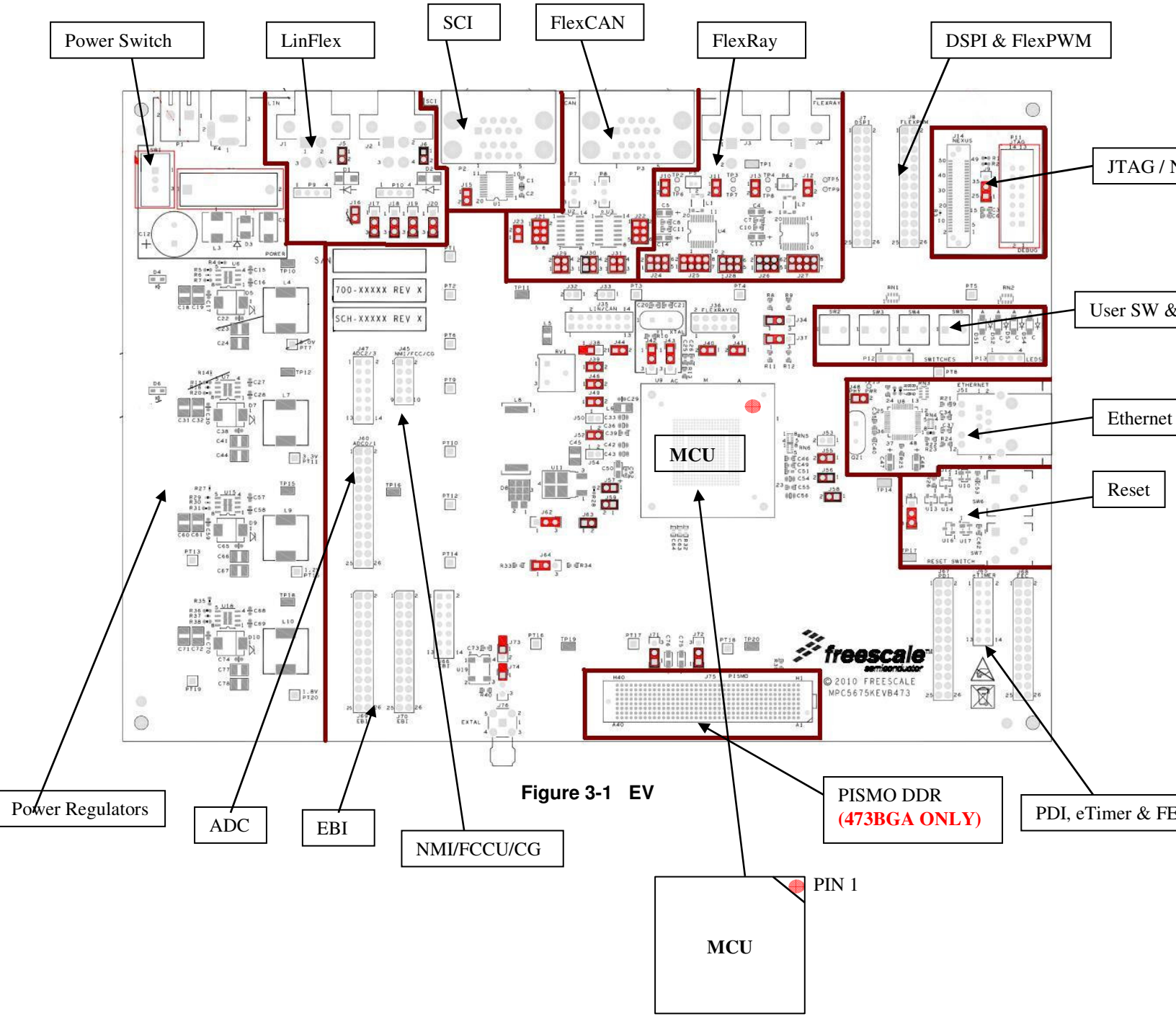

Figure 3-1 EV

3.1 Power Supply Configuration

The EVB requires an external power supply voltage of 12V DC, minimum 1A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using switching regulators to provide the necessary EVB and MCU operating voltages of 5.0V, 3.3V 1.8v and 1.2V (257BGA does not have the 1.8v supply). For flexibility there are two different power supply input connectors on the EVB as detailed below.

3.1.1 Power Supply Connectors

2.1mm Barrel Connector – P4:

This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1mm plug uses the correct polarisation as shown below:

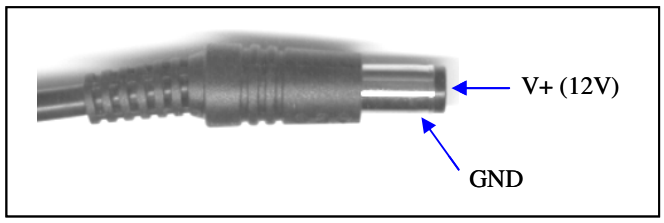

Figure 3-2 2.1mm Power Connector

2-Way Lever Connector – P1:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

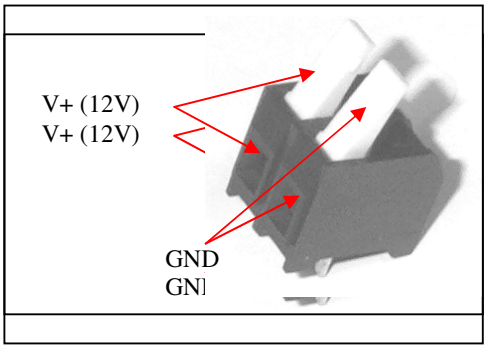

Figure 3-3 2-Lever Power Connector

3.1.2 Power Switch (SW1)

Slide switch SW1 can be used to isolate the power supply input from the EVB voltage regulators if required.

Position 1 will turn the EVB **OFF**
Position 3 will turn the EVB **ON**

3.1.3 Power Status LED's and Fuse

When power is applied to the EVB, a green power LED's adjacent to each of the voltage regulators show the presence of the supply voltages.

Green LED D15 = 5.0v Linear supply for ADC
Green LED D12 = 5.0v for EVB supply
Green LED D11 = 3.3v for EVB Supply
Green LED D14 = 1.2v for EVB supply

If there is no power to the MCU it is possible that either power switch SW1 is in the "OFF" position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a 20mm 500mA fast blow fuse.

3.1.4 MCU Supply Routing and Jumpers (J78, J79)

The EVB is designed to run the MCU at 3.3v with the option to run the ADC and the ballast circuitry (PMC) at 5v.

The MCUs ADC and ballast circuitry can be operated in 5v and 3.3v modes by changing J70 (ADC) and J71 (PMU) to the 3.3v or 5V jumper position.

The FLEXCAN and FlexRay circuitry also has 5V supplies to the transceivers.

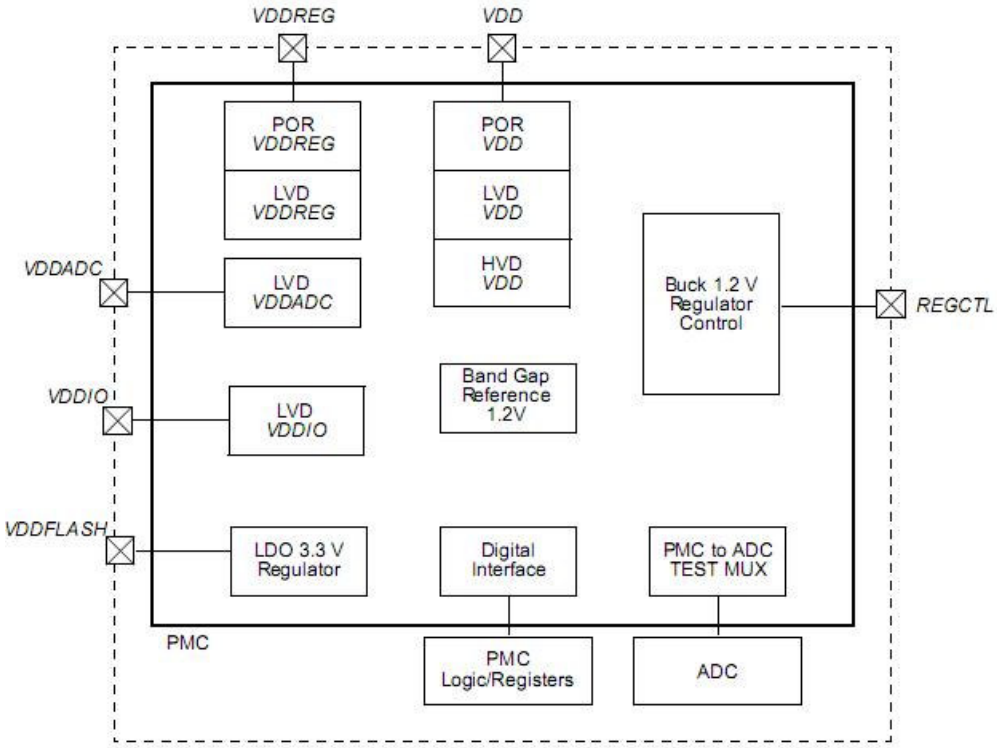

Table 3-1 MCU Power Supply Jumpers

Power Domain	Jumper	Position	Description
3.3V	**J43 (VDD_HV_IO)**	1-2 **(D)**	This supplies the IO with 3.3v
3.3v/1.8v	**J59 (VDD_HV_DRAM_REF)**	1-2 **(D)** Position 2	3.3 V to supply HV_DRAM, this needs to be supplied even though the 257BGA has no DRAM
3.3v	**J47 (VDD_HV_FLA)**	1-2 **(D)**	3.3v supply to HV_FLA (NVM FLASH supply)
3.3v	**J61 (VDD_HV_PDI)**	1-2 **(D)**	3.3v to supply PDI External supplies can be added to pin 2 if extra PDI voltages are required.
3.3v	**J41 (VDD_HV_OSC)**	1-2 **(D)**	3.3v to Oscillator circuitry
3.3v	**J56 (VDD_HV_ADV)**	1-2 **(D)**	3.3v to ADC circuitry
3.3v/5.0v	**J70 (VDD_HV_ADR)**	1-2 **(D)**	ADC Reference voltage 3.3v ADC Reference voltage 5.0v
1.2v	**J60 (VDD_LV_COR)**	1-2 **(D)**	Supplies the core with 1.2v in external mode ONLY. Do not populate if generating core voltage from internal VREG. This may damage the device.
3.3v/5.0v	**J52 (VDD_HV_PMU)**	2-3 **(D)**	3.3v supply for the PMU(VREG). 5.0v supply for the PMU(VREG).
1.2v	**J53 (VREG_CTRL)**	1-2	This should always be populated
3.3v/5.0v	**J71 (VDD_VREG CTRL)**	2-3	3.3v supply for the VREG_CTRL. 5.0v supply for the VREG_CTRL.

The jumper configuration shown in Table 3-1, details the default state **(D)** of the EVB. In this configuration all power is supplied from the regulators.

3.2 MCU Clock Control

3.2.1 Main Clock Selection (J39, J40, J67 and J68)

The EVB supports three possible MCU clock sources:

(1) The local 40MHz oscillator circuit
(2) An 8MHz oscillator module on the EVB (U18), driving the MCU EXTAL signal
(3) An external clock input to the EVB via the SMA connector (J68), driving the MCU EXTAL signal

The clock circuitry is shown in the diagram below. Please refer to the appropriate EVB schematic for specific jumper numbers and circuitry.

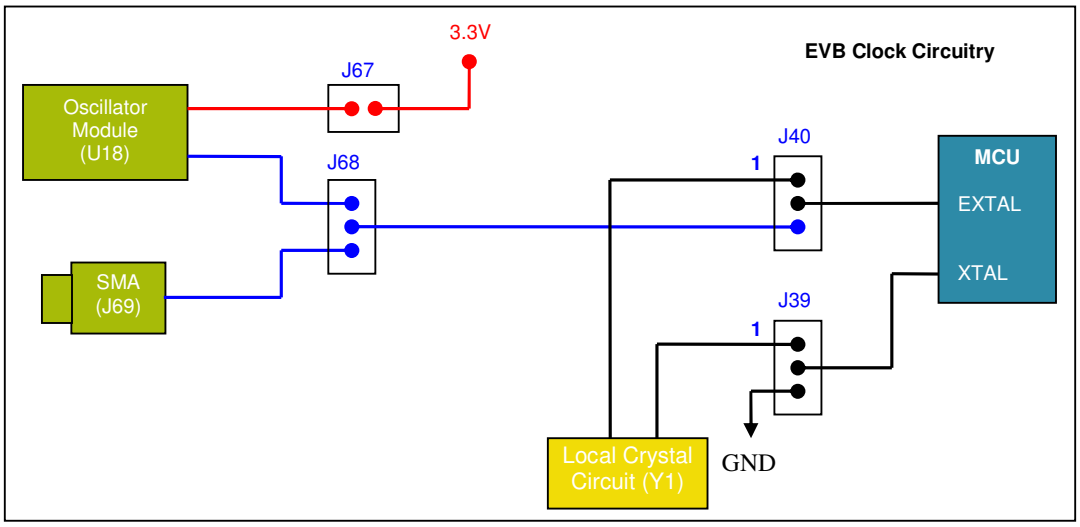

Figure 3-4 EVB Clock Selection

Table 3-2 Clock Source Jumper Selection

Jumper	Position	PCB Legend	Description
J67 (U18 PWR)	FITTED **(D)** REMOVED		EVB oscillator module U19 is powered EVB oscillator module U19 is not powered
J68(OSC SEL)	1-2 **(D)** 2-3	MOD SMA	8Mhz Oscillator is routed from U18 SMA external square wave input
J39 **Must Match J40**	1-2 **(D)** 2-3	Y1 GND	MCU Clock is Y1 XTALIN GND
J40 **Must Match J39**	1-2 **(D)** 2-3	Y1 EVB	MCU Clock is Y1 XTALOUT MCU Clock is Selected by J68

Note that the 3.3V regulator must be enabled when using oscillator module Y1.

CAUTION

The MPC5675K clock circuitry is all 3.3v based. Any external clock signal driven into the SMA connector must have a maximum voltage of 3.3V.

3.2.2 Reset Boot Configuration (J69, J34, J37)

The MPC5675 has 3 boot configuration jumpers (BOOTCFG) that determines the boot location of the MCU based at POR (Power On Reset). This is shown in the table below:

Table 3-3 BOOTCFG Control

J64 (FAB)	J37 (ABS2)	J34 (ABS0)	Boot ID	Boot Mode
2-3	1-2	1-2	-	Serial Boot LINFlex
2-3	1-2	2-3	-	Serial Boot FlexCAN
2-3	2-3	1-2	-	Serial Boot via LINFlexD or FlexCAN in autobaud
1-2	-	-	Valid	SC (Single Chip)
1-2	-	-	Not Valid	Safe Mode

3.3 ONCE and Nexus

The EVB supports a standard JTAG / ONCE cable with a 14-pin 0.1” walled header footprint. There is also a 50-pin Samtec ERF8 connector for Nexus debug.

3.3.1 Debug Connector Pinouts

The EVB is fitted with 14-pin JTAG / ONCE and 50-pin Nexus debug connectors. The following diagram shows the 14-pin JTAG / ONCE connector pin out (0.1” keyed header).

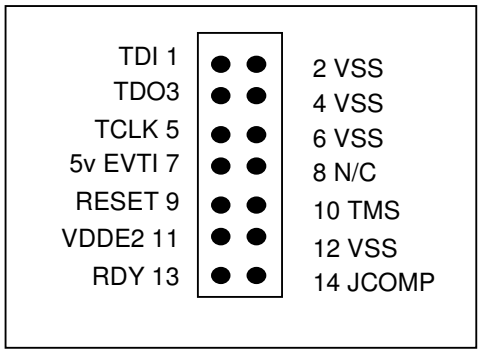

Figure 3-5. MPC5675 JTAG / ONCE Connector

The Nexus module used on the MPC5675K family uses the JTAG pins (for control of the Nexus block) along with additional Nexus pins for trace messages. Nexus mode is entered by a JTAG sequence whereby the Nexus EVTI pin is sampled on the rising edge of the JTAG TRST pin. If the EVTI is asserted on TRST, Nexus is enabled.

The table below shows the pin out of the 50-pin Samtec ERF8 Nexus connector for the MPC5675K. The new 50 pin Nexus connector has been used to support the new 16 MDO channels.

Table 3-4. NEXUS Debug Connector Pinout

Pin No	Function	BGA		Pin No	Function	BGA
1	MSEO[0]	H3		2	V_DEBUG	E1
3	MSEO[1]	G4		4	TCK	TCK
5	GND	GND		6	TMS	TMS
7	MDO0	E1		8	TDI	TDI
9	MDO1	D1		10	TDO	TDO
11	GND	GND		12	JCOMP	JCOMP
13	MDO2	E2		14	RDY	J1
15	MDO3	D2		16	EVTI	H4
17	GND	GND		18	EVTO	H1
19	MCKO	G1		20	JTAG RST	JTAG RST
21	MDO4	F4		22	RESET OUT	RESET OUT
23	GND	GND		24	GND	GND
25	MDO5	A4		26	-	
27	MDO6	F3		28	-	
29	GND	GND		30	GND	GND
31	MDO7	A5		32	-	
33	MDO8	G3		34	-	
35	GND	GND		36	GND	GND
37	MDO9	A6		38	-	
39	MDO10	F1		40	-	
41	GND	GND		42	GND	GND
43	MDO11	F2		44	MDO13	J2
45	MDO12	J3		46	MDO14	B5
47	GND	GND		48	GND	GND
49	MDO15	C2		50	-	

Note - In order to preserve the ability to accurately measure power consumption on the MCU pins, the JTAG and Nexus connector reference voltages will be sourced directly from the 5V regulator.

3.4 CAN Configuration (J20, J21, J29, J30, J31)

The EVB has 2x NXP TJA1041T high speed CAN transceiver on the MCU CAN-A and CAN-B channels. These can operate with 5v or 3.3v I/O from the MCU. For flexibility, the CAN transceiver I/O is connected to a standard 0.1" connector and DB9 connector at the top edge of the PCB. Connectors P8 and P3A provides the CAN bus level signal interface for CAN-A and connector P7 and P3B for CAN-B. The pin out for these connectors is shown below.

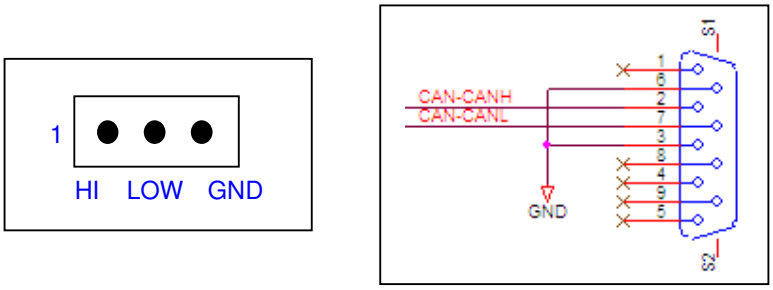

Figure 3-6 CAN Physical Interface Connector

Each of the MCU signals to the CAN transceivers is jumpered, allowing the transceiver to be isolated if that MCU pin is not configured or used for CAN operation. There is a 2x2 jumper for each CAN channel (one for Rx, one for Tx). There are also two power jumpers (J30) to physically remove power (12v and 5v) from both of the CAN transceivers. Jumpers J21 (CAN B) and J22 (CAN A) are configuration jumpers for each of the Transceivers to control Wake, Standby and Enable. Jumpers can be fitted to select default values or wires can be used to connect these pins to the MCU.

Table 3-5 CAN Control Jumpers (J30, J31, J21, J22)

Jumper	Position	PCB Legend	Description
J30 Posn 1-2	FITTED **(D)** REMOVED		5v is applied to both CAN transceivers VCC No 5v power is applied to CAN transceivers
J30 Posn 3-4	FITTED **(D)** REMOVED		12v Power is applied to both CAN transceivers VBAT No 12v power is applied to CAN transceivers
J31 (CAN-A) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU CAN0_TXD is connected to CAN controller A MCU CAN0_TXD is NOT routed to CAN controller.
J31 (CAN-A) Posn 3-4	FITTED **(D)** REMOVED	RX	MCU CAN0_RXD is connected to CAN controller A MCU CAN0_RXD is NOT routed to CAN controller.
J29 (CAN-B) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU CAN1_TXD is connected to CAN controller B MCU CAN1_TXD is NOT routed to CAN controller.
J29 (CAN-B) Posn 3-4	FITTED **(D)** REMOVED	RX	MCU CAN1_RXD is connected to CAN controller B MCU CAN1_RXD is NOT routed to CAN controller.
J21 & J22 Posn 1-2	FITTED **(D)** REMOVED	WAKE	CAN Transceiver WAKE is connected to GND WAKE is not connected and available on Pin 2
J21 & J22 Posn 3-4	FITTED **(D)** REMOVED	STB	CAN Transceiver STB is connected to 5v STB is not connected and available on Pin 4
J21 & J22 Posn 5-6	FITTED **(D)** REMOVED	EN	CAN Transceiver is Enabled EN is not connected and available on Pin 6

Access to the Error and inhibit signals from the transceivers is provided on J32 and J33.

Notes

- Care should be taken when fitting the jumper headers as they can easily be fitted in the incorrect orientation.

3.5 RS232 Configuration (J6, J17, J18, J23, J24)

The EVB has a single MAX3223 RS232 transceiver device, providing RS232 signal translation for the MCU SCI channels A and B.

Each of the two RS232 outputs from the MAX3223 device is connected to a DB9 connector, allowing a direct RS232 connection to a PC or terminal. Connector P2A provides the RS232 level interface for MCU SCI-A and P2B for MCU SCI-B. The pinout of these connectors is detailed below. Note that hardware flow control is not supported on this implementation.

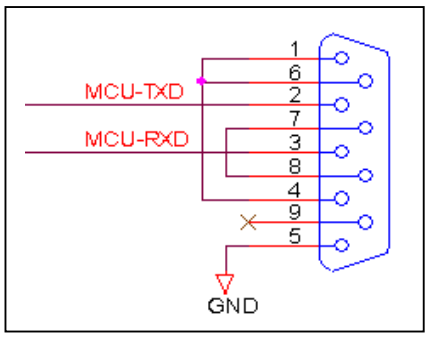

Figure 3-7 RS232 Physical Interface Connector

The MPC5675 SCI also provides hardware LIN master capability which is supported on the EVB via LIN transceivers. Jumpers J17, J18, J23 and J24 are provided to isolate the MCU SCI signals from the RS232 interface as described below. There is also a global power jumper (J15) controlling the power to the RS232 transceiver.

Table 3-6 RS232 Control Jumpers

Jumper	Position	Description
J15 (SCI-PWR)	FITTED **(D)** REMOVED	Power is applied to the MAX3223 transceiver No power is applied to the MAX3223 transceiver
J18 (SCI-A)	2-3 REMOVED	MCU TXD-A is routed to MAX3223 MCU TXD-A signal is disconnected from CAN/LIN
J17 (SCI-A)	2-3 REMOVED	MCU RXD-A is routed via MAX3223 MCU RXD-A signal is disconnected from CAN/LIN
J19 (SCI-B)	2-3 REMOVED	MCU TXD-B is routed via MAX3223 MCU TXD-B signal is disconnected from CAN/LIN
J20 (SCI-B)	2-3 REMOVED	MCU RXD-B is routed via MAX3223 MCU RXD-B signal is disconnected from CAN/LIN

The default configuration enables SCI-A and SCI-B channels. RS232 compliant interfaces (with no hardware flow control) are available at DB9 connector P1. If the MCU is configured such that SCI-A or SCI-B is set as a normal I/O port, then the relevant jumpers must be removed to avoid any conflicts occurring. If required, jumper J15 can be used to completely disable the SCI transceiver.

LIN Configuration (J5, J6, J16, J23,J18,J17,J19,J20)

The EVB is fitted with two Freescale MCZ33661EF LIN transceivers. The LINFLEX module incorporates a UART mode, and as such, the LIN transceivers are connected to the TX and RX signals of SCI via UART A and B.

For flexibility, the LIN transceivers are connected to a standard 0.1" connector (P9 for LIN-C and P10 for LIN-D) and a 4 pin molex connector (J1 for LIN-A and J2 for LIN-B) at the top edge of the PCB as shown in the figure below.

For ease of use, the 12V EVB supply is fed to pin1 of the P9, P10 headers and the LIN transceiver power input to pin 2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of header P9/P10 using a 0.1" jumper shunt.

*** Ensure P9 and P10 are added before running LIN as they are not the default on the EVB*

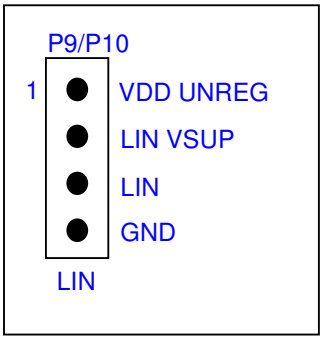

Figure 3-8 LIN Physical Interface Connectors

Along with the MCU signal routing jumpers (J17 / J18 /J19 / J20), there is are jumpers (J16 / J23) to enable or disable the LIN transceiver and jumpers (J5 and J6) which determines if the LIN transceiver is operating in master or slave mode, as defined in the table below.

Table 3-7 LIN Control Jumpers

Jumper	Position	Description
J5	FITTED **(D)** REMOVED	LIN-A transceiver is configured for LIN Master mode LIN-A transceiver is configured for LIN Slave mode
J6	FITTED **(D)** REMOVED	LIN-B transceiver is configured for LIN Master mode LIN-B transceiver is configured for LIN Slave mode
J16*	FITTED **(D)** REMOVED	The LIN-A transceiver is enabled The LIN-A transceiver is disabled
J23*	FITTED **(D)** REMOVED	The LIN-B transceiver is enabled The LIN-B transceiver is disabled
J18	2-3 1-2	MCU LIN0_TXD is connected to SCI_A TX MCU LIN0_TXD is connected to LIN Physical
J17	2-3 1-2	MCU LIN0_RXD is connected to SCI_A TX MCU LIN0_RXD is connected to LIN Physical
J19	2-3 1-2	MCU LIN1_TXD is connected to SCI_B TX MCU LIN1_TXD is connected to LIN Physical
J20	2-3 1-2	MCU LIN1_RXD is connected to SCI_B TX MCU LIN1_RXD is connected to LIN Physical

** Note – Jumpers J16/J23 do NOT route power to LIN transceivers, they only control an enable line on the LIN device. Power to the LIN transceiver is supplied via connectors P9/ P10, Pin 2.*

The Default LIN configuration is with the module enabled in master mode, LIN slave mode can be enabled by removing jumpers J5 / J6.

On the 275BGA EVB only the LIN transceiver2 (U19) J19 +J20 are not connected to the MCU as they are also used of the timing critical FEC. There to use the LIN transceiver connect a flying lead from pin 1 of each Jumper (19+20) to the appropriate pin elsewhere on the EVB.

3.6 FlexRAY Configuration (J19, J27, J25, J26, J28)

The EVB is fitted with 2 FlexRAY physical interfaces connected to MCU FlexRAY channels A and B. Jumpers J19 and J27 are provided to route the respective MCU signals to the physical interfaces as described below.

Table 3-8 Flexray MCU Signal Routing Jumpers (J19, J27)

Jumper	Position	PCB Legend	Description
J26 (Flex-A) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU B8 is connected to Flexray A transceiver TX MCU B8 is not connected to Flexray A transceiver TX
J26 (Flex-A) Posn 3-4	FITTED **(D)** REMOVED	TXEN	MCU A8 is connected to Flexray A transceiver TXEN MCU A8 is not connected to Flexray A transceiver TXEN
J26 (Flex-A) Posn 5-6	FITTED **(D)** REMOVED	RX	MCU E3 is connected to Flexray A transceiver RX MCU E3 is not connected to Flexray A transceiver RXEN
J24 (Flex-B) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU A7 is connected to Flexray B transceiver TX MCU A7 is not connected to Flexray B transceiver TX
J24 (Flex-B) Posn 3-4	FITTED **(D)** REMOVED	TXEN	MCU B7 is connected to Flexray B transceiver TXEN MCU B7 is not connected to Flexray B transceiver TXEN
J24(Flex-B) Posn 5-6	FITTED **(D)** REMOVED	RX	MCU C5 is connected to Flexray B transceiver RX MCU C5 is not connected to Flexray B transceiver RXEN

The power to the Flexray physical interface is controlled via jumper J28 to allow disconnection if required.

Table 3-9 Flexray Power Control Jumpers (J25)

Jumper	Position	PCB Legend	Description
J28 (Flex-PWR) Posn 1-2	FITTED **(D)** REMOVED	12V	12V Flexray circuitry is powered from main 12V input 12V Flexray circuitry is not powered
J28 (Flex-PWR) Posn 3-4	FITTED **(D)** REMOVED	5V	5V Flexray circuitry is powered from 5.0V switching reg 5V Flexray circuitry is not powered
J28 (Flex-PWR) Posn 5-6	FITTED **(D)** REMOVED	VIO	VIO Flexray circuitry is powered from 3.3v VIO Flexray circuitry is not powered

The flexray interface has 4 pins which are used for configuration and are pulled high or low controlled by a jumper as described in the table below. By default, all of the jumper headers are fitted. Please consult the Flexray physical interface specification before changing any of these jumpers.

Table 3-10 Flexray Control Jumpers (J26, J28)

Jumper	Position	PCB Legend	Description
J27 (Flex-A) Posn 1-2	FITTED **(D)**	BGE	Flexray-A interface BGE signal is pulled to VIO
	REMOVED		Flexray-A interface BGE signal is unterminated
J27 (Flex-A) Posn 3-4	FITTED **(D)**	EN	Flexray-A interface EN signal is pulled to VIO
	REMOVED		Flexray-A interface EN signal is unterminated
J27 (Flex-A) Posn 5-6	FITTED **(D)**	STBEN	Flexray-A interface STBN signal is pulled to VIO
	REMOVED		Flexray-A interface STBN signal is unterminated
J27 (Flex-A) Posn 7-8	FITTED **(D)**	WAKE	Flexray-A interface WAKE signal is pulled to GND
	REMOVED		Flexray-A interface WAKE signal is unterminated
J25 (Flex-B) Posn 1-2	FITTED **(D)**	BGE	Flexray-B interface BGE signal is pulled to VIO
	REMOVED		Flexray-B interface BGE signal is unterminated
J25 (Flex-B) Posn 3-4	FITTED **(D)**	EN	Flexray-B interface EN signal is pulled to VIO
	REMOVED		Flexray-B interface EN signal is unterminated
J25 (Flex-B) Posn 5-6	FITTED **(D)**	STBEN	Flexray-B interface STBN signal is pulled to VIO
	REMOVED		Flexray-B interface STBN signal is unterminated
J25 (Flex-B) Posn 7-8	FITTED **(D)**	WAKE	Flexray-B interface WAKE signal is pulled to GND
	REMOVED		Flexray-B interface WAKE signal is unterminated

Notes:

- *The flexray physical interfaces are connected to 2 pin molex connectors (FlexRAY A) 1.25mm shrouded 2-pin connectors to connect to the flexray bus (as are standard fit on many Freescale development platforms using flexray).*

Important:

A 40Mhz oscillator is required for the correct operation of the flexray controller. Please ensure that the 40Mhz crystal is selected as the system clock or use a 40Mhz external clock source.

3.7 Ethernet

The EVB is fitted with a National Semiconductor DP8348C Ethernet physical interface (U8) and a RJ45 connector with integrated activity LED's and magnetics (J51).

The National Semiconductor DP8348C physical interface is connected to the MII on the MPC5675. This is a fixed connection with no means of isolation. Pullups are also also present on some of these signals. These are detailed in the table below. Please be aware of this when using the related GPIOs.

Table 3-11 Pull up/ Pull down resistors for Ethernet Physical

Port Pin	Pull Direction	Strength
FEC_CRS	Down (GND)	2.2kΩ
FEC_RX_ER	Down (GND)	2.2kΩ
FEC_RX_DV	Down (GND)	2.2kΩ
FEC_RXD0	Down (GND)	2.2kΩ
FEC_RXD1	Down (GND)	2.2kΩ
FEC_RXD2	Down (GND)	2.2kΩ
FEC_RXD3	Down (GND)	2.2kΩ
FEC_TX_EN	Down (GND)	2.2kΩ
FEC_TXD0	Down (GND)	2.2kΩ
FEC_TXD1	Down (GND)	2.2kΩ
FEC_TXD2	Down (GND)	2.2kΩ
FEC_TXD3	Down (GND)	2.2kΩ

The voltage domain that is used by the GPIO should be set to 3.3v when power is applied to the physical interface.

Power can be removed from the physical interface via J48.

Table 3-12 Ehternet Physical Interface Power Supply Enabled (J48)

Jumper	Position	PCB Legend	Description
J48 (PHY PWR)	FITTED (D) REMOVED	**PHY PWR**	The DP4348C Ethernet Physical Interface is powered from the 3.3v SR. The DP4348C Ethernet Physical Interface is not powered

4. Default Jumper Summary Table

257BGA ONLY

The following table details the DEFAULT jumper configuration of the EVB as explained in detail in section 3. 257GA ONLY

Table 4-1 Default Jumper Positions

See next page

Jumper Reference	Default Setting	Jump Count	Description
J43	ON	1	Power on VDD_HV_IO is enabled
J59	ON	1	VDD_HV_DRAM_REF is enabled
J47	ON	1	Power on VDD_HV_FLA is enabled
J61	ON	1	Power on VDD_HV_PDI is enabled
J41	ON	1	Power on VDD_HV_OSC is enabled
J56	ON	1	Power on VDD_HV_ADV is enabled
J70	Short 1-2	1	Power on VDD_HV_ADR is 5.0V
J60	OFF	0	Power on VDD_LV_COR is disabled
J53	ON	1	Internal power is enabled
J52	ON	1	Internal power is enabled
J71	Short 2-3	1	Internal power is enabled and 3.3V to VDD_PMU
J48	Short 2-3	1	Internal power is enabled
J50	Short 1-2	1	VPP_TEST should be grounded
J38	OFF (place on PIN1 only)	1	POTS on ADC0 is disabled
J55	Short 2-3	1	PW_ON_RESET is enabled
J63	Short 1-2	1	MCRGM_FAB is tied to ground
J34	Short 1-2	1	MCRGM_ABS0 is tied to ground
J37	Short 1-2	1	MCRGM_ABS2 is tied to ground
J40	Short 1-2	1	Use on board 40.0MHz crystal
J39	Short 1-2	1	Use on board 40.0MHz crystal
J67	OFF (place on PIN1 only)	1	Use on board 40.0MHz crystal
J68	OFF (place on PIN1 only)	1	Use on board 40.0MHz crystal
J46	ON	1	Power on Ethernet PHY is enabled
J30	ON	2	Power on CAN PHY is enabled
J31	ON	2	CANA TXD & RXD are connected to MCU
J22	ON	3	CANA control signals are on
J29	ON	2	CANB TXD & RXD are connected to MCU
J21	ON	3	CANB control signals are on
J18	Short 2-3	1	UART TXD is connected to MCU
J17	Short 2-3	1	UART RXD is connected to MCU
J19	Short 2-3	1	UART TXD is connected to MCU
J20	Short 2-3	1	UART RXD is connected to MCU
J16	ON	1	Power on LINC is enabled
J5	ON	1	LINC Bus Master Mode is enabled
J23	ON	1	Power on LIND is enabled
J6	ON	1	LIND Bus Master Mode is enabled
J15	ON	1	Power on SCI is enabled
J28	ON	3	Power on Flexray is enabled
J26	ON	3	FlexrayA data signals are connected to MCU
J27	ON	4	FlexrayA control signals are on
J24	ON	3	FlexrayB data signals are connected to MCU
J25	ON	4	FlexrayB control signals are on
J13	ON	1	FlexrayA decoupling capacitor is disabled
J12	ON	1	FlexrayA decoupling capacitor is disabled
J10	ON	1	FlexrayB decoupling capacitor is disabled
J11	ON	1	FlexrayB decoupling capacitor is disabled
J78	ON	1	FLEXPWM0_B1 is disable to LED
J79	ON	1	FLEXPWM0_B0 is disable to LED
J80	ON	1	FLEXPWM0_A3 is disable to LED
J81	ON	1	FLEXPWM0_A2 is disable to LED
J82	ON	1	FLEXPWM0_X2 is disable to LED
J83	ON	1	FLEXPWM0_X3 is disable to LED
J84	ON	1	FLEXPWM0_A1 is disable to LED
J85	ON	1	FLEXPWM0_B3 is disable to LED

5. User Connector Descriptions

This section details the pinout of the EVB user connectors. The connectors are 0.1 inch pitch turned pin headers and are located at various locations on the EVB. They are grouped by port functionality and the PCB legend shows the respective port number adjacent to each pin.

5.1.1 eTimer (Connector J64)

Table 5-1 eTimer Connector Pinout (J65)

Pin	Function	Pin	Function
1	ETIMER0_ETC0	2	ETIMER1_ETC3
3	ETIMER0_ETC5	4	ETIMER1_ETC0
5	ETIMER0_ETC1	6	ETIMER1_ETC4
7	ETIMER0_ETC2	8	ETIMER1_ETC5
9	ETIMER0_ETC3	10	ETIMER1_ETC1
11	ETIMER0_ETC4	12	ETIMER1_ETC2
13	GND	14	GND

5.1.2 ADC 0/1 (Connector J54)

Table 5-2 ADC 0/1 Connector Pinout (J60)

Pin	Function	Pin	Function
1	GND	2	GND
3	ADC0_AN0	4	ADC1_AN0
5	ADC0_AN2	6	ADC1_AN1
7	ADC0_AN1	8	ADC1_AN2
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	
21	ADC0_ADC1_AN11	22	ADC0_ADC1_AN13
23	ADC0_ADC1_AN12	24	ADC0_ADC1_AN14
25	GND	26	GND

5.1.3 ADC 2/3 (Connector J45)

Table 5-3 ADC 2/3 Connector Pinout (J47)

Pin	Function	Pin	Function
1	ADC2_ADC3_AN 12	2	ADC2_ADC3_AN 14
3	ADC2_ADC3_AN 11	4	ADC2_ADC3_AN 13
5	ADC2_AN2	6	ADC3_AN1
7	ADC2_AN3	8	ADC3_AN0
9	ADC2_AN0	10	ADC3_AN2
11	ADC2_AN1	12	ADC3_AN3
13	GND	14	GND

5.1.4 NMI / FCC / CG (J44)

Table 5-4 NMI / FCC / CG Connector Pinout (J45)

Pin	Function	Pin	Function
1	NMI	2	GND
3	GND	4	MC_CGL_CLK_OUT1
5	FCCU0_F1	6	GND
7	GND	8	MC_CGL_CLK_OUT2
9	FCCU0_F0	10	GND

5.1.5 FLEXPWM (J8)

Table 5-5 FLEXPWM Connector Pinout (J8)

Pin	Function	Pin	Function
1	FLEXPWM1_B2	2	FLEXPWM0_X1
3	FLEXPWM1_B0	4	FLEXPWM0_X0
5	FLEXPWM1_B1	6	FLEXPWM0_X2
7		8	FLEXPWM0_X3
9	FLEXPWM1_A2	10	FLEXPWM0_A0
11	FLEXPWM1_A0	12	FLEXPWM0_A1
13	FLEXPWM1_A1	14	FLEXPWM0_A2
15		16	FLEXPWM0_A3
17		18	FLEXPWM0_B1
19		20	FLEXPWM0_B0
21		22	FLEXPWM0_B2
23		24	FLEXPWM0_B3
25	GND	26	GND

5.1.6 FEC (J66)

Table 5-6 FEC Connector Pinout (J68)

Pin	Function	Pin	Function
1	GND	2	GND
3	FEC_TXD3	4	FEC_RXD2
5	FEC_TXD2	6	FEC_RXD3
7	FEC_TXD0	8	FEC_RXD1
9	FEC_TXD1	10	FEC_RXD0
11	FEC_TX_CLK	12	FEC_RX_CLK
13	GND	14	GND
15	FEC_TX_EN	16	FEC_COL
17	FEC_TX_ER	18	FEC_CRS
19	GND	20	GND
21	FEC_MDC	22	FEC_RX_ER
23	FEC_MDIO	24	FEC_RX_DV
25	GND	26	GND

5.1.7 FLEXRAY (J36)

Table 5-7 FLEXRAY Connector Pinout (J36)

Pin	Function	Pin	Function
1	GND	2	GND
3	FLEXRAY_A_RX	4	FLEXRAY_B_RX
5	FLEXRAY_A_TR_EN	6	FLEXRAY_B_TR_EN
7	FLEXRAY_A_TX	8	FLEXRAY_B_TX
9	GND	10	GND

5.1.8 LINFLEX / FLEXCAN (J35)

Table 5-8 LIN / CAN Connector Pinout (J35)

Pin	Function	Pin	Function
1	GND	2	GND
3	LIN0_TXD	4	LIN1_TXD
5	LIN0_RXD	6	LIN1_RXD
7	GND	8	GND
9	CAN0_TXD	10	CAN1_TXD
11	CAN0_RXD	12	CAN1_RXD
13	GND	14	GND

5.1.9 DSPI (J7)

Table 5-9 DSPI Connector Pinout (J7)

Pin	Function	Pin	Function
1	GND	2	GND
3	DSPI0_CS0	4	DSPI0_SCK
5	DSPI0_CS2	6	DSPI0_SIN
7	DSPI0_CS3	8	DSPI0_SOUT
9	GND	10	GND
11	DSPI2_CS2	12	DSPI2_SCK
13	DSPI2_CS1	14	DSPI2_SIN
15	DSPI2_CS0	16	DSPI2_SOUT
17	GND	18	GND
19	DSPI1_CS0	20	DSPI1_SCK
21	DSPI1_CS2	22	DSPI1_SIN
23	DSPI1_CS3	24	DSPI1_SOUT
25	GND	26	GND

6. Known Bugs List

Nos.	Reported Problems	Potential Answers
1	LINFLEX Transceiver 2 is not connected to MCU	Flying Lead from Pin 1 of J19+J20 to required LIN pins

Appendix A - EVB Schematics

MPC5675KEVB257 Evaluation Board

Table of Contents

Revisions

Rev	Description	Date	Designer
X1	Draft	January 22, 2010	Qiao Jun
X2	Draft 2	January 29, 2010	Robertson Andrew & Qiao Jun
X3	Draft 3	Febuary 2, 2010	Robertson Andrew & Qiao Jun
X4	Draft 4	Febuary 6, 2010	Robertson Andrew & Qiao Jun
X5	Draft 5	Febuary 9, 2010	Robertson Andrew & Qiao Jun
X6	Split ONLY for MPC5671K 257BGA	Febuary 10, 2010	Robertson Andrew & Qiao Jun
X7	reset circuit update	Febuary 11, 2010	Robertson Andrew & Qiao Jun
X8	various updates on pages	Febuary 18, 2010	Robertson Andrew
X9	Back annotate	Febuary 23, 2010	Qiao Jun
A	Release	Febuary 26, 2010	Qiao Jun
A1	Revise	June 20, 2010	Robertson Andrew & Qiao Jun
A2	Revise	June 22, 2010	Robertson Andrew & Qiao Jun
A3	Revise	June 23, 2010	Robertson Andrew & Qiao Jun
B	Revise	June 26, 2010	Qiao Jun
B1	Release	June 29, 2010	Richard Jayne & Pietri Stefano

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6501 William Cannon Drive West
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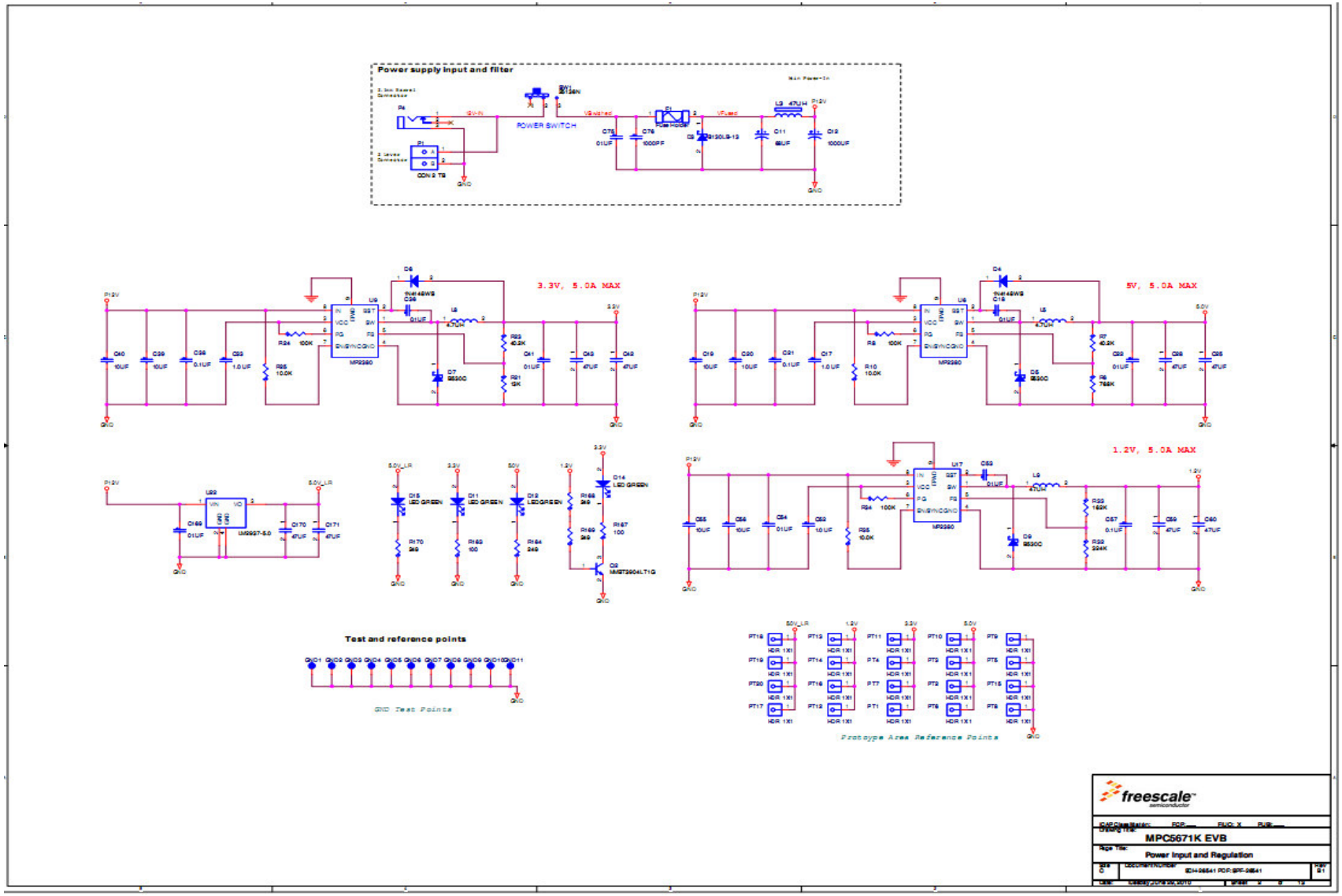
ICAP Classification: FCP: FIUO: X PUBI:

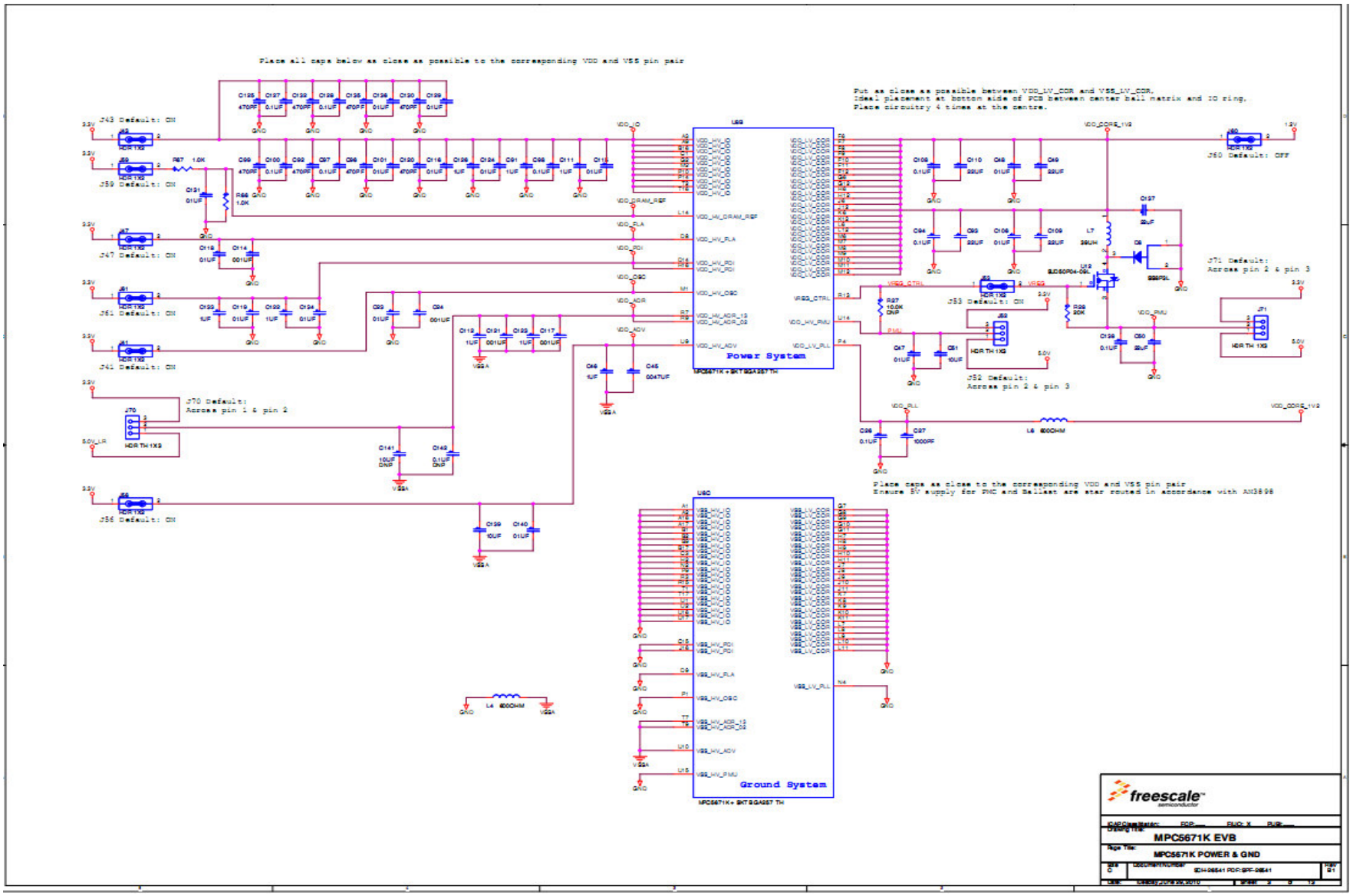
Designer: R60321 & B03443 | Drawing Title: MPC5671K EVB

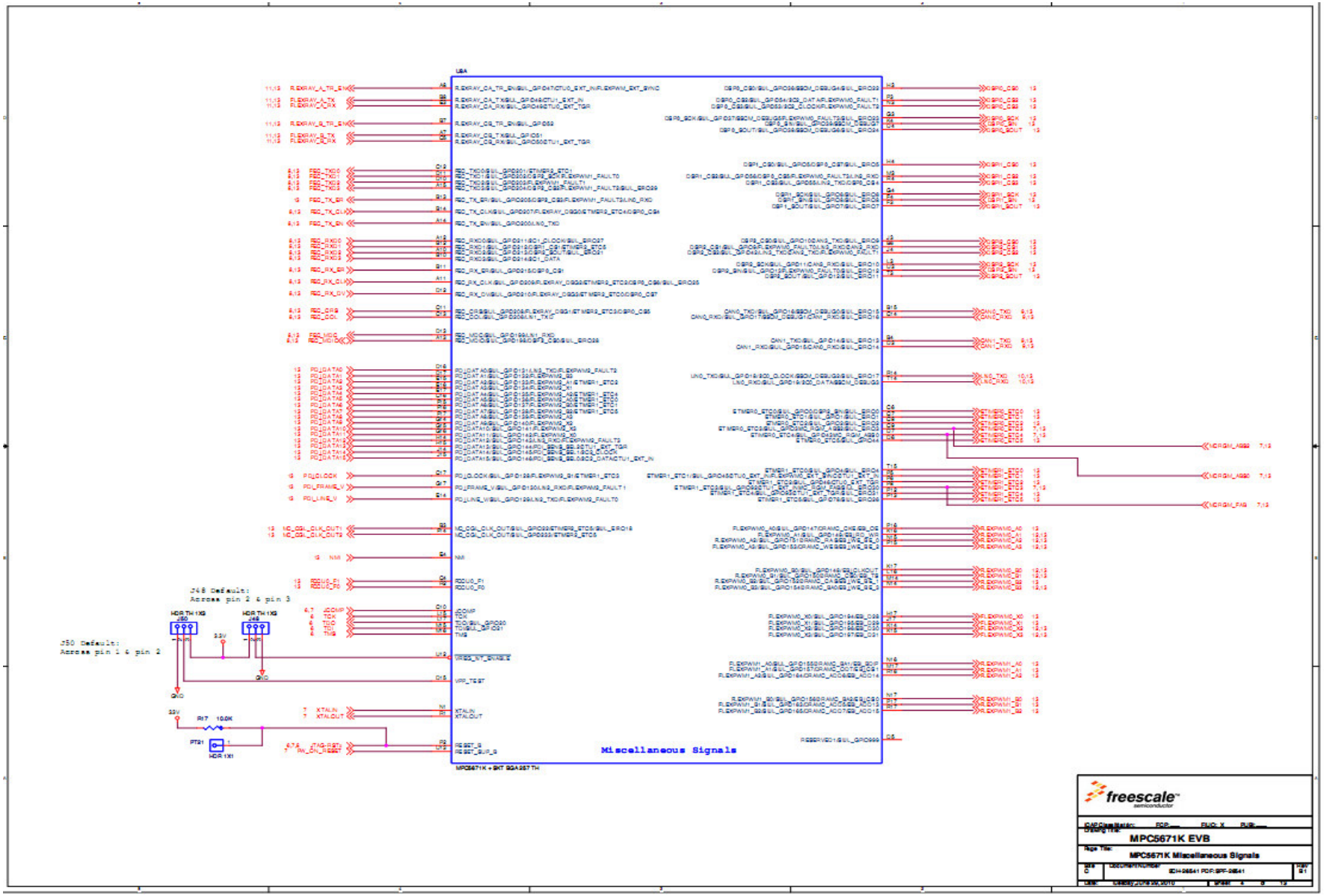
Drawn by: R60321 & B03443 | Page Title: TITLE PAGE

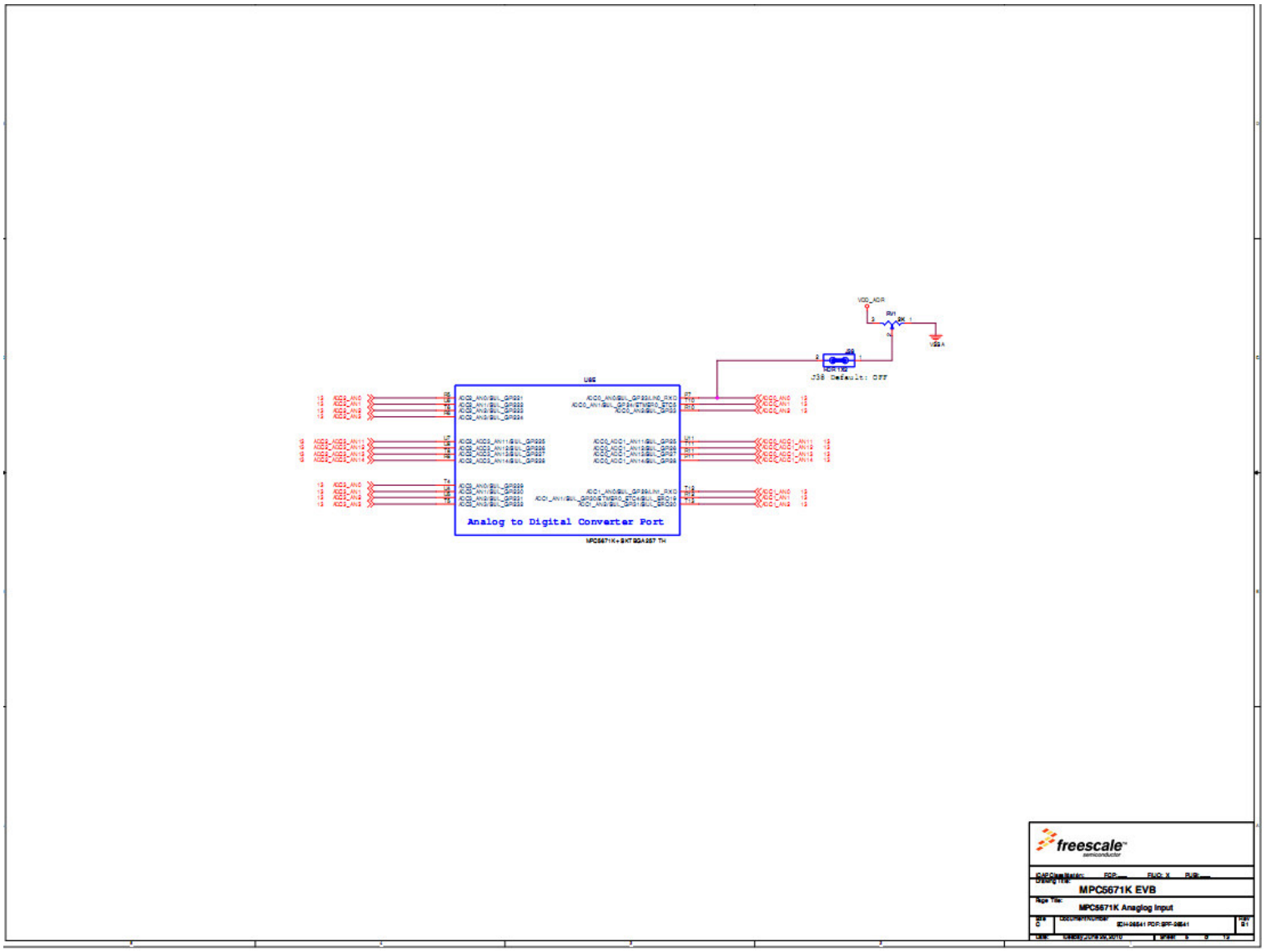
Approved: | Size C | Document Number SCH-26541 PDF: SPF26541 | Rev B1

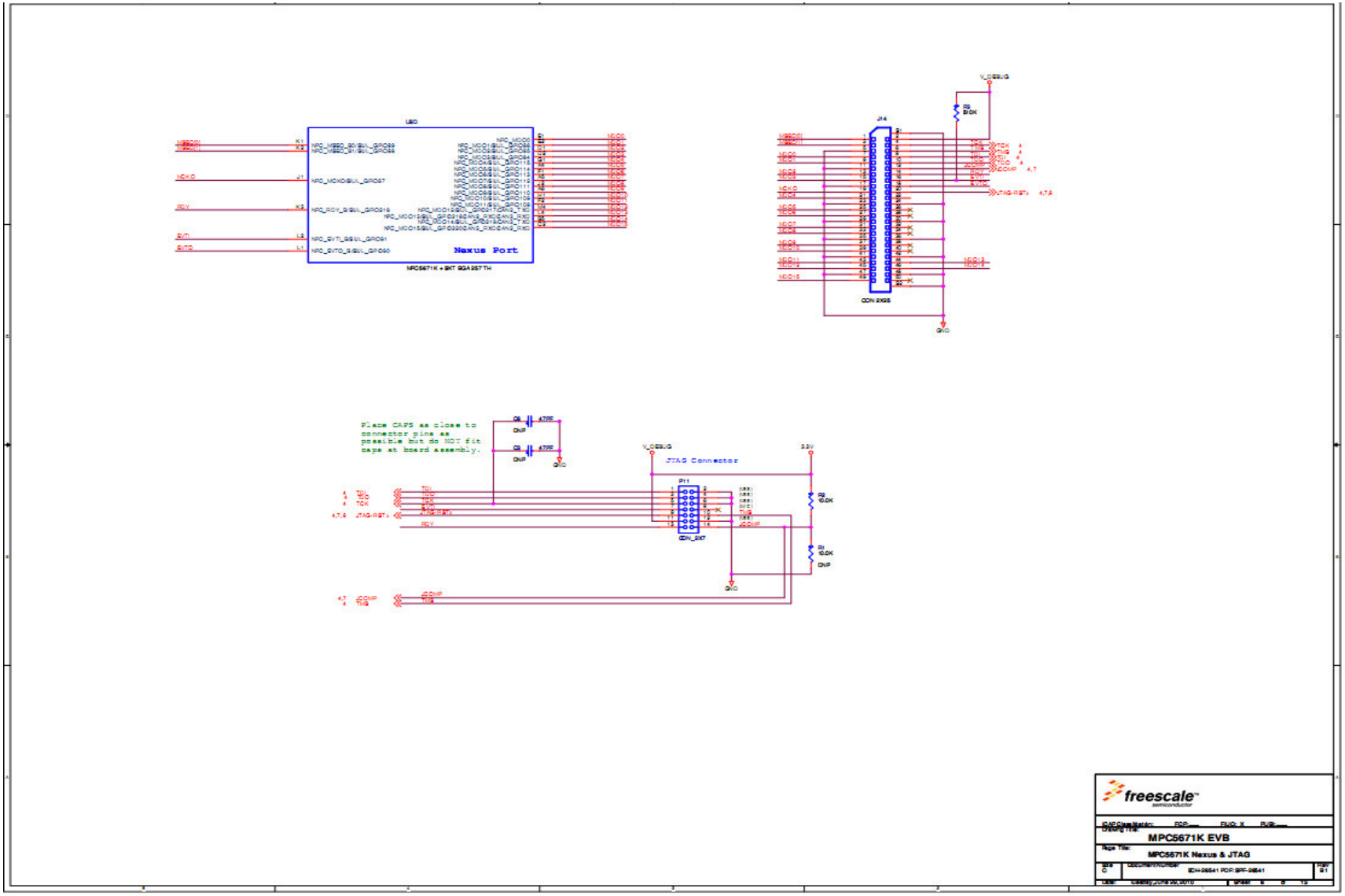
Date: [illegible] | Sheet 1 of 13

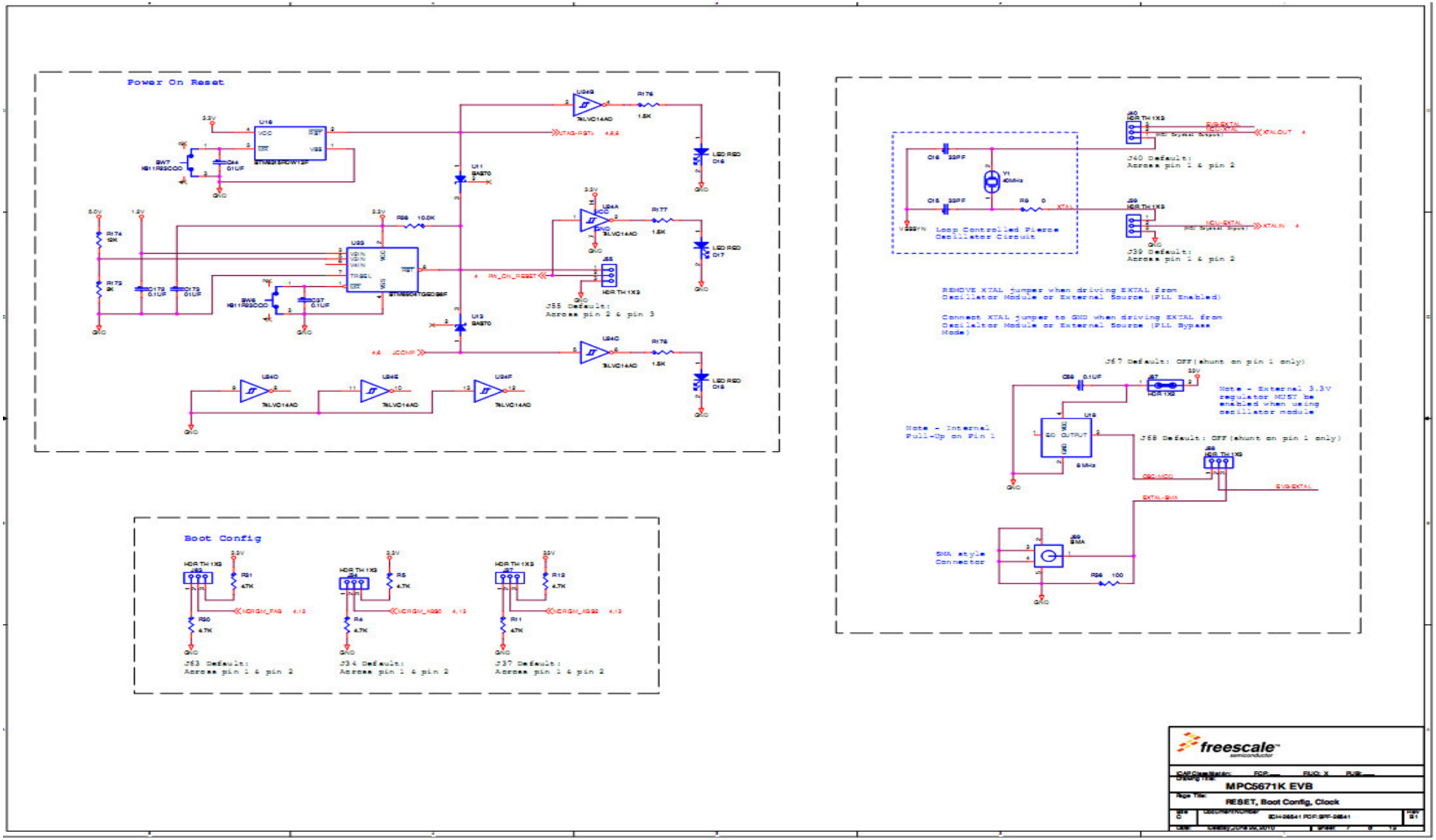

Power supply input and filter
POWER SWITCH
3.3V, 5.0A MAX
5V, 5.0A MAX
1.2V, 5.0A MAX
Test and reference points
GND Test Points
Prototype Area Reference Points
freescale
MPC5671K EVB
Power Input and Regulation

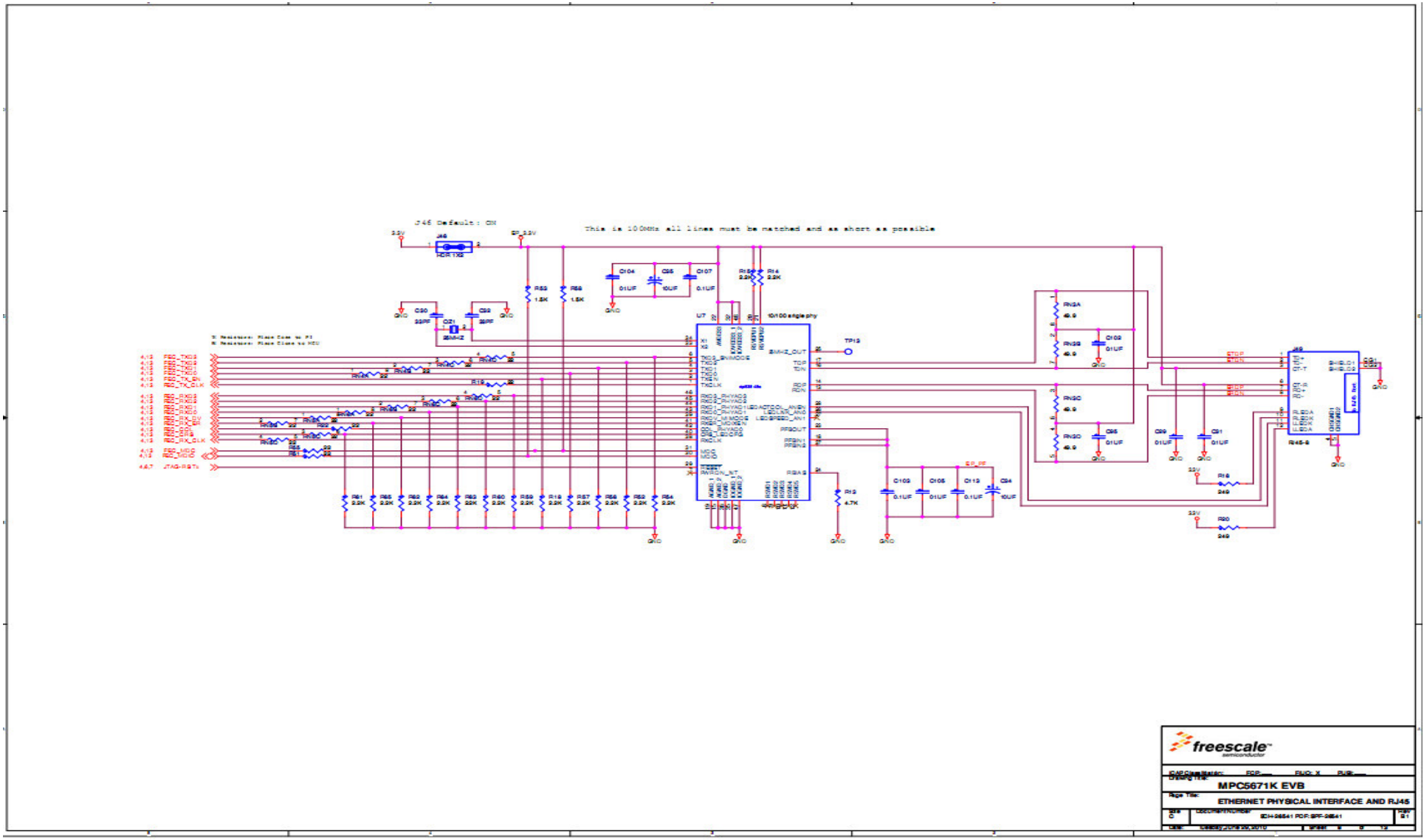

Place all caps below as close as possible to the corresponding VDD and VSS pin pair
Put as close as possible between VDD_LV_COR and VSS_LV_COR.
Ideal placement at bottom side of PCB between center ball matrix and IO ring.
Place circuitry 4 times at the centre.
Power System
Ground System
MPC5671K EVB
MPC5671K POWER & GND
freescale semiconductor

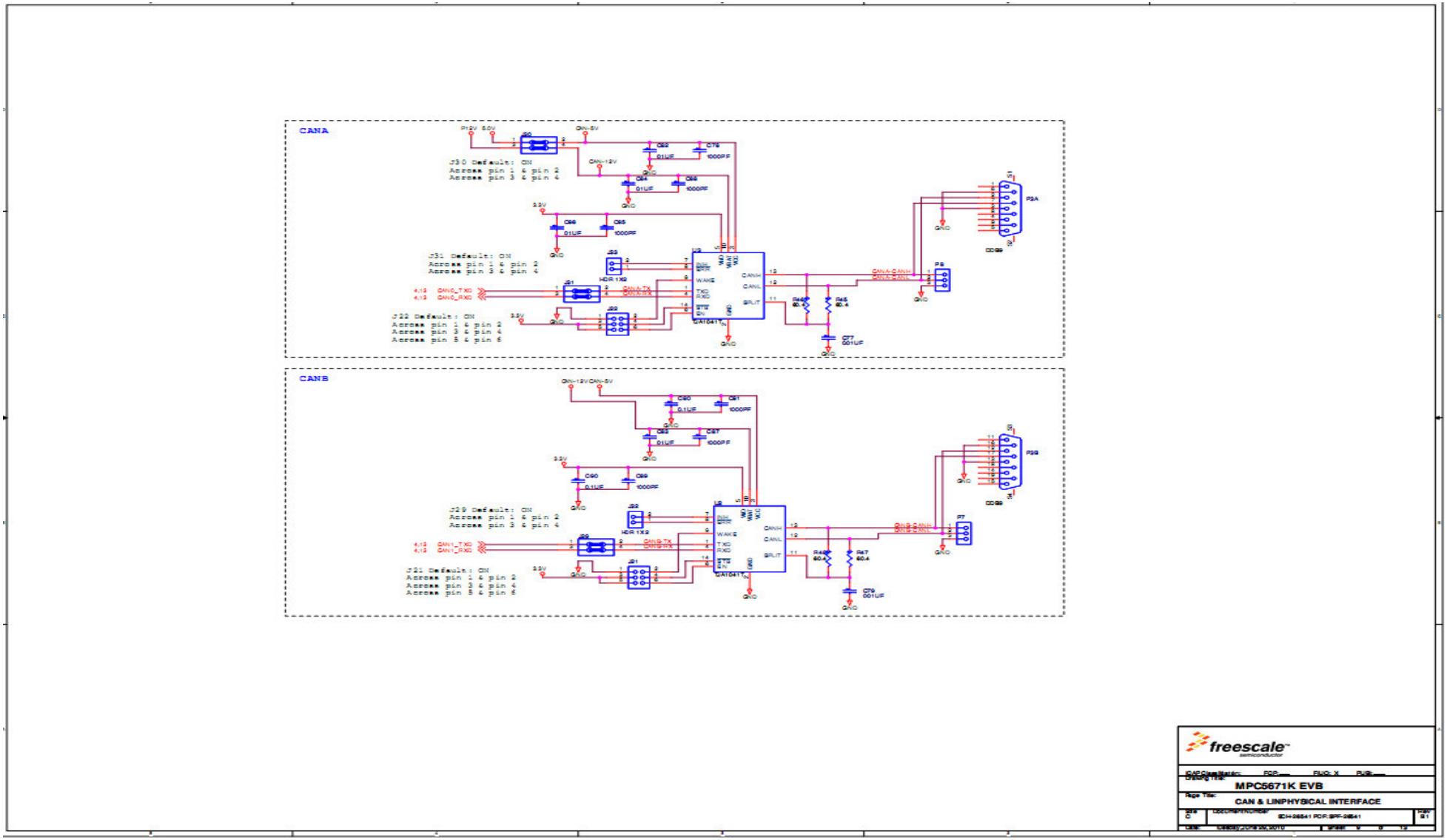

Miscellaneous Signals
MPC5671K EVB
MPC5671K Miscellaneous Signals
freescale

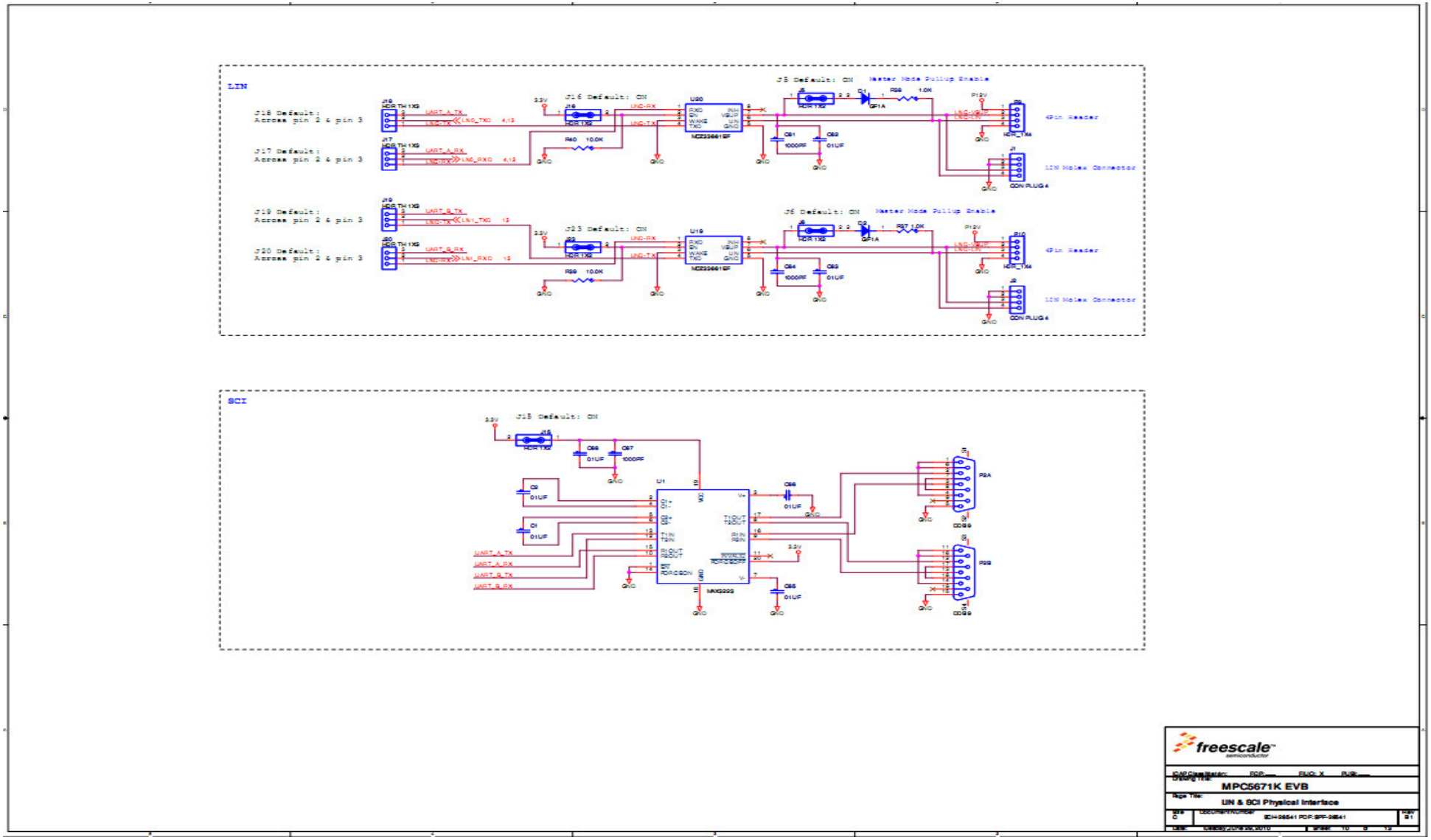

Analog to Digital Converter Port
MPC5671K Evb
MPC5671K Analog Input

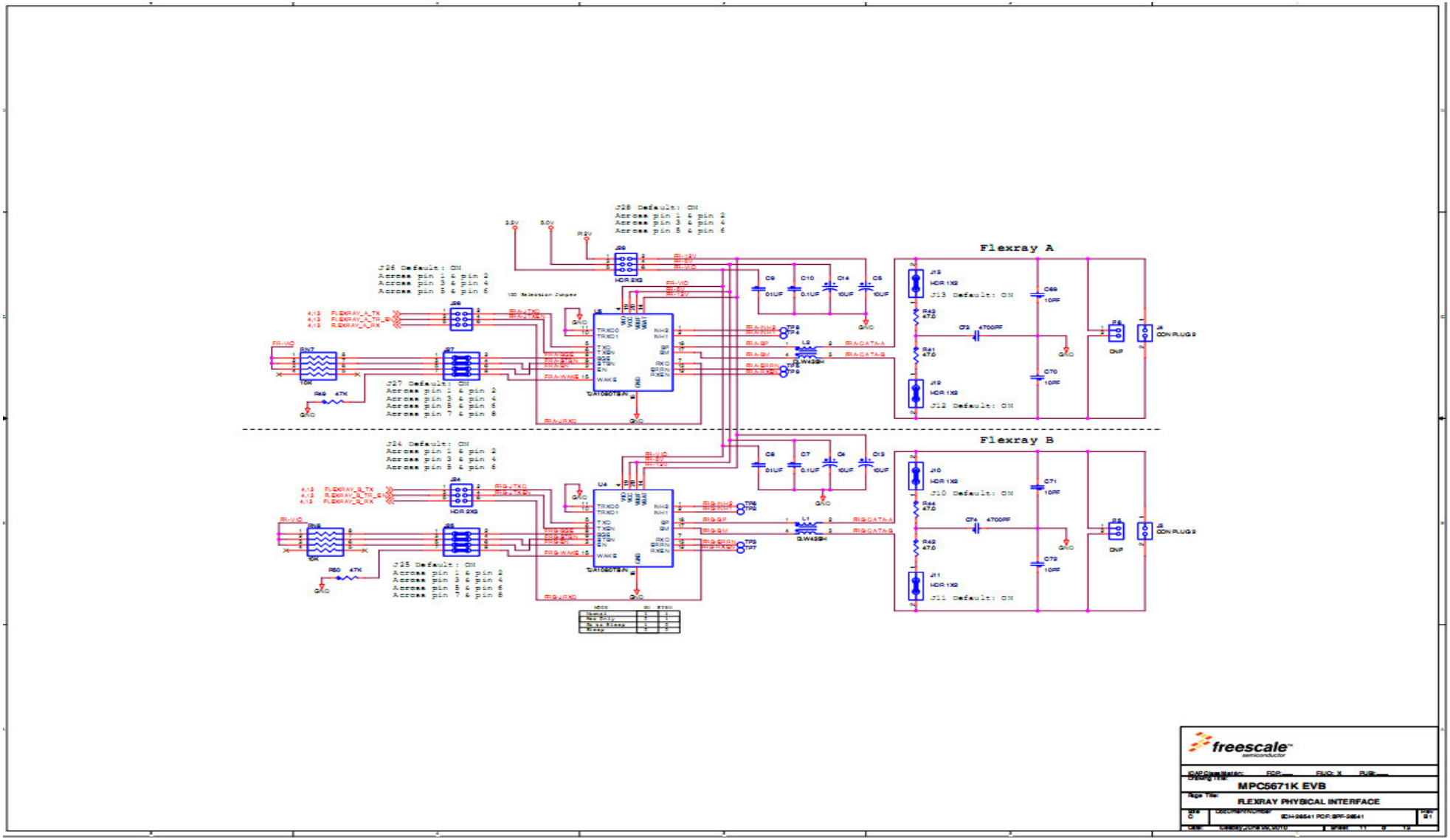

Nexus Port
MPC5671K + SKT BGA257 TH
CON 2X35
Place CAPS as close to connector pins as possible but do NOT clip caps at board assembly.
JTAG Connector
CON_2X7
freescale
MPC5671K EVB
MPC5671K Nexus & JTAG

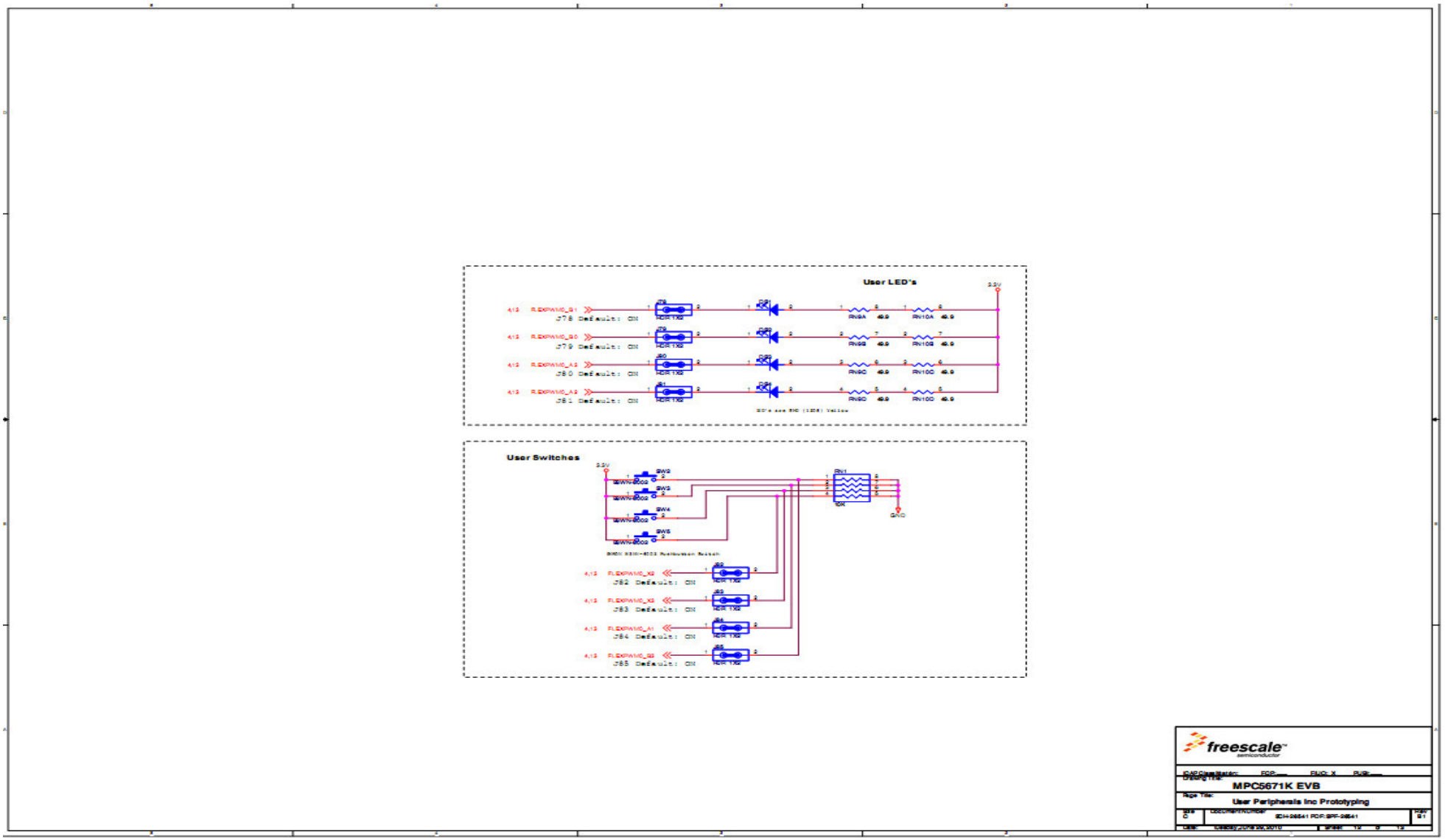

Power On Reset
Boot Config
Loop Controlled Pierce Oscillator Circuit
REMOVE XTAL jumper when driving EXTAL from Oscillator Module or External Source (PLL Enabled)
Connect XTAL jumper to GND when driving EXTAL from Oscillator Module or External Source (PLL Bypass Mode)
Note - Internal Pull-Up on Pin 1
Note - External 3.3V regulator MUST be enabled when using oscillator module
SMA style Connector
MPC5671K EVB
RESET, Boot Config, Clock

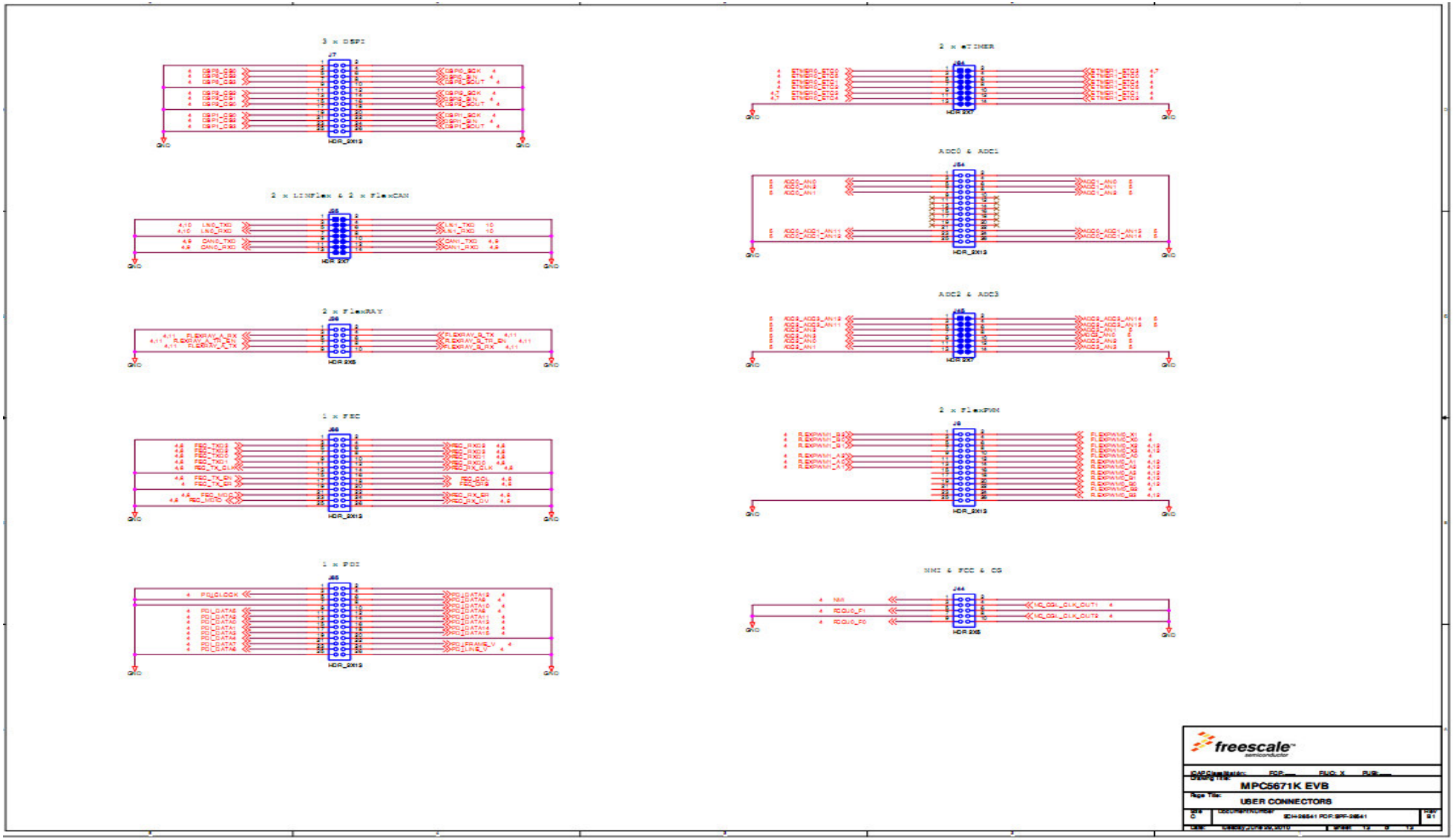

freescale
MPC5671K EVB
ETHERNET PHYSICAL INTERFACE AND RJ45


CANA
CANB
MPC5671K EVB
CAN & LINPHYSICAL INTERFACE


LIN
J18 Default:
Across pin 2 & pin 3
J17 Default:
Across pin 2 & pin 3
J16 Default: ON
J5 Default: ON
Master Mode Pullup Enable
4Pin Header
LIN Molex Connector
J19 Default:
Across pin 2 & pin 3
J20 Default:
Across pin 2 & pin 3
J23 Default: ON
J6 Default: ON
Master Mode Pullup Enable
4Pin Header
LIN Molex Connector
SCI
J15 Default: ON
MAX3223
UART_A_TX
UART_A_RX
UART_B_TX
UART_B_RX
freescale
MPC5671K EVB
LIN & SCI Physical Interface


Flexray A
Flexray B
MPC5671K EVB
FLEXRAY PHYSICAL INTERFACE


User LED's
User Switches
freescale
MPC5671K EVB
User Peripherals Inc Prototyping


3 x DSPI
2 x eTIMER
2 x LINFlex & 2 x FlexCAN
ADC0 & ADC1
2 x FlexRAY
ADC2 & ADC3
1 x FEC
2 x FlexPWM
1 x PDI
NMI & FCC & CS
freescale
MPC5671K EVB
USER CONNECTORS