MC92610 Quad SerDes Design Verification Board User's Guide

MC92610DVBUG
Rev. 3, 06/2005

freescale™
semiconductor

Contents

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Chapter 1
General Information

1.1 Introduction

This user's guide describes the MC92610DVB design verification board, Rev. C and higher. It should be read in conjunction with the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*. The design verification board (DVB) facilitates the full evaluation of the MC92610 Quad 3.125 Gbaud SerDes. It is intended for evaluation and testing purposes only. Freescale does not guarantee its performance in a production environment.

This board was designed to be used with laboratory equipment (pattern generators, data analyzers, BERT, scopes, and so on) or connected to other evaluation boards. Access to the MC92610 device (verification chip) is through connectors to each pin, to allow complete in-depth 'design verification' testing of the chip design. This allows the user to check any or all features/functions of the MC92610 quad device.

The four parallel data input ports, and all configuration/control signal pins, are accessed through common 2×10, 0.100" male connectors (headers). The parallel data output ports are accessed through 2×20, 0.100" connectors. JTAG port signals are also accessed with separate connectors.

The MC92610 high-speed serial receivers and transmitters are accessed through SMA coaxial connectors for signal integrity measurements.

A single 5.0-V power source is required for DVB operation. All necessary voltages are generated by regulators onboard. The reference clock for the MC92610 chip may be provided using either an external clock or the onboard crystal oscillator. Clock drivers on the DVB provide additional clock signals for triggering analyzer instrumentation and scopes.

1.2 Features

The functional, physical, and performance features of the MC92610DVB are as follows:

- A single external 5.0-V to onboard regulators supply +3.3, +1.8, +1.5 V, and HSTL voltage reference power to all onboard circuitry.
- Reference clock source is a 156.25-MHz crystal oscillator or an external clock source
- Parallel data interfaces accessible through standard 0.100", 2 row connectors for data generators and analyzers.
- Full-duplex differential data links accessible through SMA connectors
- Two pairs of 50-Ω test traces with SMA connections facilitate TDR measurements of the characteristic impedance of representative board traces.
- Connector provided for JTAG test access port

1.3 Specifications

The MC92610DVB design verification board specifications are provided in Table 1-1.

Table 1-1. MC92610DVB Design Verification Board Specifications

Characteristics		Specifications
Board revision		Rev. C and higher
External power supply		+5 ± 0.5 V DC < 2.0 A typical
Support circuit regulator		3.3 ± 0.3 V DC
MC92610 core and link I/O regulator		1.8 ± 0.15 V DC
Interface I/O (V_{DDQ}) regulator		1.5 ± 0.1 V DC or 1.8 ± 0.15 V DC
MC92610 package		324 MAPBGA
Operating temperature		0°–30°C
Material		FR-4
Dimensions	Height	14.8", 377 mm
	Width	12.3", 312 mm
	Thickness	0.1", 2.4 mm
Conducting layers		Three ground planes, one split power plane, two signal routing layers, top and bottom component layers with some additional signal routing

1.4 Block Diagram

Figure 1-1 shows the MC92610DVB design verification board block diagram.

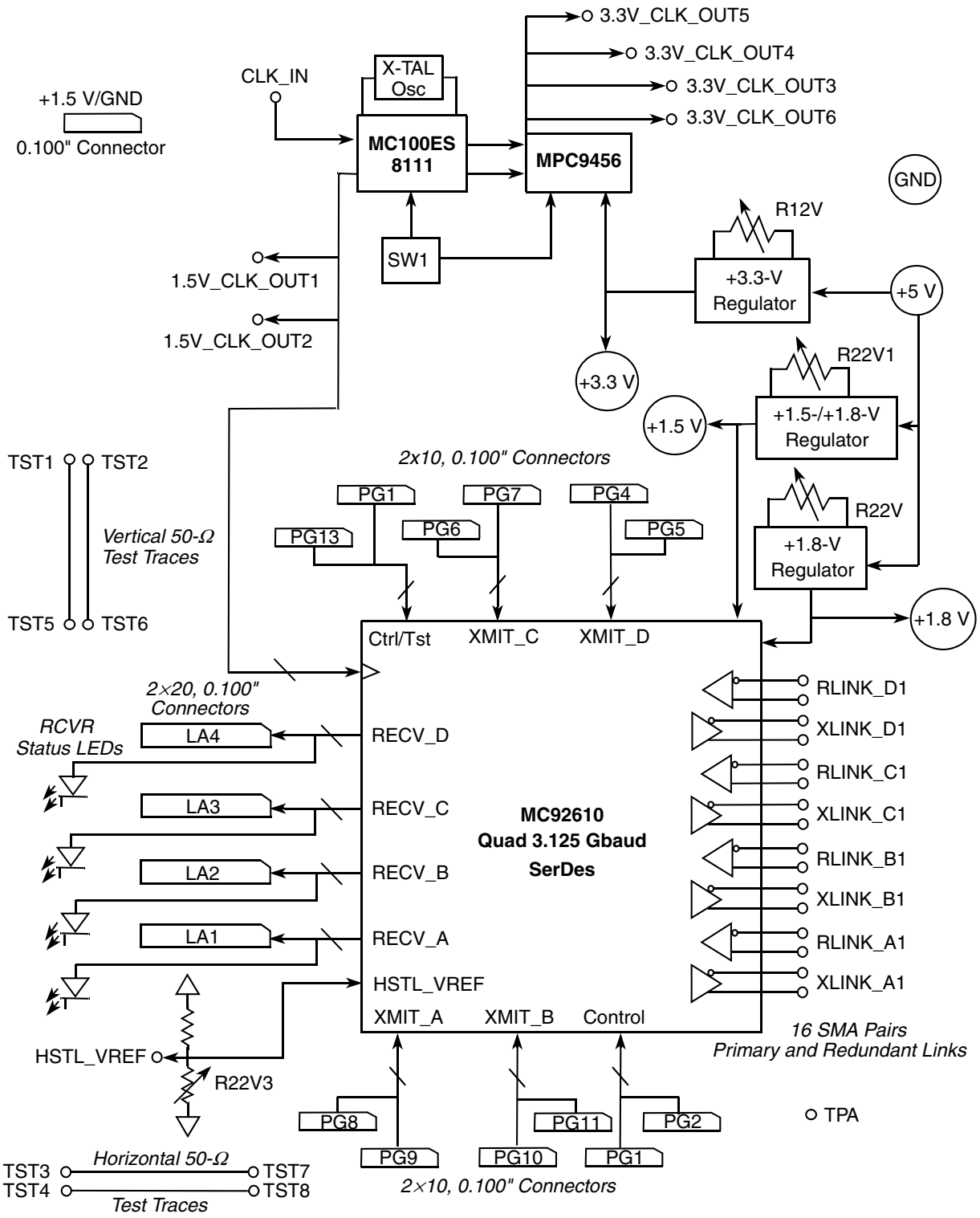


Figure 1-1. MC92610DVB Design Verification Board Block Diagram

1.5 Board Components

Table 1-2 is a list of major components of the MC92610DVB design verification board. A complete parts listing can be found in Appendix B, "Parts List."

Table 1-2. Major Board Components

Component	Description
MC92610VF	Freescale Quad 3.125 Gbaud SerDes
2×10, 0.100" connectors	PG1–PG11, and PG13 provide access to the parallel inputs and control signals.
2×20, 0.100" connectors	LA1–LA4 provide access to the parallel outputs.
2×8, 0.100" connectors	PG12 and PG14 provide access to the $+V_{DD}$ and ground planes.
SMA connectors	SMA1–SMA32: Serial transmit and receive connections TST1–TST8: Impedance test trace connections CLK_OUT1–CLK_OUT6: Reference clock outputs CLK_IN: External reference clock input
LT1587 voltage regulators	VR33, VR18, and VR15: +3.3 V, +1.8 V, and $+V_{DD}$ voltage regulators
Potentiometers	R12V, R22V, R22V1, and R22V2: Potentiometers for setting +3.3 V, +1.8 V, and $+V_{DD}$ and HSTL voltage reference levels
XTAL oscillator	Y1, Y2: Onboard 156.25-MHz crystal oscillator
MC100ES8111 clock buffer	U2: Level shift and clock buffer
MPC9456 clock buffer	U3: +2.5- and +3.3-V LVCMOS clock fanout buffer

1.6 Abbreviation List

Table 1-3 contains abbreviations used in this document.

Table 1-3. Acronyms and Abbreviated Terms

Term	Meaning
'1'	High logic level (nominally 1.5 or 1.8 V)
'0'	Low logic level (nominally 0.0 V)
BIST	Built-in self-test
DVB	Design verification board
I/F	Interface
N/C	No connection
PN	Pseudo-noise
PRBS	Pseudo random bit sequence
TAP	Test access port
TDR	Time delay reflectometry
UIp-p	Peak-to-peak unit interval

1.7 Related Documentation

Related documentation includes the following:

- *MC92610 Quad 3.125 Gbaud SerDes Reference Guide* (MC92610RM)
- MC92610DVB schematics
- MC100ES8111 data sheet
- MPC9456 data sheet
- IEEE Std 802.3-2002®, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications

1.8 Contact Information

For questions concerning the MC92610 design verification kit or to place an order for a kit, contact a local Freescale field applications engineer.

Chapter 2
Hardware Preparation and Installation

This chapter provides instructions for unpacking, hardware preparation, configuration and installation, and a description of the interface components for the MC92610DVB.

2.1 Unpacking Instructions

Unpack the board from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of the equipment.

2.2 MC92610DVB Package Contents

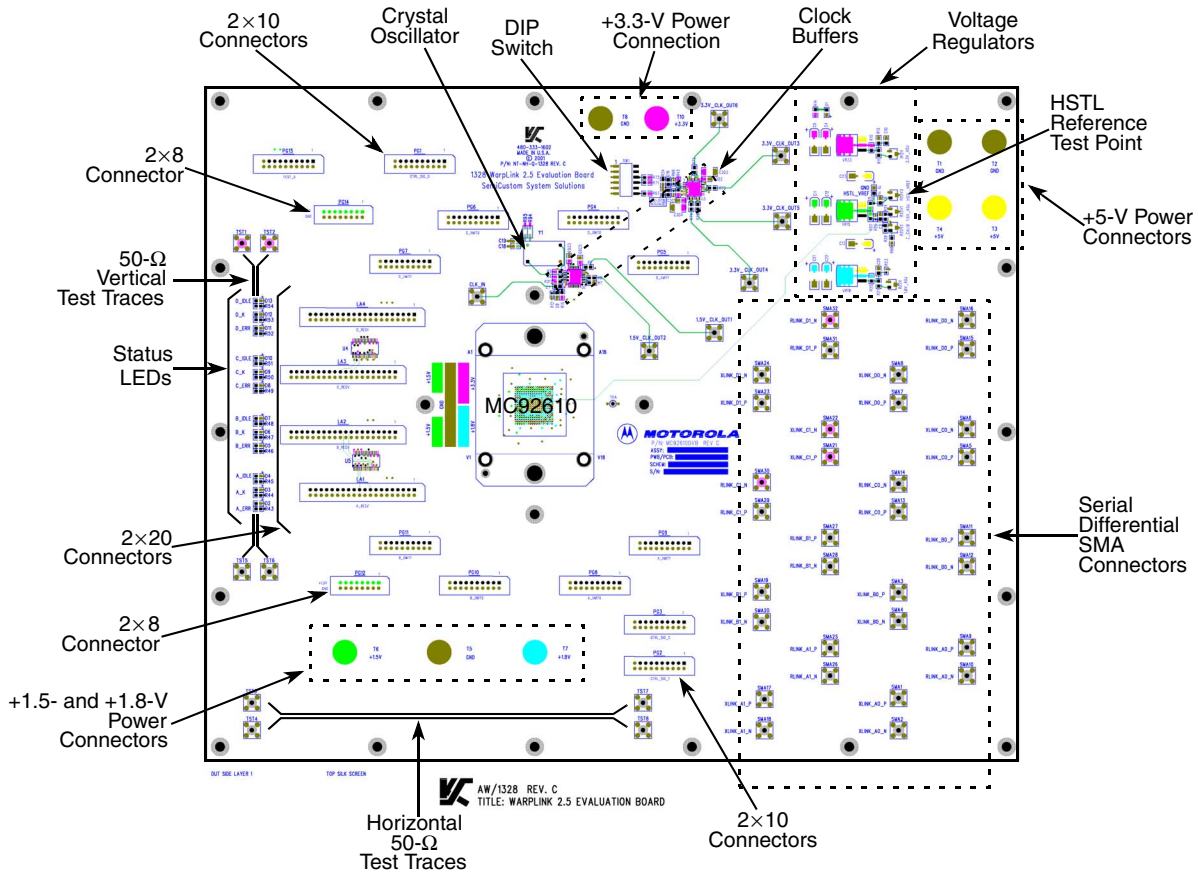
Table 2-1 describes the contents of the MC92610DVB kit.

Table 2-1. MC92610DVB Kit Contents

Quantity	Item
1	MC92610DVB design verification board
1	*MC92610DVBUM Quad SerDes Design Verification Board User's Guide*
1	*MC92610 Quad 3.125 Gbaud SerDes Reference Guide*
1	Complete set of MC92610DVB design verification board schematics
70	0.100" shunts
10	Square pin receptacle patch cords

2.3 Hardware Preparation

Operation of the MC92610DVB requires proper setup of the power supply and voltage regulators as well as the reference clock. Figure 2-1 depicts the location of the major components on the board. The following sections describe proper setup of the MC92610DVB.



NOTE:
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit, or function of the current product.

Figure 2-1. Top Side Part Location Diagram

2.3.1 Setting the Power Supply and Voltage Regulators

The MC92610DVB requires a single +5.0-V supply. Fully operational, the board will draw a maximum current less than 1.5 A from the +5.0-V supply. Actual current consumption depends on the user-set voltage levels, clock frequencies and the MC92610 operating mode. The board contains two +5.0-V connection posts and two ground connection posts. These duplicate connections simplify using a four-wire supply: supply and ground, force and sense.

2.3.2 Setting the Voltage Regulators

The +5.0-V supply powers 3 onboard voltage regulators, VR33, VR18, and VR15. These regulators generate +3.3, +1.8, and +1.5/1.8 V (V_{DDQ}), respectively. The +3.3-V supply provides power to the oscillator, clock buffer chips, and LED drivers. This supply can be varied over the range +3.3 ± 0.3 V using the R12V potentiometer.

The +1.8-V supply powers the MC92610 core logic, transceivers, and on-chip phase-locked loop (PLL). This regulator can be adjusted over the range +1.8 ± 0.15 V using R22V.

The +1.5-V (HSTL) V_{DDQ} supply powers the MC92610 control signal, parallel input, and output interface circuitry. This voltage level is determined by the desired logic interface. The +1.5-V supply can be adjusted using the R22V1 potentiometer from +1.5 V + 0.45 V/–0.15 V. If desired the +1.5-V regulator can be adjusted to match the +1.8-V range for evaluation in those systems that will not contain a separate +1.5-V supply.

The +3.3-V, +1.8-V, and +V_{DDQ} supplies are accessible through connection posts. Please note that these regulators should be set to voltage limits within the operating ranges described in the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide.* Failure to operate within these ranges can cause damage to the MC92610. Freescale does not guarantee MC92610 operation beyond the ranges specified. The R12V, R22V, and R22V1 potentiometers will be factory set for +3.3, +1.8, and +1.5 V, respectively.

2.3.3 HSTL Voltage Reference Regulator

The HSTL I/O has a voltage reference that must be adjusted to set the logic high/low switch point. For a nominal +1.5 V on the +1.5-V (V_{DDQ}) supply, R22V3 should be set such that the voltage at the HSTL_VREF test point is +0.75 V. For those systems whose HSTL voltage will be +1.8 V, this potentiometer should be set to +0.9 V. The R22V3 potentiometer is typically factory set for +0.8 V.

2.4 Reference Clock Source

Through a combination of clock buffers, a reference clock is supplied to the MC92610 and several SMA output connectors. The input reference clock for the MC92610 can be supplied by either using an onboard crystal oscillator or directly driving an external reference clock into the board's clock buffer circuit through the SMA connector, CLK_IN. The clock circuitry for the MC92610DVB is shown in Figure 2-2.

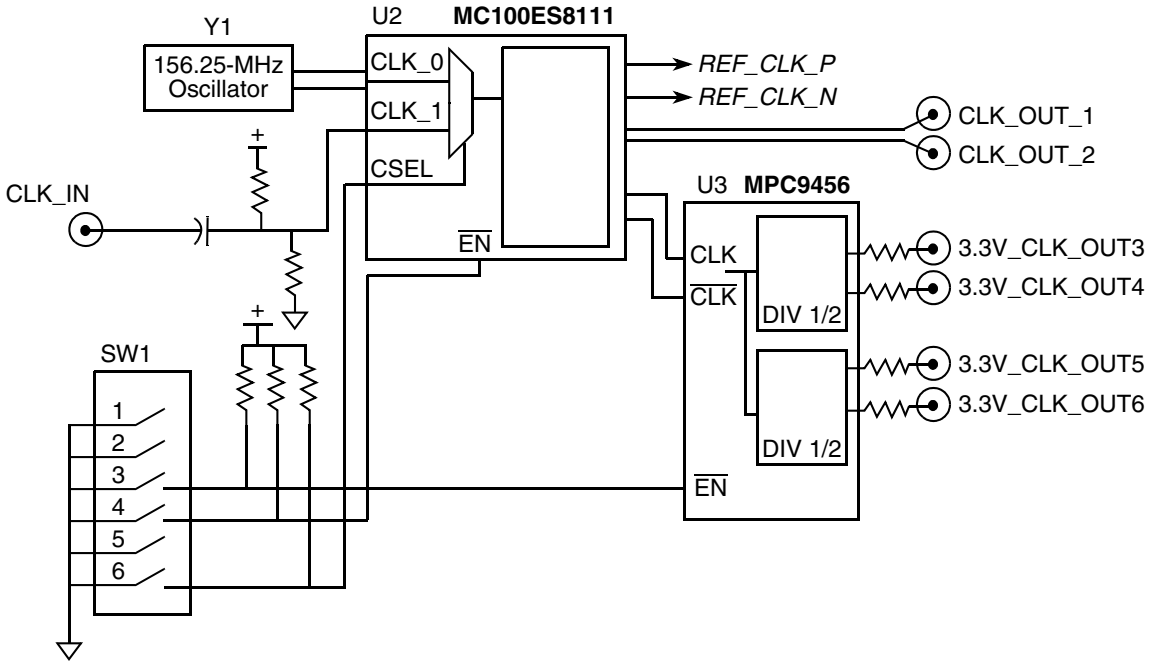


Figure 2-2. MC92610DVB Clock Circuitry

The input reference clock, from either the onboard oscillator or an external source, is applied to the MC100ES8111 clock buffer. Its outputs are differential low-voltage, +1.5-V HSTL signals. These signals drive the MC92610 reference clock inputs, REF_CLK_P and REF_CLK_N, two SMA connectors for triggering other equipment, 1.5V_CLK_OUT1 and 1.5V_CLK_OUT2, and the inputs of the second clock buffer MPC9456. The outputs of the MPC9456 are single-ended series terminated +3.3-V signals driving four additional SMA connectors, 3.3V_CLK_OUT3, 3.3V_CLK_OUT4, 3.3V_CLK_OUT5, and 3.3V_CLK_OUT6. These connections provide board synchronized trigger signals for use with laboratory equipment.

2.4.1 Using the Onboard Oscillator

The crystal oscillator is socketed on the board (not soldered) to allow the user to easily change frequencies by swapping in crystal oscillators with other values. The default reference clock frequency oscillator supplied with the board is 156.25 MHz. Crystal oscillators used with this board should have +3.3-V complementary PECL outputs capable of driving lines terminated with 50 Ω. These types of crystal oscillators are available from external vendors in a variety of frequencies. For a listing of recommended crystal oscillators refer to Appendix C, "Crystal Oscillator Vendors."

When selecting reference oscillators or external reference frequencies, only those frequencies listed in the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide* are considered valid. Freescale does not guarantee operation of the MC92610 at frequencies other than those listed in the user's Guide. DIP switch settings select either the onboard oscillator or the external reference, as well as enable the clock buffer chips.

2.4.2 External Reference Clock Source

To supply an external reference clock, switch number 6 on SW1 must be set to the 'off' position. The user must then supply a 1.0 Vp-p input clock through the CLK_IN SMA connector. This input is AC coupled on the board and, therefore, does not require any DC biasing of the input signal. After the AC coupling, the CLK_IN input is terminated with a 50-Ω impedance. This input clock is buffered by the MC100ES8111 and level translated from PECL to HSTL. It provides REF_CLK_P, _N inputs of the MC92610, and the 1.5V_CLK_OUT1 and 1.5V_CLK_OUT2 SMA connectors. Switch number 4 on SW1 must be set to the 'on' position to enable the outputs of the MC100ES8111.

NOTE

The outputs of the MCP100ES8111 expect to see a DC 50-Ω path to ground. Therefore, if a DC blocker is being used with the 1.5V_CLK_OUT1 or 1.5V_CLK_OUT2 outputs as a trigger or signal to an oscilloscope, a 50-Ω feed through termination must be placed in line before the DC blocker before the attachment to the oscilloscope. A 3dB attenuator may be used in place of the 50-Ω feed through termination. See Section 3.2.1.1, "Equipment Setup," for an example oscilloscope setup.

2.4.3 3.3V_CLK_OUT*n* SMA Connectors

Four single-ended, 3.3-V level clock signals are available on SMA connectors to drive other instruments. Between the MC100ES8111 output and the four SMAs, is an MPC9456 that performs a differential HSTL to a single-ended +3.3-V LVTTL/CMOS level shift. These CMOS outputs are series terminated on the board and connected to the SMA connectors labeled 3.3V_CLK_OUT3, 3.3V_CLK_OUT4, 3.3V_CLK_OUT5, and 3.3V_CLK_OUT6. All of the MPC9456 outputs can be disabled by setting the DIP switch SW1, switch 7 to the ‘off’ position.

Figure 2-3 depicts the switch settings for using an onboard oscillator with all of the clock buffer outputs enabled.

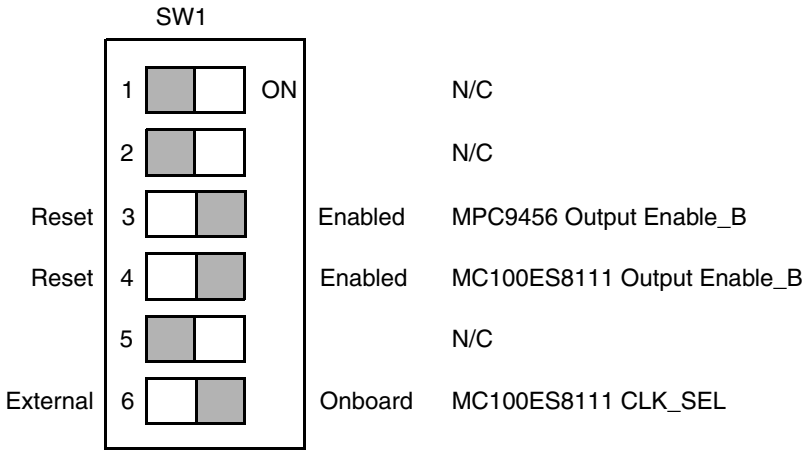


Figure 2-3. Switch Settings for Using the Onboard Oscillator

2.5 Interface Components

The following sections list the descriptions of the MC92610DVB interface connector components.

2.5.1 Parallel Inputs and Outputs

The MC92610 parallel I/O is supplied by the +1.5-V (HSTL) V_{DDQ} voltage regulator (set for 1.5 or 1.8 V) and has a rail-to-rail signal swing. There are no bidirectional signals on the MC92610 or the design verification board.

2.5.1.1 Parallel Inputs

The parallel inputs, both data and control, are accessible through 2×10, 0.100" connectors. Figure 2-4 depicts the 2×10, 0.100" connector numbering scheme, with pin 1 being labeled on the board. A complete mapping of the MC92610 inputs to the 2×10, 0.100" connectors is listed in Appendix A, "Connector Signals." Note that all even number pins are connected to ground.

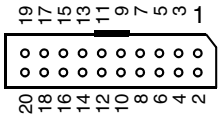


Figure 2-4. 2×10, 0.100" Input Connector Numbering Scheme (Top View)

For a description of the input functionality of the MC92610, refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*.

2.5.1.2 Parallel Outputs

All parallel outputs, both data and status bits, are present at four 2×20, 0.100" connectors. Figure 2-5 depicts the 2×20, 0.100" output connector numbering scheme, with pin 1 labeled on the board. The parallel output signals of the MC92610 are 1.5- or 1.8-V HSTL compatible depending on the setting of the V_{DDQ} regulator. A complete mapping of the MC92610 outputs to the 2×20, 0.100" connectors is listed in Appendix A, "Connector Signals." Note that all even number pins are connected to ground.

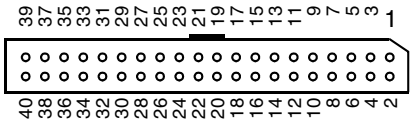


Figure 2-5. 2×20, 0.100" Output Connector Number Scheme (Top View)

For information regarding the MC92610 outputs, refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*.

2.5.2 +V_{DDQ} and Ground (GND) Access Connections

The MC92610DVB also has two 2×8, 0.100" connectors, PG12 and PG14, with dedicated connections to the +1.5-V V_{DDQ} and ground planes. These are useful for biasing parallel input signals using jumper cables. The odd number pins (1, 3, 5, and 7) are connected to the V_{DDQ} plane. The even number pins (2, 4, 6, and 8) are connected to the ground (0.0-V) plane.

2.5.3 Receiver Interface Status LEDs

The state of the three parallel receiver bus status bits, RECV_*x*_ERR, RECV_*x*_K, and RECV_*x*_IDLE, are also accessible through the LEDs located next to the receiver parallel output connectors. An illuminated LED corresponds to a logic 'high' signal. Conversely, a non-illuminated LED represents a logic 'low.' For more information about the state of the status bits, refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*.

2.5.4 Serial Inputs and Outputs

All MC92610 high-speed serial differential inputs and differential outputs are connected to appropriately labeled pairs of SMA connectors through board traces with a characteristic impedance of 50 Ω (100-Ω differential). The output driver requires a 50-Ω parallel termination to mid-rail (+0.9 V nominal for +1.8-V supply). If the termination voltage is not +0.9 V, the signal must be AC coupled. There is no AC coupling (DC blocking) of the serial outputs on the board. If needed, AC coupling must be done in-line before any termination.

During all testing, the serial transmitter outputs should be terminated with 50 Ω. This can be done by connecting the serial transmitter outputs to serial receiver inputs, to any laboratory equipment with 50-Ω input impedance through in-line AC coupling, or by terminating the outputs with 50-Ω SMA terminations.

2.6 Special Test Connection

The MC92610DVB also contains an oscilloscope PCB test socket, labeled TPA. When the MC92610 is configured in a PLL factory test mode, this test socket enables special access to the PLL.

NOTE

This test mode is for factory testing purposes only. There are no system applications for this mode, and test socket TPA should remain unconnected at all times.

2.7 Test Traces

The MCS92610DVB design verification board has both vertical and horizontal 50-Ω test traces:

- Vertical: TST1–TST5 and TST2–TST6
- Horizontal: TST3–TST7 and TST4–TST8

These traces can be used to determine the impedance of the board using TDR measurement techniques.

Chapter 3
Laboratory Equipment and Quick Setup Evaluation

This chapter begins with a listing of the recommended test equipment needed to perform complete evaluations on the MC92610. Chapter 4, "Test Setups," covers specific setup configurations for this equipment depending on the desired feature under test. Appendix B, "Parts List," offers various suggested data test patterns that may be used with these test setups.

The quick setup evaluation procedures outlined below describe how the MC92610DVB can be used to evaluate the data 'eye diagram' and a simple error rate test using the internal test features of the MC92610 with a minimal amount of test equipment. Only a power supply and sampling oscilloscope are required.

Details of testing in specific systems is left to the user. For more information regarding the MC92610 feature set, refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*.

3.1 Recommended Laboratory Equipment

Evaluation of the MC92610 feature set is possible using the MC92610DVB evaluation kit in conjunction with several pieces of test equipment. The quick setup evaluations and other tests listed in this guide utilize the basic set of test equipment listed in Table 3-1. Equivalent instrumentation may be substituted. Not all pieces of test equipment are necessary for all tests.

Table 3-1. Recommended Test Equipment

Quantity	Equipment
1	MC92610DVB evaluation kit
1	Tektronix TDS 8000 digital sampling oscilloscope
1	Tektronix 80E04 TDR/sampling head (20 GHz)
3	Tektronix 80E03 sampling heads (20 GHz)
1	Hewlett-Packard HP16700 logic analysis system
5	Hewlett-Packard HP16522A pattern generators
2	Hewlett-Packard HP16557D logic analyzers
1	Hewlett Packard HP6624A system DC power supply

Table 3-2 lists the laboratory accessories.

Table 3-2. Lab Accessories

• SMA male each end coax patch cords, lengths: various • SMA 3-dB attenuators • SMA 6-db attenuators • SMA DC blockers (AC couplers) • 50-Ω SMA terminations (to ground) • SMA 50-Ω feed through terminations • 5/16" torque wrench (fits SMA, 2.9- and 3.5-mm connectors) • Bias-T networks • Power splitters • BNC to SMA adapters • SMA female to SMA female adapters • SMA male to SMA male adapters

In-depth testing of the MC92610 can be performed using a bit error rate tester and a jitter analysis system. Table 3-3 provides a listing of test equipment that can be used for these types of tests.

Table 3-3. Jitter Analysis Test Equipment

Quantity	Equipment
1	Agilent 71500C jitter analysis system
1	HP 70820A microwave transition analyzer
1	HP 70004A display
1	HP 3325B synthesizer/function generator
1	HP 83752A synthesized sweeper
1	HP 86130A BitAlyzer (serial bit error rate tester)
1	HP 70874C jitter personality card
2 each	Assorted bandpass filters
1	Rohde and Schwarz SMIQ-04B signal generator
1	Agilent HP 6624A system DC power supply
1	Agilent 11636B power splitter
1	Divide-by-xx prescalers

3.2 Quick Setup Data-Eye Diagram

The MC92610DVB design evaluation kit comes equipped to immediately demonstrate two of the MC92610 functions:

- Data-eye signal generation and observation
- Bit error rate checking using internal built-in self-test (BIST) features

3.2.1 Quick Setup Data-Eye Generation and Observation

A transmitted data-eye can be observed at either of the serial outputs of the MC92610 using its integrated, 23rd order, pseudo-noise (PN) pattern generator. The implementation of the 23-bit PN generator uses one of the two following polynomials. (Polynomial selection depends on the state of BIST_MODE_SEL.)

$f = 1 + x^5 + x^{23}$ (BIST_MODE_SEL = 0)

or

$f = 1 + x^{18} + x^{23}$ (BIST_MODE_SEL = 1)

Stimulus from this generator is 8B/10B encoded and may also be used for further system testing. Refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide* for additional information.

3.2.1.1 Equipment Setup

Generation and observation of the data-eye produced by the on-chip PN generator requires only the MC92610DVB, a power supply, a high-speed digital sampling scope, 0.100" shunts, and single-pin receptacle patch cords. The shunts and patch cords are provided with the MC92610DVB evaluation kit.

The MC92610DVB and test equipment should be connected as shown in Figure 3-1. Configure clock circuits with SW1 as shown in Figure 2-3.

NOTE

All unconnected serial transmitter outputs should be terminated to 50 Ω. This can be done by connecting the serial transmitter outputs to the serial receiver inputs or to 50-Ω SMA terminations through in-line AC coupling (DC blocking).

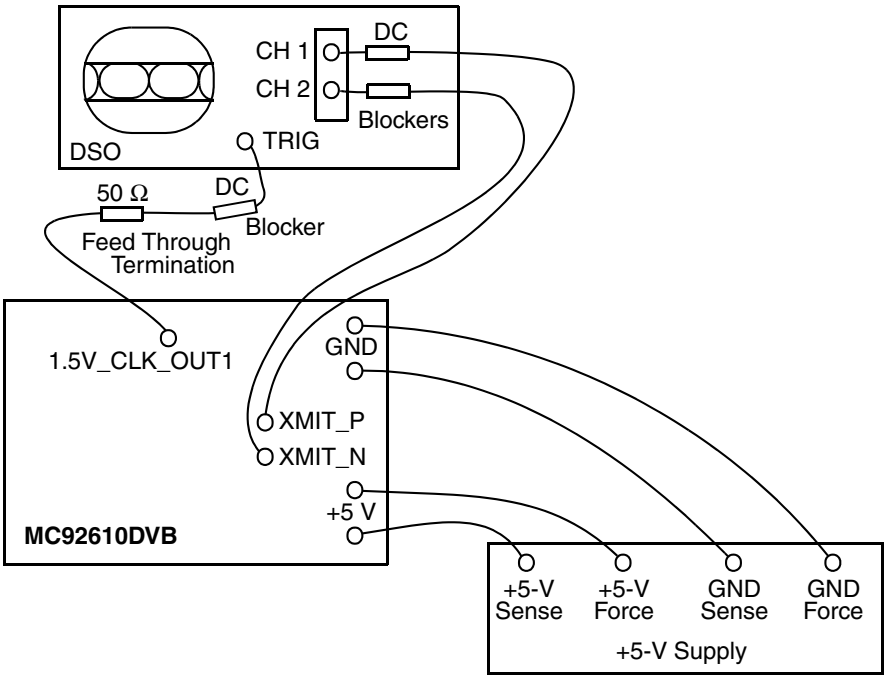


Figure 3-1. Data-Eye Observation Setup

3.2.1.2 Parallel Input Connections

The basic eye diagram will be generated by biasing the parallel inputs according to Table 3-4. Ground connections can be made using the 0.100" shunts. Connections to V_{DDQ} can be made using the square pin receptacle patch cords and jumpering to the odd number pins of headers PG12 and PG14. The shunts and patch cords are provided with the MC92610DVB kit. All even number pins on the connector headers are connected to the board's ground plane. All unlisted pins are not connected.

Table 3-4. Data-Eye Generation Parallel Input Biasing

Pin	Signal	Bias Level	Pin	Signal	Bias Level	Pin	Signal	Bias Level
	CTRL_SIG_0			A_XMIT0			A_XMIT1	
1	REPE	GND	1	XMIT_A_0	GND	1	XMIT_A_K	+1.5 V
3	RCCE	+1.5 V	3	XMIT_A_1	GND	3	$\overline{\text{XMIT\_A\_IDLE}}$	GND
5	WSE	GND	5	XMIT_A_2	GND	5	XCVR_A_DISABLE	GND
7	HSE	GND	7	XMIT_A_3	GND	7	XCVR_A_RSEL	GND
9	ADIE	GND	9	XMIT_A_4	GND	9	XMIT_A_CLK	GND
11	$\overline{\text{RESET}}$	GND	11	XMIT_A_5	GND	11	—	N/C
13	DDRE	+1.5 V	13	XMIT_A_6	GND	13	—	N/C
15	—	N/C	15	XMIT_A_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C

Table 3-4. Data-Eye Generation Parallel Input Biasing (continued)

Pin	Signal	Bias Level	Pin	Signal	Bias Level	Pin	Signal	Bias Level
	CTRL_SIG_1			B_XMIT0			B_XMIT1	
1	LBOE	GND	1	XMIT_B_0	GND	1	XMIT_B_K	+1.5 V
3	LBE	GND	3	XMIT_B_1	GND	3	$\overline{\text{XMIT\_B\_IDLE}}$	GND
5	—	N/C	5	XMIT_B_2	GND	5	XCVR_B_DISABLE	GND
7	TBIE	GND	7	XMIT_B_3	GND	7	XCVR_B_RSEL	GND
9	LME	GND	9	XMIT_B_4	GND	9	XMIT_B_CLK	GND
11	XMIT_EN_ALL	GND	11	XMIT_B_5	GND	11	—	N/C
13	XMIT_EQ_EN	+1.5 V	13	XMIT_B_6	GND	13	—	N/C
15	XMIT_REF_A	GND	15	XMIT_B_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C
	CTRL_SIG_2			C_XMIT0			C_XMIT1	
1	BSYNC	+1.5 V	1	XMIT_D_0	GND	1	XMIT_C_K	+1.5 V
3	DROP_SYNC	GND	3	XMIT_D_1	GND	3	$\overline{\text{XMIT\_C\_IDLE}}$	GND
5	TST_1	GND	5	XMIT_D_2	GND	5	XCVR_C_DISABLE	GND
7	TST_0	+1.5 V	7	XMIT_D_3	GND	7	XCVR_C_RSEL	GND
9	BIST_MODE_SEL	GND	9	XMIT_D_4	GND	9	XMIT_C_CLK	GND
11	WSI	+1.5 V	11	XMIT_D_5	GND	11	—	N/C
13	RECV_EQ_EN	+1.5 V	13	XMIT_D_6	GND	13	—	N/C
15	RECV_REF_A	GND	15	XMIT_D_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C
	TEST_0			D_XMIT0			D_XMIT1	
1	—	N/C	1	XMIT_D_0	GND	1	XMIT_D_K	+1.5 V
3	—	N/C	3	XMIT_D_1	GND	3	$\overline{\text{XMIT\_D\_IDLE}}$	GND
5	—	N/C	5	XMIT_D_2	GND	5	XCVR_D_DISABLE	GND
7	SCAN_EN	GND	7	XMIT_D_3	GND	7	XCVR_D_RSEL	GND
9	TDI	GND	9	XMIT_D_4	GND	9	XMIT_D_CLK	GND
11	TCK	GND	11	XMIT_D_5	GND	11	—	N/C
13	TMS	GND	13	XMIT_D_6	GND	13	—	N/C
15	$\overline{\text{TRST}}$	GND	15	XMIT_D_7	GND	15	—	N/C
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C

3.2.2 Basic Eye Observation—Test Procedure

1. Connect the MC92610DVB and test equipment as described in Figure 3-1. and Table 3-4. This will place the MC92610 in PN generation mode with the MC92610 in reset.

Steps 2 and 3 may be skipped if they were previously performed when setting up the DVB.

2. Apply +5.0 V to the evaluation board. Verify voltage levels of +3.3 V, +1.8 V, and +V_{DDQ} (1.5 V) regulators at connectors T10, T7, and T6, respectively. If necessary, adjust R12V, R22V, and R22V1 to obtain the desired voltage levels.
3. Verify that the reference clock frequency at CLK_OUT1 is 156.25 MHz (period = 6.4 ns).
4. Observe XMIT_*x*_P or XMIT_*x*_N output. Since the chip is in reset, the transmitter should show a constant output level at ground, and the status LEDs should indicate that the receiver is in startup, LEDs RECV_*x*_ERR and RECV_*x*_K are on, and LED RECV_*x*_IDLE is off.
5. Connect $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a V_{DDQ} access connection. This releases the $\overline{\text{RESET}}$ signal.
6. Observe XMIT_*x*_P or XMIT_*x*_N. The transmitter should now be outputting random data. Setting the digital sampling oscilloscope to infinite persistence mode will display a data-eye. An example of a data-eye is shown in Figure 3-2.

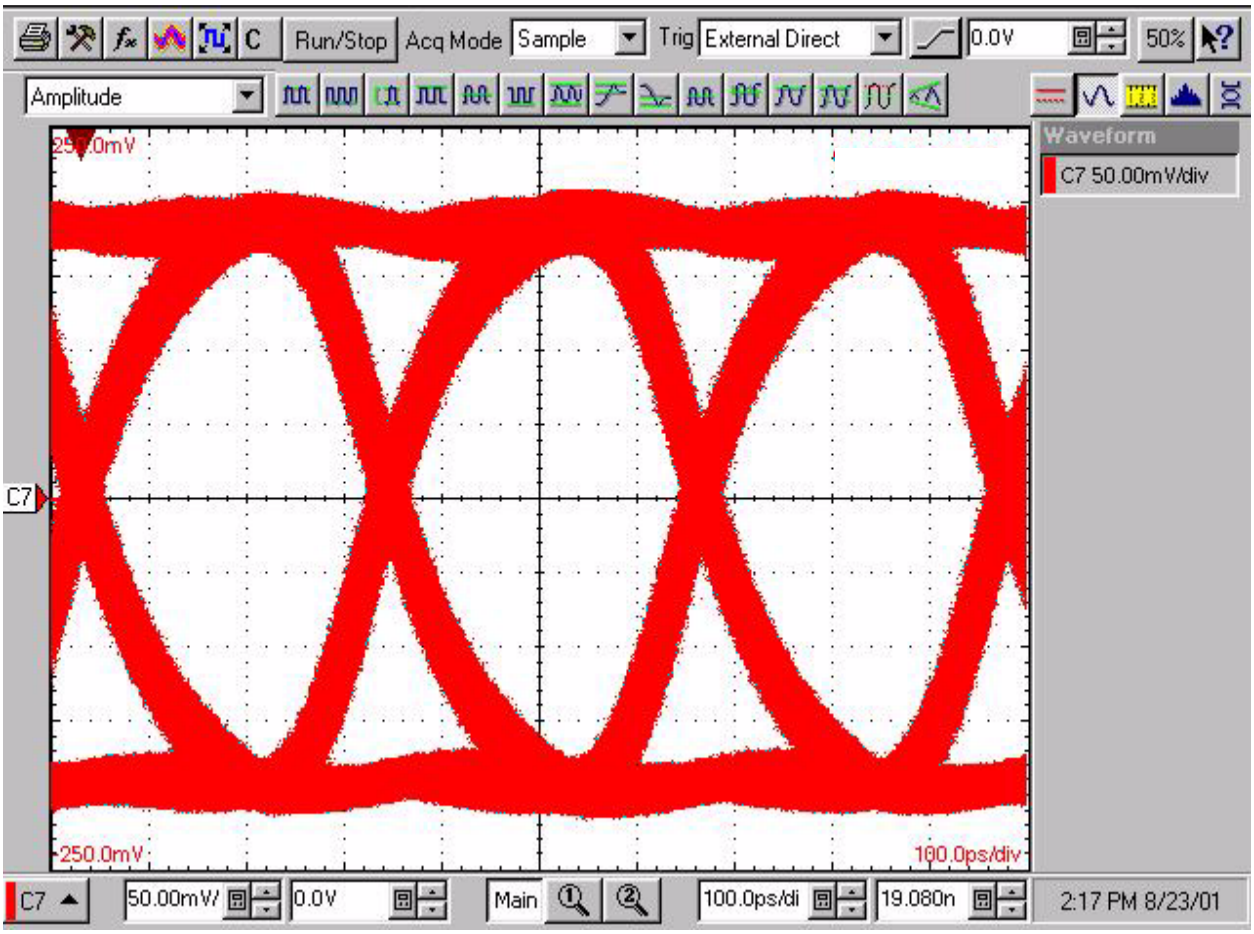


Figure 3-2. MC92610 Data-Eye Using Recommended Test Setup

3.2.3 Quick Setup Bit Error Rate Checking

In addition to having an integrated PN generator, the MC92610 also has a bit error rate checker (BERC). An integrated 23rd order signature analyzer that is synchronized to the incoming PN stream is used to count code group mismatch errors relative to the internal PN reference pattern. The following test procedure will describe how to use this BIST feature. For more information concerning the MC92610 BIST, refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*.

3.2.3.1 Equipment Setup

Connect the MC92610DVB as shown in Figure 3-3. by connecting the transmitter outputs of the link under test (XLINK_*x*_P/N) to the receiver under test (RLINK_*x*_P/N).

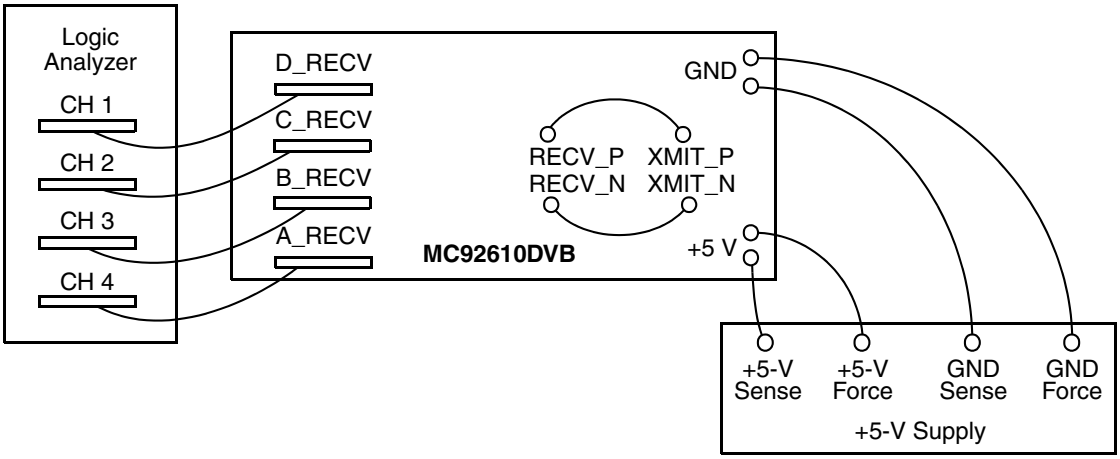


Figure 3-3. Bit Error Rate Check Test Setup

3.2.3.2 Parallel I/O Connections

The bias connections for the parallel inputs to perform the quick setup BERC test are the same as those for the quick setup eye diagram and shown in Table 3-4.

The parallel outputs are connected to a data analysis system. For a simple quick test, the logic analyzer is not required, since the errors are reported and may be observed on the channel status LEDs.

3.2.3.3 Quick Setup BERC Test Procedure

1. Connect the MC92610DVB and the test equipment as described in Section 3.2.3.1, "Equipment Setup." This will place the MC92610 in PN generation mode with the MC92610 held in reset, and set the receivers to BERC mode using the recovered clock.

Step 2 and 3 may be skipped if previously performed when setting up the DVB.

2. Apply +5.0 V to the evaluation board. Verify voltage levels of +3.3 V, +1.8 V, and +V_{DDQ} (1.5 V) regulators at connectors T10, T7, and T6, respectively. If necessary, adjust R12V, R22V, and R22V1 to obtain the desired voltage levels.
3. Verify that the reference clock frequency at CLK_OUT1 is 156.25 MHz (period = 6.4 ns).

4. Connect $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a +1.5-V V_{DDQ} access connection. This releases the $\overline{\text{RESET}}$ signal.
5. Observe the parallel outputs on the data analyzer and the status LEDs. As described in the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide,* the MC92610 will start and lock its PLL, initialize the receivers, perform byte alignment, and reset its bit error counter.
6. When the receivers are locked and BIST is running, the recovered clock is observable on RECV_*x*_RCLK. See Figure 3-4 for an example of a receiver startup and error detection sequence. The sequence shown in Table 3-5 will occur on each receiver's status outputs observable on the LEDs.

Table 3-5. State Sequence of Receiver

Receiver State		Status Outputs		
		RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_IDLE
1.	Receiver in startup	1	1	0
2.	Receiver byte/word synchronized, PN analyzer not locked	1	0	1
3.	BIST running no PN mismatch this character	0	0	0

7. Once the receiver has initially locked all receiver data bits, RECV_*x*_[7:0], are set to zero (logic low). Should an error occur, RECV_*x*_[7:0] will increment by one and RECV_*x*_ERR will flag the error during that byte time. The value of RECV_*x*_[7:0] remains constant until another error is detected or the system is reset. If the receiver counter fills with errors, all bits of RECV_*x*_[7:0] stay a logic high (11111111) until the receiver is reset. Refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide* for more detail.

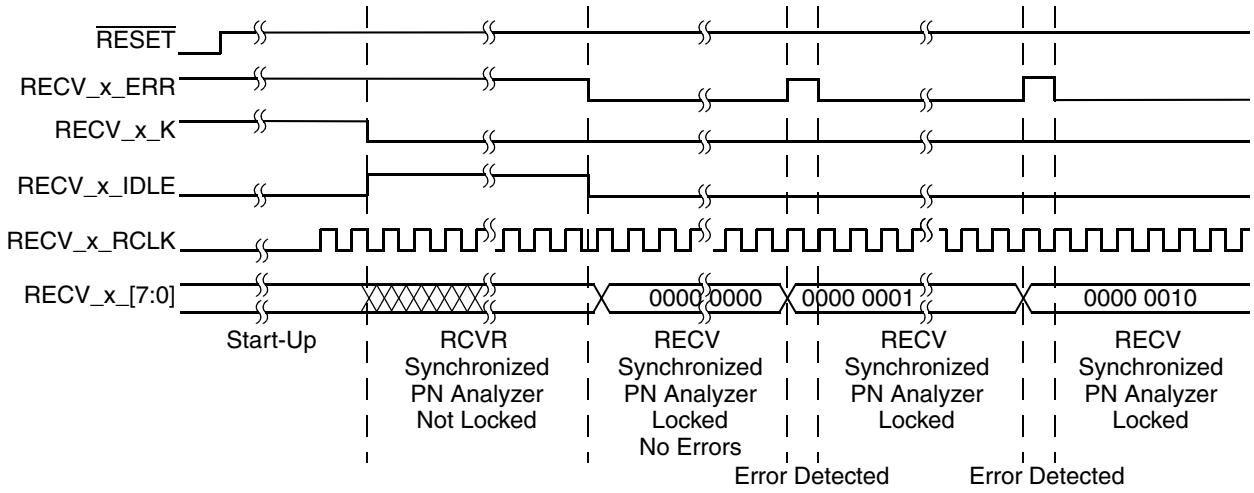


Figure 3-4. Receiver Startup and Error Detection Sequence

Chapter 4
Test Setups

This chapter outlines the laboratory test equipment setup and procedure to evaluate the features of the MC92610 in more depth than those outlined in the previous chapter. These setups are meant to be guidelines only and are not implied to be complete. Details of testing in specific system applications are left to the user.

4.1 Serial Link Verification Using a Serial Bit Error Rate Tester (BERT)

This test setup is used to observe the rate at which the MC92610 produces errors given either pseudo-random (PRBS) patterns or user-defined pattern sets generated by the serial bit error rate tester (BERT). The MC92610 is placed in repeater mode, REPE = high, thereby disabling the parallel receiver and transmitter buses. Testing performed using the ten-bit interface mode does not require the insertion of idle characters for word recognition or byte alignment. If verification using the 8B/10B encoder or other MC92610 features is required, appropriate idle insertion and timing requirements as outlined in the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide* must be followed.

4.1.1 Test Setup for Double Data Rate or Link Multiplex Modes

Figure 4-1 depicts the test setup for MC92610 in double data rate mode (DDRE) or link multiplex mode (LME) The control bits are set as follows:

- DDRE = 1 or LME = 1
- REPE = 1
- XMIT_EQ_EN = 1
- TBIE = 1
- RECV_EQ_EN = 1

All other control bits are set to 0, except $\overline{\text{RESET}}$, which is initially set to 0 and then transitioned to 1 to start the MC92610.

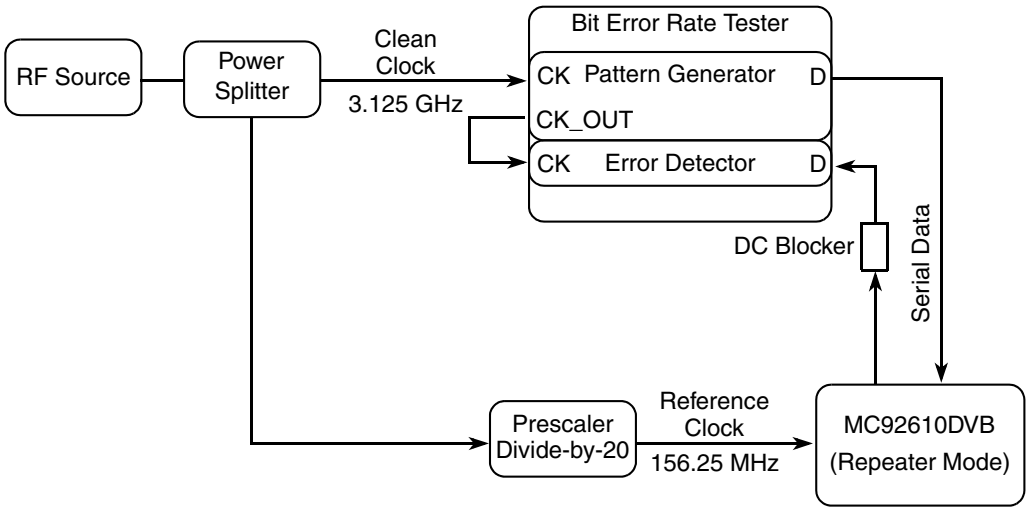


Figure 4-1. DDRE or LME Serial Link Test Setup

4.1.2 Test Setup for Double Data Rate and Link Multiplex Modes

Serial link testing may also be performed using both double data rate mode (DDRE) and link multiplex mode (LME). This reduces the reference frequency required by the MC92610 by a factor of two. Figure 4-2 depicts the serial link test setup for asserting both DDRE and LME and using a divide-by-40 prescaler.

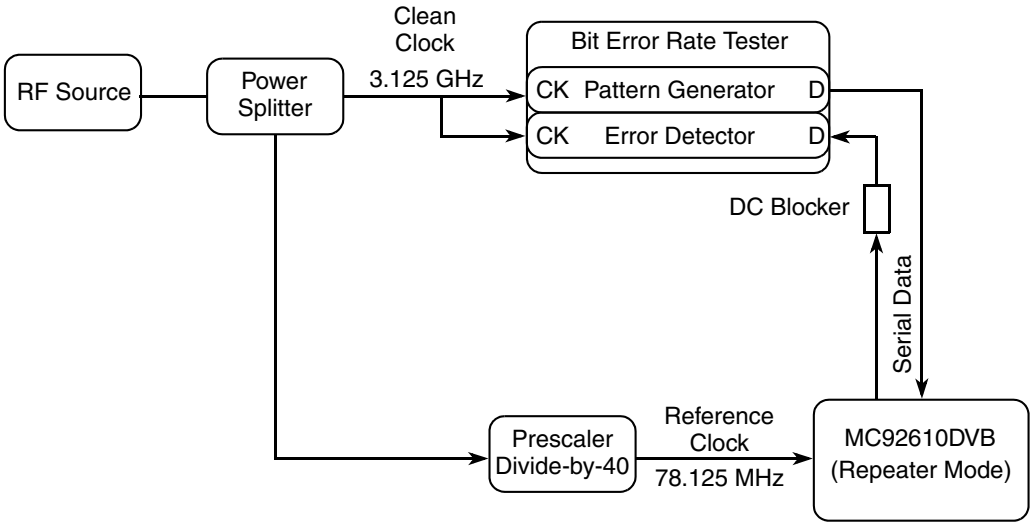


Figure 4-2. DDRE and LME Serial Link Test Setup

4.2 Jitter Testing

The following tests are guidelines for verifying the performance of the MC92610 in ‘noisy’ conditions. Results will vary depending on input reference frequencies, MC92610 mode of operation, test setup and equipment, and test environment.

4.2.1 Jitter Test System Calibration

Before beginning any type of jitter measurement, the system must first be calibrated, as shown in Figure 4-3, to produce the desired frequency and amplitude modulation of the jittered source. The amplitude of modulation is then translated into jitter in units of peak-to-peak unit intervals (UIp-p). Different synthesized sweepers have different characteristics at different frequencies. It is possible for certain frequencies to produce spurious side lobes that will affect jitter characterization. It is strongly advised that a bandpass filter centered on the carrier frequency be used at the input to the microwave transition analyzer. Refer to the synthesized sweeper reference Guide for more details.

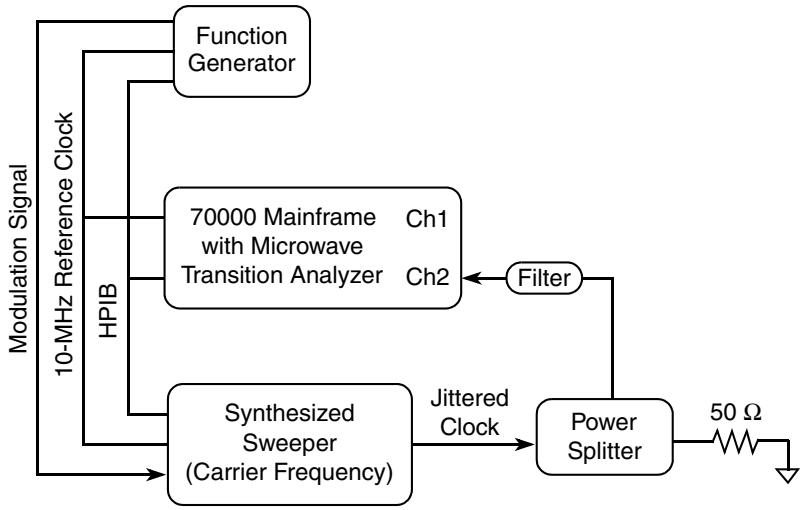


Figure 4-3. Jitter Measurement System Calibration

4.2.2 Reference Clock Jitter Transfer Test

The test setup shown in Figure 4-4 is used to observe the amount of jitter placed on the reference clock that is transferred to the data outputs. Example frequencies were chosen to match narrow bandpass filters available with the Agilent 71500C jitter analysis system. The control bits are set as follows:

- DDRE = 1
- LME = 1
- XMIT_EQ_EN = 1
- TBIE = 1
- RECV_EQ_EN = 1

The parallel data inputs must be set to the pattern shown in Figure 4-4. This data pattern appears as a 622-MHz clock signal at the serial outputs.

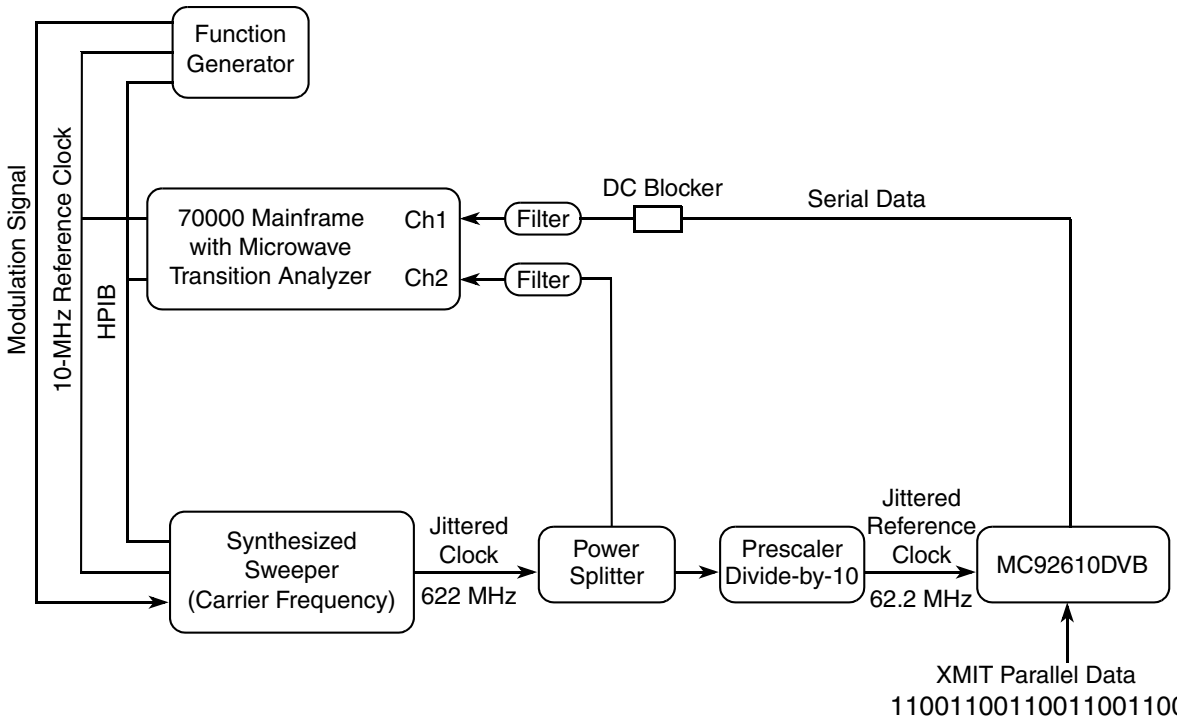


Figure 4-4. Reference Clock Jitter Transfer Test Setup

4.2.3 Reference Clock Jitter Tolerance Test

The test setup shown in Figure 4-5 is used to observe the amount of jitter placed on the reference clock that does not produce errors on the serial data outputs as compared to the input serial data stream. The MC92610 is placed in ten-bit interface mode (TBIE) and repeater mode (REPE). The serial data stream can be set to either PRBS or user-defined data. The control bits are set as follows:

- DDRE = 1
- XMIT_EQ_EN = 1
- REPE = 1
- TBIE = 1
- RECV_EQ_EN = 1

All other control inputs are set to 0.

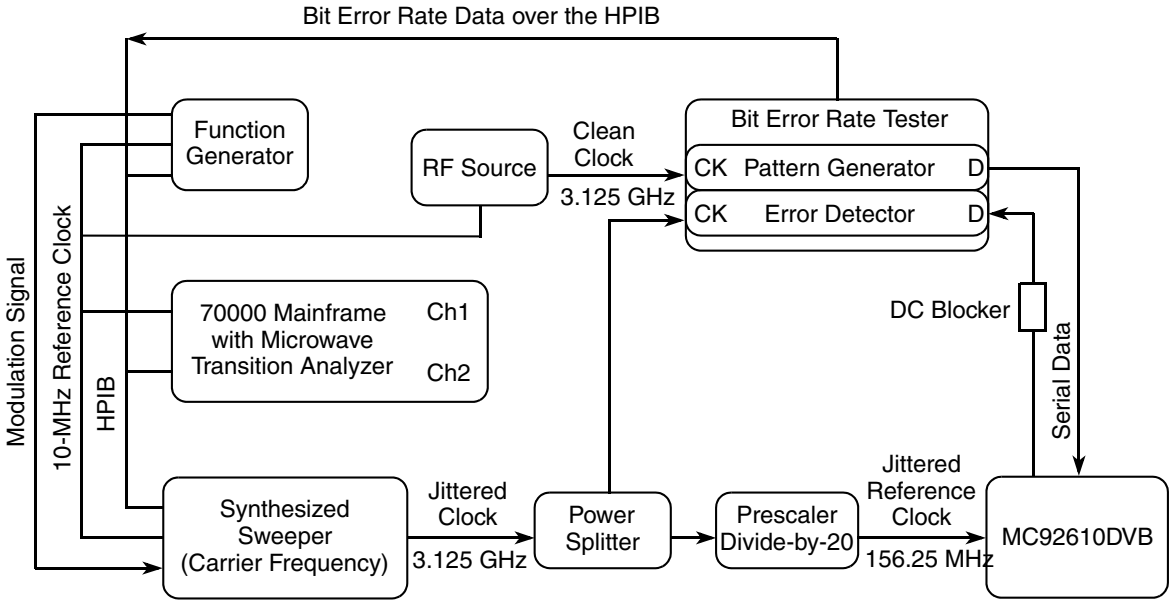


Figure 4-5. Reference Clock Jitter Tolerance Test Setup

4.2.4 Data Jitter Tolerance Test

The test setup shown in Figure 4-6 is used to observe the amount of jitter placed on the serial data inputs that does not produce errors on the serial data outputs. The MC92610 is placed in ten-bit interface mode (TBIE) and repeater mode (REPE). The serial data stream can be set to either PRBS or user-defined data. The control bits are set as follows:

- DDRE = 1
- XMIT_EQ_EN = 1
- REPE = 1
- TBIE = 1
- RECV_EQ_EN = 1

All other control inputs are set to 0.

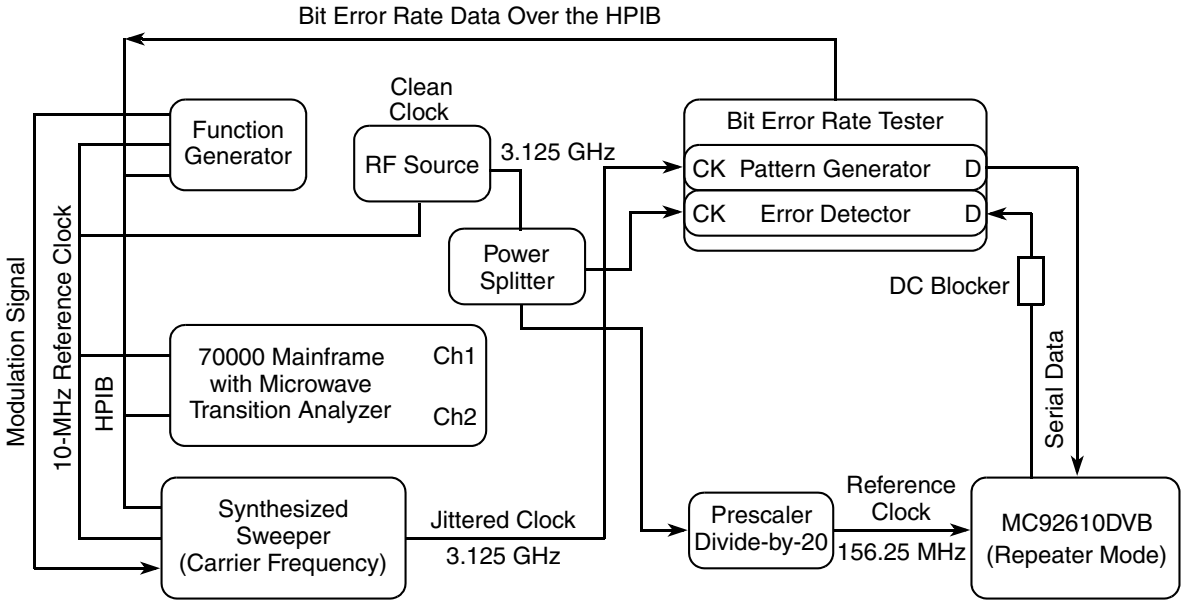


Figure 4-6. Data Jitter Tolerance Test Setup

Appendix A
Connector Signals

The parallel data input and output signals of the MC92610DVB design verification board are listed in the following tables. All the connection test points use the common 2 row 0.100" spaced 3-M type connectors.

A.1 Input: 2×10 (0.100") Connectors

The configuration, control, data, and test inputs to the MC92610 are via 2 row by 10 connectors. There are a total of 12 input connectors on the DVB.

On each connector, the even pin numbers (2, 4, ..., to 20) are connected to the ground plane. The signal inputs (on the odd pin numbers) do not have pull-up resistors on the DVB board. Therefore, if the configuration requires a ‘high’ or logic 1, the pin must be jumper connected to +1.5 V (V_{DDQ}) on the access connectors PG12 or PG14. If the input is required to be ‘low,’ a shorting jumper may be installed. The signal name, description, and MC92610 device ‘ball’ (pin) number are listed in the following tables for each of the input connectors.

A.1.1 Control Signal Input Connectors

The signals on connectors CTRL_SIG_0, CTRL_SIG_1, and CTRL_SIG_2 (PG1–PG3, respectively) are control input signals that set the basic configuration to the MC92610. These signals and corresponding connector pins are listed in Table A-1, Table A-2, and Table A-3, respectively.

Table A-1. CTRL_SIG_0 Connector

Connector Pin	MC92610 Pin	Input Signal Name	Description
1	C11	REPE	Repeater mode enable
3	D11	RCCE	Recovered clock enable
5	D10	WSE	Word synchronization enable
7	C13	HSE	Half-speed mode enable
9	E10	ADIE	Add/drop idle enable
11	T10	RESET	System reset bar
13	B13	DDRE	Double data rate enable
15	N/C	—	—
17	N/C	—	—
19	N/C	GND	Ground connection

Table A-2. CTRL_SIG_1 Connector

Connector Pin	MC92610 Pin	Input Signal Name	Description
1	B11	LBOE	Loopback output enable
3	B12	LBE	Loopback enable
5	N/C	—	—
7	V10	TBIE	Ten-bit interface enable
9	D12	LME	Link multiplex enable
11	C12	XMIT_EN_ALL	Transmitter link broadcast enable
13	U14	XMIT_EQ_EN	Transmit equalization enable
15	U12	XMIT_REF_A	Transmit reference clock A select
17	N/C	—	—
19	N/C	GND	Ground connection

Table A-3. CTRL_SIG_2 Connector

Connector Pin	MC92610 Pin	Input Signal Name	Description
1	R10	BSYNC	Byte synchronization mode
3	V8	DROP_SYNC	Drop synchronization
5	U9	TST_1	Test mode—select 1
7	T9	TST_0	Test mode—select 0
9	R9	BIST_MODE_SEL	Selects PRBS pattern
11	B4	WSI	Word synchronization bus input
13	R12	RECV_EQ_EN	Receiver equalization enable
15	T12	RECV_REF_A	Receiver reference clock A select
17	N/C	—	—
19	N/C	GND	Ground connection

A.1.2 Transmitter Parallel Data Input Connectors

The MC92610 parallel transmitter data input signals for channels A through D are mapped to the 2×10 connectors as listed in the tables below. Table A-4 shows the 8-bit data byte input for transmitter channels A through D, respectively, on connectors A_XMIT0–D_XMIT0 (PG8, PG10, PG6, and PG4).

Table A-4. A_XMIT0, B_XMIT0, C_XMIT0, and D_XMIT0 Connectors

Connector Pin No.	MC92610 Ball No.				Input Signal Name	Description
	A_XMIT0, (CH A)	B_XMIT0, (CH B)	C_XMIT0, (CH C)	D_XMIT0, (CH D)		
1	T6	R6	D9	B7	XMIT_*x*_0	Transmitter *x*, data input bit 0
3	U6	V5	E8	C8	XMIT_*x*_1	Transmitter *x*, data input bit 1
5	R7	U5	B6	A7	XMIT_*x*_2	Transmitter *x*, data input bit 2
7	P8	T5	C7	B8	XMIT_*x*_3	Transmitter *x*, data input bit 3
9	T7	U4	D7	C9	XMIT_*x*_4	Transmitter *x*, data input bit 4
11	R8	R5	B5	E9	XMIT_*x*_5	Transmitter *x*, data input bit 5
13	P9	T4	A4	A8	XMIT_*x*_6	Transmitter *x*, data input bit 6
15	T8	R4	C5	B9	XMIT_*x*_7	Transmitter *x*, data input bit 7
17	N/C	N/C	N/C	N/C	—	—
19	N/C	N/C	N/C	N/C	GND	Ground connection

Table A-5 lists the remaining transmitter input signals for the four channels on connectors A_XMIT–D_XMIT_1 (PG9, PG11, PG7, and PG5), respectively.

Table A-5. A_XMIT1, B_XMIT1, C_XMIT1, and D_XMIT1 Connectors

Connector Pin No.	MC92610 Ball No.				Input Signal Name	Description
	A_XMIT1, (CH A)	B_XMIT1, (CH B)	C_XMIT1, (CH C)	D_XMIT1, (CH D)		
1	U8	V3	D6	A9	XMIT_*x*_K	Transmitter *x*, special character (data bit 8 for ten-bit mode)
3	V9	U3	C6	C10	XMIT_*x*_IDLE	Transmitter *x*, Idle enable bar (data bit 9 for ten-bit mode)
5	D13	C14	B14	A14	XCVR_*x*_DISABLE	Transceiver *x*, disable
7	P11	U13	T13	P12	XCVR_*x*_RSEL	Transceiver *x*, redundant link select
9	U7	V4	D8	B10	XMIT_*x*_CLK	Transmitter *x*, interface clock
11	N/C	N/C			—	—
13	N/C	N/C			—	—
15	N/C	N/C			—	—
17	N/C	N/C			—	—
19	N/C	N/C			GND	Ground connection

A.2 Output: 2×20 (0.100") Connectors

The MC92610 receiver parallel data outputs are connected to 2×20, 0.100" connectors. A mapping of these signals is shown in Table A-6.

Table A-6 lists the signals for the A_RECV, B_RECV, C_RECV, and D_RECV (LA1–LA4, respectively) connectors. Note that the receive data clock, RECV_*x*_RCLK, is brought out to two connector pins. Care should be exercised when connecting to both these pins not to exceed the drive capacity of the chip output. Refer to the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*, for more details.

Table A-6. A_RECV and B_RECV Connectors

Connector Pin No.	MC92610 Ball No.				Output Signal Name	Description
	A_RECV, (CH A)	B_RECV, (CH B)	C_RECV, (CH C)	D_RECV, (CH D)		
1	N/C	N/C	N/C	N/C	—	—
3	P5	K3	H2	D4	RECV_*x*_CLK	XCVR_ *x*, receive data clock
5	N/C	N/C	N/C	N/C	—	—
7	P5	K3	H2	D4	RECV_*x*_CLK	XCVR_ *x*, receive data clock
9	N/C	N/C	N/C	N/C	GND	Ground connection
11	N/C	N/C	N/C	N/C	GND	Ground connection
13	C4	R11	N/C	N/C	For channel A this pin is WSO, (word sync. output). For channel B this pin is TDO (JTAG, test data out). For channels C and D this pin is GND.	
15	V2	J1	J2	A3	RECV_*x*_ERR	Receiver x, error detect
17	U2	K4	H1	A2	RECV_*x*_IDLE	Receiver x, $\overline{\text{Idle}}$ detect
19	P4	K2	H3	C3	RECV_*x*_ 9	Receiver x, data bit 9 for TBI mode
21	T3	L2	J4	D5	RECV_*x*_K	Receiver *x*, special character (data bit 8 in TBI mode)
23	T2	L3	G1	A1	RECV_*x*_7	Receiver *x*, data bit 7
25	T1	M1	G2	B2	RECV_*x*_6	Receiver *x*, data bit 6
27	N4	M2	H4	C2	RECV_*x*_5	Receiver *x*, data bit 5
29	M4	M3	F1	D3	RECV_*x*_4	Receiver *x*, data bit 4
31	R3	N1	F2	D2	RECV_*x*_3	Receiver *x*, data bit 3
33	R1	N3	F3	D1	RECV_*x*_2	Receiver *x*, data bit 2
35	P3	L4	G4	E3	RECV_*x*_1	Receiver *x*, data bit 1
37	P2	P1	E1	E2	RECV_*x*_0	Receiver *x*, data bit 0
39	N/C	N/C	N/C	N/C	—	—

A.3 TEST_0 Connector

Table A-7 lists the signals for the connector TEST_0 (PG13). This is the MC92610 test access port (TAP) interface for IEEE Std 1149 JTAG testing.

NOTE

There are no internal pull ups/pull downs on any of the MC92610 JTAG inputs. These pins should all be shunted to ground on the TEST_0 connector.

For more information on the test access port, see Section 5.1 in the *MC92610 Quad 3.125 Gbaud SerDes Reference Guide*, for more details.

Table A-7. TEST_0 Connector

Connector Pin	MC92610 Pin	Input Signal Name	Description
1	N/C	—	—
3	N/C	—	—
5	N/C	—	—
7	U10	SCAN_EN	Test mode, scan shift enable (for factory use only)
9	U11	TDI	JTAG test data in
11	V12	TCK	JTAG test clock
13	V11	TMS	JTAG test mode select
15	T11	TRST	JTAG test reset bar
17	N/C	—	—
19	N/C	GND	Ground connection

Appendix B
Parts List

B.1 Design Verification Board Parts List

Table B-1 shows the parts used in constructing the MC92610DVB design verification board.

Table B-1. MC92610DVB Design Verification Board Parts List (Sheet 1 of 3)

Item	Qty.	Reference	Value	Manufacturer	Manufacturer's Part No.	Description
1	15	C1, C24, C30–C33, C54–C57, C208–C210, C303–C304	1 µF	Bourns	C1812C105K5RAC	Ceramic chip capacitor, 1 µF, size 1812
2	3	C4, C11, C21	100 µF	Kemet	T495X107K010AS	100-µF solid tantalum chip capacitor, low ESR, 10 V, size 7343
3	5	C5, C13, C12, C22–C23	10 µF	Kemet	T495X106K035AS	10-µF solid tantalum chip capacitor, low ESR, 35 V, size 7343H
4	3	C6, C16, C17	100 pF		C0805C101J1GAC	Ceramic chip capacitor, 100 pF, size 0805
5	5	C3, C10, C20, C18, C19	0.1 µF	Kemet	C0805X7R500-104KNE	Ceramic chip capacitor, 0.1 µF, size 0805
6	37	C2, C7–C9, C14–C15, C25, C26, C34–C53, C201–C207, C301–302	0.01 µF	Kemet	C0805X7R500-103KNE	Ceramic chip capacitor, 0.01 µF, size 0805
7	1	Y1	156.25 MHz	Connor-Winfield	EE14-521-156.25M	156.25-MHz through-hole, 14-pin DIP crystal oscillator
8	1	SW1	N/A	Omron	A6S-6104	6-pole DIP slide switches, 2 positions (open or closed), surface mount
9	2	PG12, PG14	N/A	3M	2516-6002UB	2×8 keyed header with shroud, 0.1" pin spacing, low profile
10	12	PG1–PG11, PG13	N/A	3M	3428-6002UB	2×10 keyed header with shroud, 0.1" pin spacing

Table B-1. MC92610DVB Design Verification Board Parts List (Sheet 2 of 3)

Item	Qty.	Reference	Value	Manufacturer	Manufacturer's Part No.	Description
11	4	LA1–LA4	N/A	3M	2540-6002UB	2×20 keyed header with shroud, 0.1" pin spacing, low profile
12	13	D1–D13	N/A	Dialight	597-5311-402	Green LED surface mount
13	3	VR15, VR18, VR33	N/A	Linear Technology	LT1587CM	Linear voltage regulator, 3-ampere, 3-lead DD pak
14	1	U3	N/A	Freescale	MPC9456A	3.3-V clock buffer 32-pin gull wing LQFP
15	1	U2	N/A	Freescale	MC100ES8111	Level shift and clock buffer, 32-pin gull wing TQFP
18	9	T1–T8, T10	N/A	SPC Technology	2304/2303/ 9648/9649/9650	4-mm screw terminal binding post, red/black/ yellow/blue/green
19	2	U4, U5	N/A	Texas Instruments	SN74HSTL16919DGGR or SN74HSTL16918DGGR	Memory address latch (used as +1.8 to +3.3-V buffer/level shift) TSOP package
20	6	R5–R6, R9, R12, R23, R25	82 Ω	SPC/ Multicomp	CR16B820JT	82-Ω chip resistor, size 0603
21	7	R3, R4, R10, R15, R20, R22, R31	124 Ω	Dale	CRCW08051240FT	124-Ω chip resistor, size 0805
22	2	R13, R11	330 Ω	Welwyn	WCR0805330RG	330-Ω chip resistor, size 0805
23	1	R21	68 Ω	Dale	CRCW0805-10W680JT	68-Ω chip resistor, size 0805
24	13	R14, R43–R54	120 Ω	Dale	CRCW08051200FRT1	120-Ω chip resistor, size 0805
25	12	R2, R8, R16–R19, R27, R61–R65	0 Ω	Dale	CR0805-10W-000T	0-Ω chip resistor, size 0805
26	1	R26	100 Ω	Dale	CRCW08051000FT-X	100-Ω chip resistor, size 0805
27	3	R33, R94, R95	1 Ω	Dale	CRCW12061R0JT	1.0-Ω chip resistor, size 1206
28	1	TPA	N/A	Johnson	129-0701-202	Scope PCB test socket
29	47	CLK_IN, CLK_OUT1–CLK_OUT6, SMA1–SMA32, TST1–TST8	N/A	Amp	901-144-8-RFX	SMA 50-Ω RF PCB jack socket

Table B-1. MC92610DVB Design Verification Board Parts List (Sheet 3 of 3)

Item	Qty.	Reference	Value	Manufacturer	Manufacturer's Part No.	Description
30	1	R12V	1 KΩ	BOURNS	3214W-1-102E	Surface mount trimming resistor, J lead
31	3	R22V, R22V1, R22V3	500 Ω	BOURNS	3214W-1-501E	Surface mount trimming resistor, J lead
32	1	U1	N/A	Freescale	MC92610VF	Quad 3.125 Gbaud SerDes
33	70	N/A	N/A	3M	929950-00	0.100" shunts
34	10	N/A	N/A	Pomona	4741-12-0/4741-12-2	Square pin receptacle patch cord
35	2	R42, R68	825 Ω	Panasonic	P825CCT	825-Ω chip resistor, size 0805
36	2	R69, R70	2400 Ω	Dale	CR16B242JT	2400-Ω chip resistor, size 0603
37	1	R66	63.4 Ω	Panasonic	P63.4CCT	63.4-Ω chip resistor, size 0805
38	6	R67, R71, R72, R90–R92	10 KΩ	Dale	CR0805-10W-103J	10-KΩ chip resistor, size 0805
39	1	Y1 socket	N/A		504 - AG11D	14-lead DIP socket for crystal oscillator
40	9	R7, R34, R35, R59, R60, R73–R76	49.9 Ω	Dale	CRCW080549R9FT	49.9-Ω chip resistor, size 0805
41	1	R24	12.1 Ω	Panasonic	P12ACT-ND	12.1-Ω chip resistor, size 0805
42	1	R28	187 Ω	Dale	CRCW0051870FT	187-Ω chip resistor, size 0805

Appendix C
Crystal Oscillator Vendors

C.1 Oscillator Vendors

Table C-1 lists crystal oscillator vendors.

Table C-1. Crystal Oscillators Vendors

Manufacturer	Model Number	Website	Maximum Frequency (MHz)
MF Electronics	M2944	www.mfelectronics.com www.mfelec.com	210
Connor-Winfield		www.conwin.com	160
Champion Technologies		www.champtech.com	200
Mercury		www.mecxtal.com	200
Saronix		www.saronix.com	155.52

Appendix D
Prescaler for Jitter Measurement

D.1 Divide-by-*xx* Prescaler Description

Evaluating jitter in a system requires that all clocks within the system be based on one common source. For this reason, it is often necessary to use prescalers to derive the needed reference clock. Freescale has developed a small programmable prescaler with a maximum input frequency of 4.4 GHz that can be assembled using commercially available parts. Figure D-1 depicts the block diagram of this prescaler.

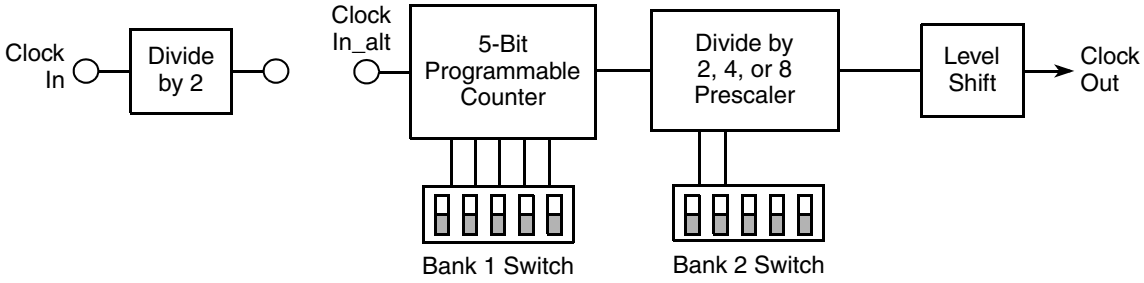


Figure D-1. Divide-by-*xx* Prescaler Block Diagram

The input to the prescaler can be either through a divide-by-2 or directly into the 5-bit programmable counter. The bank 1 and bank 2 DIP switches can be used to select a variety of prescaler values based on the following formula:

$$\text{Modulus} = 2 \cdot (A + 1) \cdot N$$

where A = 1 to 31 and N = 2, 4, or 8.

For values commonly used in 1.0-Gbit systems, refer to Table D-1.

Table D-1. Switch Settings for 1.0-Gbit SerDes Prescalers

Input	Bank 1					Bank 2		Modulus
	SW5	SW4	SW3	SW2	SW1	SW2	SW1	
Clock In_alt	0	0	1	0	0	1	1	$5 \times 2 = 10$
Clock In	0	0	1	0	0	1	1	$2 \times 5 \times 2 = 20$
Clock In	0	0	1	0	0	0	1	$2 \times 5 \times 4 = 40$
Clock In	0	1	0	0	1	1	1	$2 \times 10 \times 2 = 40$

Schematics for this prescaler are available from local Freescale field applications engineers.

D.2 Prescaler Components

Table D-2 lists the major integrated circuit components needed for the prescaler.

Table D-2. Major Components for Divide-by-*xx* Prescaler

Part No.	Manufacturer	Supplier	Comments
MC12093	Freescale	Newark	1.1-GHz prescaler (divide by 2, 4, or 8)
MC100ELT23	On Semiconductor	Newark	Dual differential PECL to TTL translator, with separate inputs
MC100ELT21	On Semiconductor	Newark	Single differential PECL to TTL translator. Alternative to above part.
MC100ELT26	On Semiconductor	Newark	Dual differential PECL to TTL translator, with common inputs. Alternative to above part.
HMMC-3122	Agilent	Arrow	12-GHz divide-by-2 prescaler, GaAs HBT MMIC
HMC364S8G	Hittite Microwave	Hittite	12-GHz divide-by-2 prescaler, GaAs HBT MMIC. Pin-for-pin alternative to above part.
HMC394LP4	Hittite Microwave	Hittite	2.2-GHz programmable 5-bit counter, GaAs HBT MMIC

Appendix E
Revision History

This appendix provides a list of the major differences between revisions of the *MC92610 Quad SerDes Design Verification Board User's Guide* (MC92610DVBUM).

Table E-1 provides a revision history for this document.

Table E-1. MC92610DVB Revision History

Rev. No.	Date	Substantial Change(s)
1	05/02/2002	Initial release.
2	03/30/2004	Reformatted for new release.
3	12/9/2004	Reformatted to Freescale with minor edits. Added note to Figure 2-1. Top Side Part Location Diagram.

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MC92610DVBUG
Rev. 3, 06/2005

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