MC92603 Quad GEt Design Verification Board User's Guide

MC92603DVBUG
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freescale™
semiconductor

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Chapter 1
General Information

1.1 Introduction

This user's guide describes the MC92603DVB design verification board for the MC92603 integrated circuit. It should be read in conjunction with the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*. The design verification board (DVB) facilitates the full evaluation of the MC92603 Quad Gigabit Ethernet transceiver (GEt). It is intended for evaluation and testing purposes only. Freescale does not guarantee its performance in a production environment.

This board was designed to be used with laboratory equipment (pattern generators, data analyzers, BERT, scopes, and so on) or connected to other evaluation boards. Access to the MC92603 device (verification chip) is through connectors to each pin, to allow complete in-depth 'design verification' testing of the chip design. This allows the user to check any or all features/functions of the MC92603 GEt device.

The two parallel data input ports, and all configuration/control signal pins, are accessed through common 2×10, 0.100" male connectors (headers). The parallel data output ports are accessed through 2×20, 0.100" connectors. Device JTAG and MDIO port signals are also accessed with separate connectors.

The MC92603 high-speed serial receivers and transmitters are accessed through SMA coaxial connectors for signal integrity measurements. Gigabit Ethernet fiber media evaluations can be made with the provided small form-factor plugable (SFP) socket on the DVB, and an MSA (multi-source agreement) compliant transceiver. To use this SFP socket, four short coax cables are required to connect the SFP socket to the device's transmitter and receiver SMA connectors.

A single 5.0-V power source is required for DVB operation. All necessary voltages are generated by regulators onboard. The reference clock for the MC92603 chip may be provided using either an external clock or the onboard crystal oscillator. Clock drivers on the DVB provide additional clock signals for triggering analyzer instrumentation and scopes.

1.2 Features

The functional, physical, and performance features of the MC92603DVB are as follows:

- A single external 5.0-V to onboard regulators supply power to all onboard circuitry.
- Reference clock source is a 250-MHz crystal oscillator or an external clock source
- IEEE Std 802.3-2002® compliant GMII or TBI interfaces accessible through standard 0.100", 2 row connectors for data generators and analyzers
- Full-duplex differential data links accessible through SMA connectors
- Two pairs of 50-Ω test traces with SMA connections facilitate TDR measurements of the characteristic impedance of representative board traces.
- Connectors provided for JTAG and MDIO ports
- Two SFP sockets provided for MSA-compliant fiber modules
- Two IEEE Std 1394b (bilingual) sockets provided for standard cable links

1.3 Specifications

The MC92603DVB design verification board specifications are provided in Table 1-1.

Table 1-1. MC92603DVB Design Verification Board Specifications

Characteristics		Specifications
Board revision		A
External power supply		+5 DC ± 0.5 V DC < 2 A typical
Support circuit regulator		3.3 ± 0.3 V DC
MC92603 core and link I/O regulator		1.8 ± 0.15 V DC
Interface I/O (V_{DDQ}) regulator		2.5 ± 0.2 V DC or 3.3 ± 0.3 V DC
MC92603 package		256 MAPBGA
Operating temperature		0°–30°C
Material		FR-4
Dimensions	Height	14.1", 358 mm
	Width	10.0", 254 mm
	Thickness	0.062", 1.6 mm
Conducting layers		Four ground planes, one split power plane, three signal routing layers, top and bottom component layers with some additional signal routing

1.4 Block Diagram

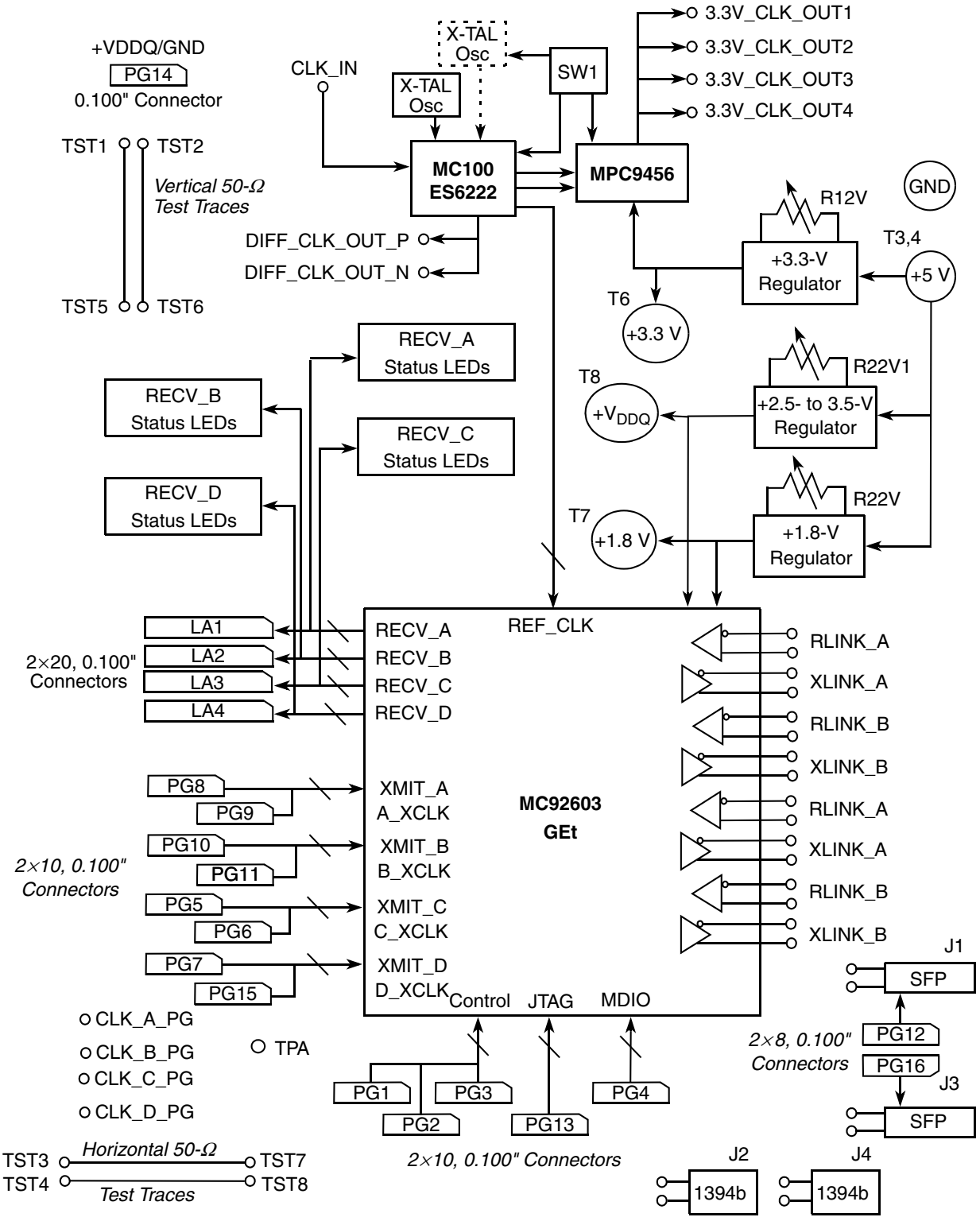


Figure 1-1. MC92603DVB Design Verification Board Block Diagram

1.5 Board Components

Table 1-2 is a list of major components of the MC92603DVB design verification board. A complete parts listing can be found in Appendix B, "Parts List."

Table 1-2. Major Board Components

Component	Description
MC92603VF	Freescale quad Gigabit Ethernet transceiver SerDes
2×10, 0.100" connectors	PG1–PG11, PG8–PG13, and PG15 provide access to the parallel inputs and control signals.
2×20, 0.100" connectors	LA1–LA4 provide access to the parallel outputs.
2×8, 0.100" connectors	PG12, PG16, and PG14 provide access to the SFP connector and $+V_{DD}$/ground planes, respectively.
SMA connectors	SMA1–SMA8: Serial transmit and receive connections TST1–TST8: Impedance test trace connections CLK_OUT1–CLK_OUT4, DIFF_CLK_OUT_P and _N: Reference clock outputs CLK_IN: External reference clock input CLK_A_PG, CLK_B_PG, CLK_C_PG, CLK_D_PG: Input clock connectors
SPF connector	J1, J3: Provide connections for SFP MSA optical modules
IEEE Std 1394b bilingual connector	J2, J4: Provide serial interface to 'Firewire' type a or b cable
LT1587 voltage regulators	VR33, VR18, and VR1: +3.3 V, +1.8 V, and $+V_{DD}$ voltage regulators
Potentiometers	R12V, R22V, R22V1: Potentiometers for setting +3.3 V, +1.8 V, and $+V_{DD}$ voltage levels
XTAL oscillator	Y1: Onboard 250-MHz crystal oscillator
MC100ES6222 clock buffer	U2: Divide-by-1 or divide-by-2 clock buffer
MPC9456 clock buffer	U3: +3.3-V LVCMOS clock buffer

1.6 Abbreviation List

Table 1-3 contains abbreviations used in this document.

Table 1-3. Acronyms and Abbreviated Terms

Term	Meaning
'1'	High logic level (nominally 2.5 or 3.3 V)
'0'	Low logic level (nominally 0.0 V)
BIST	Built-in self-test
DVB	Design verification board
I/F	Interface
MDIO	Management data input/output port
MSA	Multi-source agreement
N/C	No connection
PN	Pseudo-noise
PRBS	Pseudo random bit sequence
SFP	Small form-factor plugable (fiber optics module)
TAP	Test access port
TDR	Time delay reflectometry
UIp-p	Peak-to-peak unit interval

1.7 Related Documentation

Related documentation includes the following:

- *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide* (MC92603RM)
- MC92603DVB schematics
- MC100ES6222 data sheet
- MPC9456 data sheet
- IEEE Std 802.3-2002, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications

1.8 Contact Information

For questions concerning the MC92603 design verification kit or to place an order for a kit, contact a local Freescale field applications engineer.

Chapter 2
Hardware Preparation and Installation

This chapter provides instructions for unpacking, hardware preparation, configuration and installation, and a description of the interface components for the MC92603DVB.

2.1 Unpacking Instructions

Unpack the board from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of the equipment.

2.2 MC92603DVB Package Contents

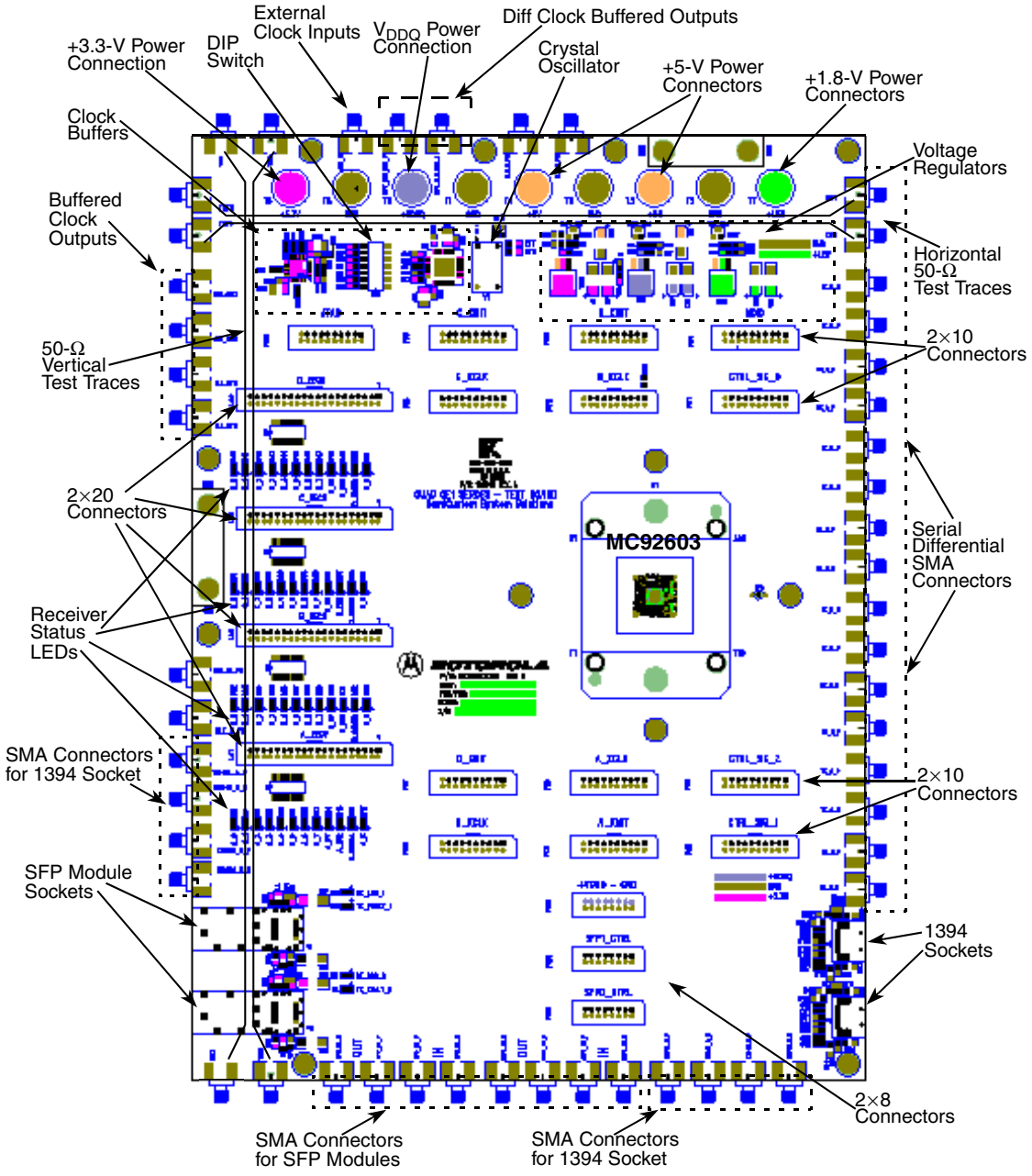
Table 2-1 describes the contents of the MC92603DVB kit.

Table 2-1. MC92603DVB Kit Contents

Qty.	Item
1	MC92603DVB design verification board
1	*MC92603DVBUM Quad GEt Design Verification Board User's Guide*
1	*MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*
1	Complete set of MC92603DVB design verification board schematics
85	0.100" shunts
6	Square pin receptacle patch cords

2.3 Hardware Preparation

Operation of the MC92603DVB requires proper setup of the power supply and voltage regulators as well as the reference clock. Figure 2-1 depicts the location of the major components on the board. The following sections describe the proper setup of the MC92603DVB.



NOTE:
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit, or function of the current product.

Figure 2-1. Top Side Part Location Diagram

2.3.1 Setting the Power Supply and Voltage Regulators

The MC92603DVB requires a single +5.0-V supply. Fully operational, the board will draw a maximum current less than 2.0 A from the +5.0-V supply. Actual current consumption depends on the user-set voltage levels, clock frequencies, use of an SFP module, and the MC92603 operating mode. The board contains two +5.0-V connection posts and two ground connection posts. These duplicate connections simplify using a four-wire supply: supply and ground, force and sense.

2.3.2 Setting the Voltage Regulators

The +5.0-V supply powers three onboard voltage regulators, VR33, VR18, and VR1. These regulators generate +3.3, +1.8, and +2.5/3.3 V (V_{DDQ}), respectively. The +3.3-V supply provides power to the oscillator, clock buffer chips, LED drivers, and power source for the SFP sockets. This supply can be varied over the range +3.3 V ± 0.3 V using the R12V potentiometer.

The +1.8-V supply powers the MC92603 core logic, transceivers, and on-chip phase-locked loop (PLL). This regulator can be adjusted over the range +1.8 V ± 0.15 V using R22V.

The V_{DDQ} supply powers the MC92603 control signal, parallel input, and output interface circuitry. This voltage level is determined by the desired logic interface. The supply can be adjusted using the R22V1 potentiometer from a nominal +2.5 to +3.3 V.

The +3.3-V, +1.8-V, and +V_{DDQ} supplies are accessible through connection posts. Note that these regulators should be set to voltage limits within the operating ranges described in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*. Failure to operate within these ranges could cause damage to the MC92603. Freescale does not guarantee MC92603 operation beyond the ranges specified. The R12V, R22V, and R22V1 potentiometers will be factory set for +3.3, +1.8, and +3.3 V, respectively.

2.4 Reference Clock Source

Through a combination of clock buffers, a reference clock is supplied to the MC92603 and several SMA output connectors. The input reference clock for the MC92603 can be supplied by either using an onboard crystal oscillator, or directly driving an external reference clock into the board's clock buffer circuit through the SMA connector, CLK_IN.

When selecting reference oscillators or external reference frequencies, only those frequencies listed in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide* are considered valid. Freescale does not guarantee operation of the MC92603 at frequencies other than those listed in the reference Guide. DIP switch settings select either the onboard oscillator or the external reference, as well as the enable for the clock buffer chips.

The clock circuitry for the MC92603DVB is shown in Figure 2-2.

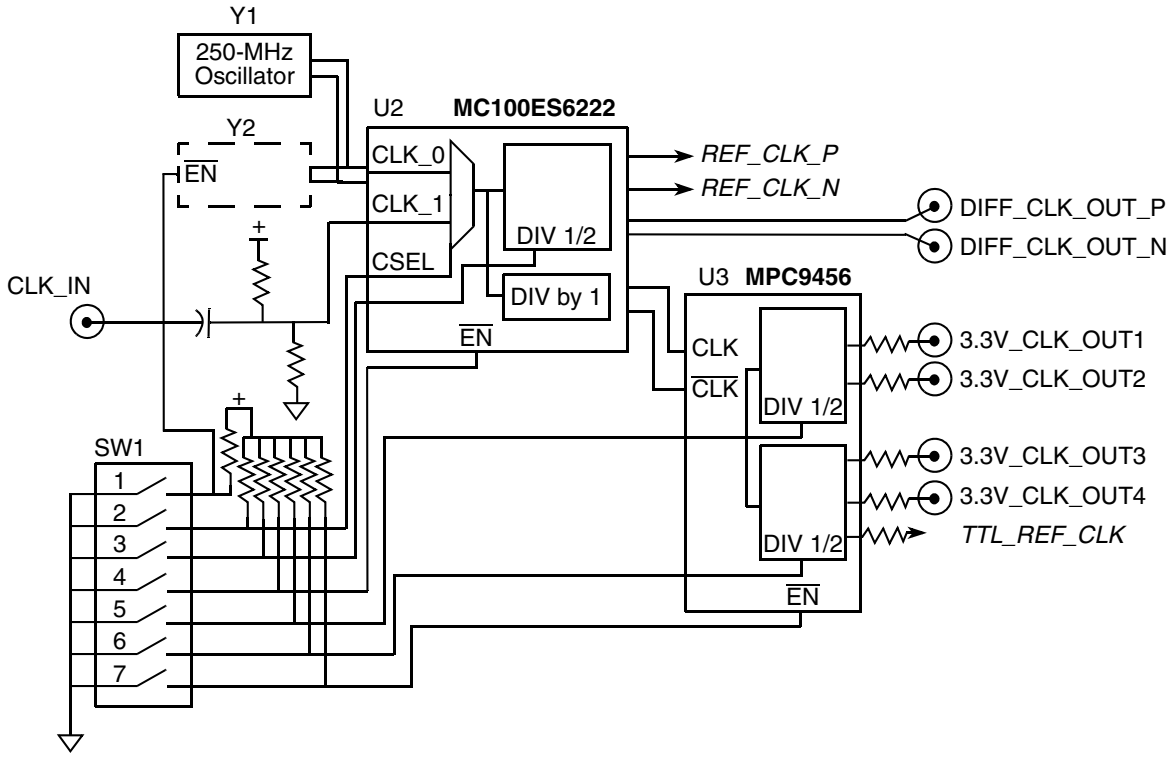


Figure 2-2. DVB Clock Circuitry

2.4.1 Using the Onboard Oscillators

There are two available positions for using onboard oscillators. A standard 14-pin DIP socket is available on the board to allow the user to easily change frequencies by swapping in crystal oscillators with other values. The onboard oscillators must be two times (2×) the desired MC92603 reference clock frequency. The default reference clock frequency oscillator supplied with the board is 250 MHz.

Crystal oscillators used with this board should have +3.3-V complementary PECL outputs capable of driving a line terminated with 50 Ω. Oscillators conforming to these specifications are available in surface mount packages and can be soldered onto the underside of the MC92603DVB at location Y2. This oscillator, Y2, can then be enabled by placing SW1 switch 1 in the ‘on’ position. Both types of crystal oscillators are available from external vendors in a variety of frequencies. The DVB may be shipped with either the Y1 or the Y2 oscillator installed. When using the Y2 oscillator, the Y1 oscillator must be removed from its socket. Once either type of oscillator is installed, SW1 switch 2 must be placed in the ‘on’ position to select the onboard oscillator.

2.4.2 External Reference Clock Source

The input reference clock can also be supplied by using an external reference clock into the clock buffer circuit on the board through the CLK_IN SMA connector. To supply an external reference clock, switch number 2 on SW1 must be set to the ‘off’ position. The user must then supply a 1.0-Vp-p input clock through the SMA connector. The CLK_IN input is AC coupled on the board and, therefore, does not require any DC biasing of the input signal. This external clock input is also terminated with a 50-Ω impedance.

2.4.3 Supplying a Clock to the MC92603

The input reference clock, from either the onboard oscillator or an external source, is applied to a MC100ES6222 clock buffer. This buffer has an input clock select multiplexer and a programmable divide-by-one/divide-by-two function. The buffer also contains a master reset ($\overline{\text{Enable}}$). It is recommended that this reset, found on SW1 switch 4, be activated, then deactivated after changing the divide-by-*xx* switch. This will ensure proper frequency generation.

The MC100ES6222 PECL outputs provide the differential reference clock to the MC92603 (REF_CLK_P and REF_CLK_N) and also to an MC9456 TTL fanout buffer. When using the default 250-MHz clock, Y1, switch position 3 must be ‘off’ to do a divide-by-2 to provide 125 MHz to the MC92603. A differential output pair, DIFF_CLK_OUT_P/ DIFF_CLK_OUT_N, is also provided for use with external equipment.

2.4.4 3.3V_CLK_OUT*n* SMA Connectors

Four single-ended, 3.3-V level clock signals are available on SMA connectors to drive other instruments. Between the MC100ES6222 output and the four SMAs is an MPC9456 that performs a differential PECL to a single-ended +3.3-V LVTTL/CMOS level shift. These CMOS outputs are series terminated on the board and connected to the SMA connectors labeled 3.3V_CLK_OUT1, 3.3V_CLK_OUT2, 3.3V_CLK_OUT3, and 3.3V_CLK_OUT4. All of the outputs of the MPC9456 can be disabled by setting the DIP switch SW1, switch 7 to the ‘off’ position.

2.4.5 Clock Frequency Selection

To accommodate the fact that the MC92603 can receive data on both edges of the reference clock (DDR) but many pieces of the test equipment are single-edge triggered (SDR), the MC92603DVB clock outputs can be programmed to be either the same as the supplied frequency or half the supplied frequency by setting SW1, switches 3, 5, and 6 to either ‘on’ (divide-by-1) or ‘off’ (divide-by-2). This allows the interface between the board and the bench to be either single data rate (SDR) with a double-speed clock, or double data rate (DDR) with a single-speed clock.

The SMA outputs 3.3V_CLK_OUT1 and 3.3V_CLK_OUT2 can be programmed by setting SW1, switch 5. The 3.3V_CLK_OUT3 and 3.3V_CLK_OUT4 outputs can be programmed by setting SW1, switch 6. Table 2-2 lists the switch positions and output frequencies. The input frequency, CLK_IN refers to either the onboard oscillator frequency or the externally applied clock source frequency.

NOTE

Only those frequencies listed in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide* are considered valid. Freescale does not guarantee operation of the MC92603 at frequencies other than those listed in the reference Guide.

Table 2-2. SW1 Settings and Output Frequencies

SW1 Switch	Switch Position	MC92603 REF_CLK_P, REF_CLK_N, and DIFF_CLK_OUT_P/N	3.3V_CLK_OUT1, 3.3V_CLK_OUT2	3.3V_CLK_OUT3, 3.3V_CLK_OUT4
3	on	CLK_IN	N/A	N/A
	Off	CLK_IN/2	N/A	N/A
5	On	N/A	CLK_IN	N/A
	Off	N/A	CLK_IN/2	N/A
6	On	N/A	N/A	CLK_IN
	Off	N/A	N/A	CLK_IN/2

Table 2-3 depicts SW1 settings for using an onboard oscillator with the divide-by-2 function set for the MC92603 and 3.3V_CLK_OUT*n* SMA outputs. The 3.3V_CLK_OUT1 and 3.3V_CLK_OUT2 SMA outputs are enabled and set to the divide-by-1 function. The 3.3V_CLK_OUT3 and 3.3V_CLK_OUT4 SMA outputs are also enabled and are set to the divide-by-2 function.

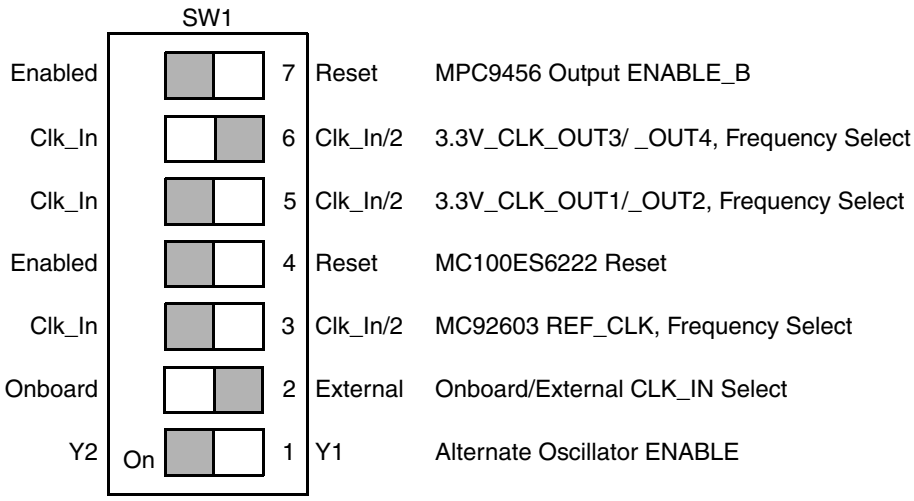


Figure 2-3. Reference Clock Selection Example Switch Settings

2.5 Interface Components

The following sections list the descriptions of the MC92603DVB interface connector components.

2.5.1 Parallel Inputs and Outputs

The MC92603 parallel I/O is supplied by the V_{DDQ} voltage regulator (set for 2.5 or 3.3 V) and has a rail-to-rail signal swing. The MC92603DVB is shipped with V_{DDQ} set at 3.3 V.

2.5.1.1 Parallel Inputs

The parallel inputs, both data and control, are accessible through 2×10, 0.100" connectors. Figure 2-4 depicts the 2×10, 0.100" connector numbering scheme, with pin 1 being labeled on the board. A complete mapping of the MC92603 inputs to the 2×10, 0.100" connectors is listed in Appendix A, "Connector Signals." Note that all even number pins are connected to ground.

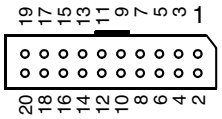


Figure 2-4. 2×10, 0.100" Input Connector Numbering Scheme (Top View)

For a description of the input functionality of the MC92603, refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*.

2.5.1.2 Parallel Outputs

All parallel outputs, both data and status bits, are present at four 2×20, 0.100" connectors. Figure 2-5 depicts the 2×20, 0.100" output connector numbering scheme, with pin 1 labeled on the board. The parallel output signals of the MC92603 are 2.5- or 3.3-V logic compatible depending on the setting of the V_{DDQ} regulator. A complete mapping of the MC92603 outputs to the 2×20, 0.100" connectors is listed in Appendix A, "Connector Signals." Note that all even number pins are connected to ground.

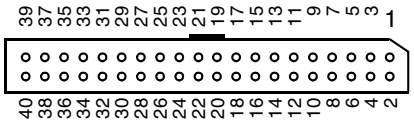


Figure 2-5. 2×20, 0.100" Output Connector Number Scheme (Top View)

For information regarding the MC92603 outputs, refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*.

2.5.2 +V_{DDQ} and Ground (GND) Access Connections

The MC92603DVB also has a 2×8, 0.100" connector, PG14, with dedicated connections to the +V_{DDQ} and ground planes. These are useful for biasing parallel input signals using jumper cables. All of the odd number pins (1, 3, 5, and 7) are connected to the V_{DDQ} plane. All of the even number pins (2, 4, 6, and 8) are connected to the ground (0.0 V) plane.

2.5.3 Serial Inputs and Outputs

All MC92603 high-speed serial differential inputs and outputs are connected to appropriately labeled pairs of SMA connectors through board traces with a characteristic impedance of 50 Ω (100-Ω differential). The output driver requires a 50-Ω parallel termination to mid-rail (+0.9 V nominal for +1.8-V supply). If the

termination voltage is not +0.9 V, the signal must be AC coupled. There is no AC coupling (DC blocking) of the serial outputs on the board. If needed, AC coupling must be done in-line before any termination.

During all testing, the serial transmitter outputs should be terminated with 50 Ω. This can be done by connecting the serial transmitter outputs to serial receiver inputs, to any laboratory equipment with 50-Ω input impedance through in-line AC coupling or by terminating the outputs with 50-Ω SMA terminations.

2.6 Special Application Connections

There are four sets of special connectors provided for application interface evaluation. A pair of Gigabit Ethernet SFP sockets are provided with SMA connections to connect to the MC92603DVB serial links and then perform evaluation testing with a fiber optic interface. The user must supply the SFP module. It is not provided with the MC92603DVB. Each SFP socket has it's own control interface connector, SFP0_CTRL and SFP1_CTRL. A mapping of these 2×8, 0.100" connectors is listed in Appendix A, "Connector Signals."

Likewise, a pair of IEEE Std. 1394B sockets (bilingual version) are provided with SMA connections to connect to the MC92603 serial links and perform testing with standard patch cords. (Note that there is a slight impedance mismatch, as the 1394 cables are 110-Ω differential.)

2.7 Special Test Connection

The MC92603DVB also contains an oscilloscope PCB test socket, labeled TPA. When the MC92603 is configured in a PLL factory test mode, this test socket enables special access to the PLL.

NOTE

This test mode is for factory testing purposes only. There are no system applications for this mode, and test socket TPA should remain unconnected at all times.

2.8 Test Traces

The MCS92610DVB design verification board has both vertical and horizontal 50-Ω test traces:

- Vertical: TST1–TST5 and TST2–TST6 are 14.59 inches long.
- Horizontal: TST3–TST7 and TST4–TST8 are 10.51 inches long.

These traces can be used to determine the impedance of the board using TDR measurement techniques.

NOTE

The vertical test traces should not be used as a differential pair. When doing TDR measurements, observe the difference in propagation delays. This is due to the TST1–TST5 trace being on the bottom surface layer (10) and TST2–TST6 being on an embedded signal layer (6). The horizontal test traces may be used a a differential pair and are located on the same embedded signal layer (8).

Chapter 3
Laboratory Equipment and Quick Setup Evaluation

This chapter begins with a listing of recommended test equipment needed to perform complete evaluations on the MC92603. Chapter 4, "Test Setups," covers specific setup configurations for this equipment depending on the desired feature under test. Appendix B, "Parts List," offers various suggested data test patterns that may be used with these test setups.

The quick setup evaluation procedures outlined below describe how the MC92603DVB can be used to evaluate the data 'eye diagram' and a simple error rate test using the internal test features of the MC92603 with a minimal amount of test equipment. Only a power supply and sampling oscilloscope are required.

Details of testing in specific systems is left to the user. For more information regarding the MC92603 feature set, refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*.

3.1 Recommended Laboratory Equipment

Evaluation of the MC92603 feature set is possible using the MC92603DVB evaluation kit in conjunction with several pieces of test equipment. The quick setup evaluations and other tests listed in this guide utilize the basic set of test equipment listed in Table 3-1. Equivalent instrumentation may be substituted. Not all pieces of test equipment are necessary for all tests.

Table 3-1. Recommended Test Equipment

Qty	Item
1	MC92603DVB evaluation kit
1	Tektronix TDS 8000 digital sampling oscilloscope
1	Tektronix 80E04 TDR/sampling head (20 GHz)
3	Tektronix 80E03 sampling heads (20 GHz)
1	Hewlett-Packard HP16700 logic analysis system
5	Hewlett-Packard HP16522A pattern generators
2	Hewlett-Packard HP16557D logic analyzers
1	Hewlett-Packard HP6624A system DC power supply

Table 3-2 lists the laboratory accessories.

Table 3-2. Lab Accessories

• SMA male each end coax patch cords, lengths: various
• SMA 3-dB attenuators
• SMA 6-db attenuators
• SMA DC blockers (AC couplers)
• 50-Ω SMA terminations (to ground)
• SMA 50-Ω feed through terminations
• 5/16" torque wrench (fits SMA, 2.9- and 3.5-mm connectors)
• Bias-T networks
• Power splitters
• BNC to SMA adapters
• SMA female to SMA female adapters
• SMA male to SMA male adapters
• SFP MSA optical modules (Agilent: HFBR5710L)

In-depth testing of the MC92603 can be performed using a bit error rate tester and a jitter analysis system. Table 3-3 provides a listing of test equipment that can be used for these types of tests.

Table 3-3. Jitter Analysis Test Equipment

Qty	Item
1	Agilent 71500C jitter analysis system
1	HP 70820A microwave transition analyzer
1	HP 70004A display
1	HP 3325B synthesizer/function generator
1	HP 83752A synthesized sweeper
1	HP 86130A BitAlyzer (serial bit error rate tester)
1	HP 70874C jitter personality card
2 each	Assorted bandpass filters
1	Rohde and Schwarz SMIQ-04B signal generator
1	Agilent HP 6624A system DC power supply
1	Agilent 11636B power splitter
1	Divide-by-*xx* prescalers

3.2 Quick Setup Data-Eye Diagram

The MC92603DVB design evaluation kit comes equipped to immediately demonstrate two of the MC92603 functions:

- Data-eye signal generation and observation
- Bit error rate checking using internal built-in self-test (BIST) features

3.2.1 Quick Setup Data-Eye Generation and Observation

A transmitted data-eye can be observed at either of the serial outputs of the MC92603 using its integrated, 23rd order, pseudo-noise (PN) pattern generator. The implementation of the 23-bit PN generator uses the following polynomial:

$$f = 1 + x^5 + x^{23}$$

Stimulus from this generator may also be used for further system testing. Refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, for more information.

3.2.1.1 Equipment Setup

Generation and observation of the data-eye produced by the on-chip PN generator requires only the MC92603DVB, a power supply, a high-speed digital sampling scope, and 0.100" shunts and single-pin receptacle patch cords.

The MC92603DVB and test equipment should be connected as shown in Figure 3-1. Configure clock circuits with SW1, as shown in Figure 2-3.

NOTE

All unconnected serial transmitter outputs should be terminated to 50 Ω. This can be done by connecting the serial transmitter outputs to the serial receiver inputs or to 50-Ω SMA terminations through in-line AC coupling (DC blocking).

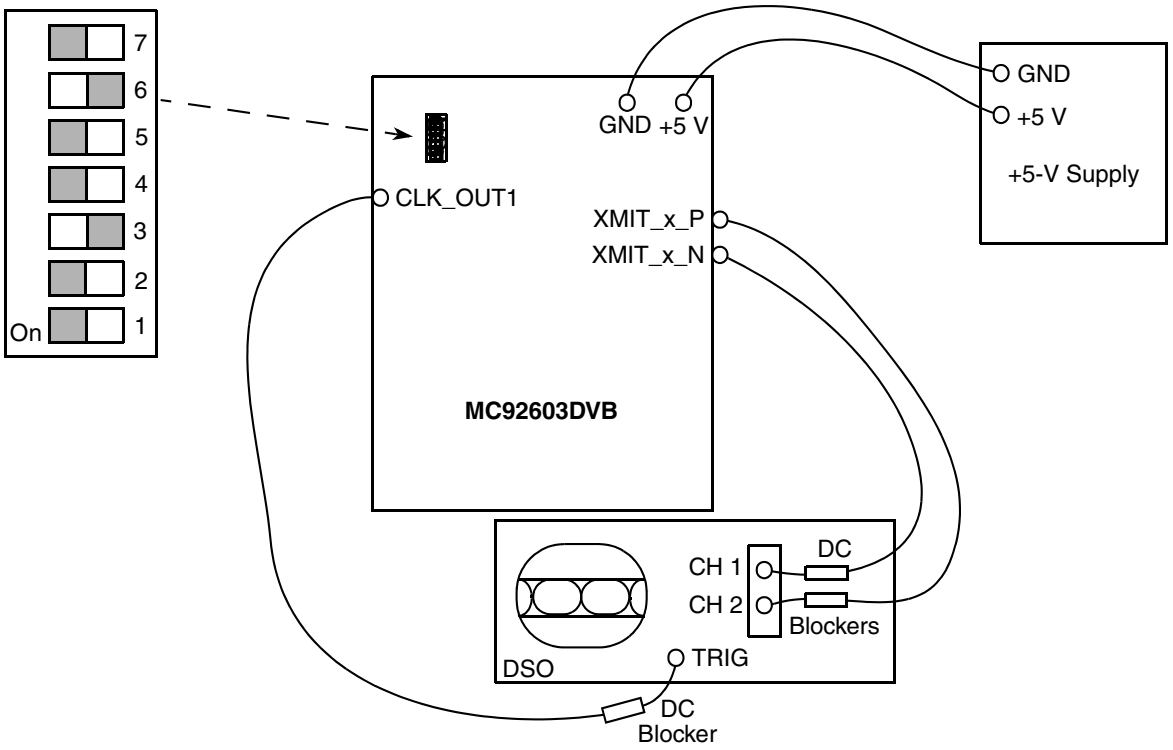


Figure 3-1. Data-Eye Observation Setup

3.2.1.2 Parallel Input Connections

The basic eye diagram will be generated by biasing the parallel inputs according to Table 3-4. Ground connections can be made using the 0.100" shunts. Connections to V_{DDQ} can be made using the square pin receptacle patch cords and jumpering to the odd number pins of header PG14. The shunts and patch cords are provided with the MC92603DVB kit. All even number pins on the connector headers are connected to the board's ground plane. All unlisted pins are not connected.

All the signal pins on the five connectors: CNTRL_SIG_0, CNTRL_SIG_1, CNTRL_SIG_2, JTAG, and MDIO have 10K pullup resistors to V_{DDQ}. By making no connection (N/C) to any of these pins, they are effectively biased high, or a logic '1.' Using a shorting shunt will bias them low, or logic '0.'

The signal pins on the channels *x*_XMIT and *x*_XCLK connectors do not have pullup resistors and, therefore, need to be biased high with jumper connections to V_{DDQ} or biased low with the shorting shunts.

Using a jumper wire on $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) and connecting to an access pin on connector PG14 will allow the MC92603 to be held in reset mode (connected to ground) or released (connected to V_{DDQ}).

Table 3-4 shows the initial configuration input biasing for the MC92603DVB as it is shipped from the factory. Test configurations in this document will necessitate the insertion or removal of the shorting shunts shown. If tests are performed with pattern generators and data analyzers, all shunts will need to be removed.

Table 3-4. Parallel Input Biasing as Shipped

Pin	Signal	Bias Level	Pin	Signal	Bias Level	Pin	Signal	Bias Level
	CTRL_SIG_0			A_XMIT			A_XCLK	
1	REPE	GND	1	XMIT_A_0	GND	1	GTX_CLK_0	N/C
3	RCCE	N/C	3	XMIT_A_1	GND	3	—	N/C
5	RECV_CLK_CENT	N/C	5	XMIT_A_2	GND	5	XCVR_A_DISABLE	GND
7	HSE	GND	7	XMIT_A_3	GND	7	XMIT_A_CLK	N/C
9	ADIE	GND	9	XMIT_A_4	GND	9	XMIT_A_K	GND
11	$\overline{\text{RESET}}$	Jumper to GND	11	XMIT_A_5	GND	11	XCVR_A_LBE	GND
13	DDR	GND	13	XMIT_A_6	GND	13	XMIT_A_ENABLE (bit 8)	GND
15	STNDBY	GND	15	XMIT_A_7	GND	15	XMIT_A_ERR (bit 9)	GND
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C
	CTRL_SIG_1			B_XMIT			B_XCLK	
1	LBOE	GND	1	XMIT_B_0	GND	1	GTX_CLK_1	N/C
3	USE_DIFF_CLK	N/C	3	XMIT_B_1	GND	3	—	N/C
5	MEDIA	GND	5	XMIT_B_2	GND	5	XCVR_B_DISABLE	GND
7	TBIE	GND	7	XMIT_B_3	GND	7	XMIT_B_CLK	N/C
9	COMPAT	GND	9	XMIT_B_4	GND	9	XMIT_AB	GND
11	JPAK	GND	11	XMIT_B_5	GND	11	XCVR_B_LBE	GND
13	RECV_REF_A	GND	13	XMIT_B_6	GND	13	XMIT_B_ENABLE (bit 8)	GND
15	XMIT_REF_A	GND	15	XMIT_B_7	GND	15	XMIT_B_ERR (bit 9)	GND
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C
	CTRL_SIG_2			C_XMIT			C_XCLK	
1	BSYNC	N/C	1	XMIT_C_0	GND	1	GTX_CLK_0	N/C
3	DROP_SYNC	GND	3	XMIT_C_1	GND	3	—	N/C
5	TST_1	GND	5	XMIT_C_2	GND	5	XCVR_C_DISABLE	GND
7	TST_0	N/C	7	XMIT_C_3	GND	7	XMIT_C_CLK	N/C
9	WSYNC1	GND	9	XMIT_C_4	GND	9	XMIT_C_K	GND
11	WSYNC0	GND	11	XMIT_C_5	GND	11	XCVR_C_LBE	GND
13	ENABLE_AN	GND	13	XMIT_C_6	GND	13	XMIT_C_ENABLE (bit 8)	GND
15	—	N/C	15	XMIT_C_7	GND	15	XMIT_C_ERR (bit 9)	GND
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C

Table 3-4. Parallel Input Biasing as Shipped (continued)

Pin	Signal	Bias Level	Pin	Signal	Bias Level	Pin	Signal	Bias Level
	JTAG			D_XMIT			D_XCLK	
1	XCVR_A_RSEL	GND	1	XMIT_D_0	GND	1	GTX_CLK_1	N/C
3	XCVR_B_RSEL	GND	3	XMIT_D_1	GND	3	—	N/C
5	BROADCAST	GND	5	XMIT_D_2	GND	5	XCVR_D_DISABLE	GND
7	ENAB_RED	GND	7	XMIT_D_3	GND	7	XMIT_D_CLK	N/C
9	TDI	N/C	9	XMIT_D_4	GND	9	XMIT_D_K	GND
11	TCK	N/C	11	XMIT_D_5	GND	11	XCVR_D_LBE	GND
13	TMS	N/C	13	XMIT_D_6	GND	13	XMIT_D_ENABLE (bit 8)	GND
15	$\overline{\text{TRST}}$	GND	15	XMIT_D_7	GND	15	XMIT_D_ERR (bit 9)	GND
17	—	N/C	17	—	N/C	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C
	MDIO			SFP0_CTRL			SFP1_CTRL	
1	MD_CLK	GND	1	—	N/C	1	—	N/C
3	MD_ENABLE	GND	3	—	N/C	3	—	N/C
5	MD_DATA	N/C	5	—	N/C	5	—	N/C
7	—	N/C	7	MOD_DEF_0	N/C	7	MOD_DEF_0	N/C
9	—	N/C	9	MOD_DEF_1	GND	9	MOD_DEF_1	GND
11	MD_ADR_2	GND	11	MOD_DEF_2	GND	11	MOD_DEF_2	GND
13	MD_ADR_3	GND	13	RATE_SELECT	N/C	13	RATE_SELECT	N/C
15	MD_ADR_4	GND	15	TX_DISABLE	GND	15	TX_DISABLE	GND
17	—	N/C						
19	GND	N/C						

3.2.1.3 Basic Eye Observation—Test Procedure

1. Connect the MC92603DVB and test equipment as described in Figure 3-1 and Table 3-4. This will place the MC92603 in PN generation mode with the MC92603 in reset.

   Steps 2 and 3 may be skipped if they were previously performed when setting up the DVB.
2. Apply +5.0 V to the evaluation board. Verify voltage levels of +3.3 V, +1.8 V, and +V_{DDQ} (3.3 V) regulators at connectors T6, T7, and T8, respectively. If necessary, adjust R12V, R22V, and R22V1 to obtain the desired voltage levels.
3. Verify that the reference clock frequency at CLK_OUT1 is 125 MHz (period = 8.0 ns).
4. Observe XMIT_*x*_P or XMIT_*x*_N output. Since the chip is in reset, the transmitter should show a constant output level at ground.

5. Connect $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a V_{DDQ} access connection on connector PG14. This releases the $\overline{\text{RESET}}$ signal.
6. Observe XMIT_*x*_P or XMIT_*x*_N. The transmitter should now be outputting random data. Setting the digital sampling oscilloscope to infinite persistence mode will display a data-eye. An example of a data-eye is shown in Figure 3-2.

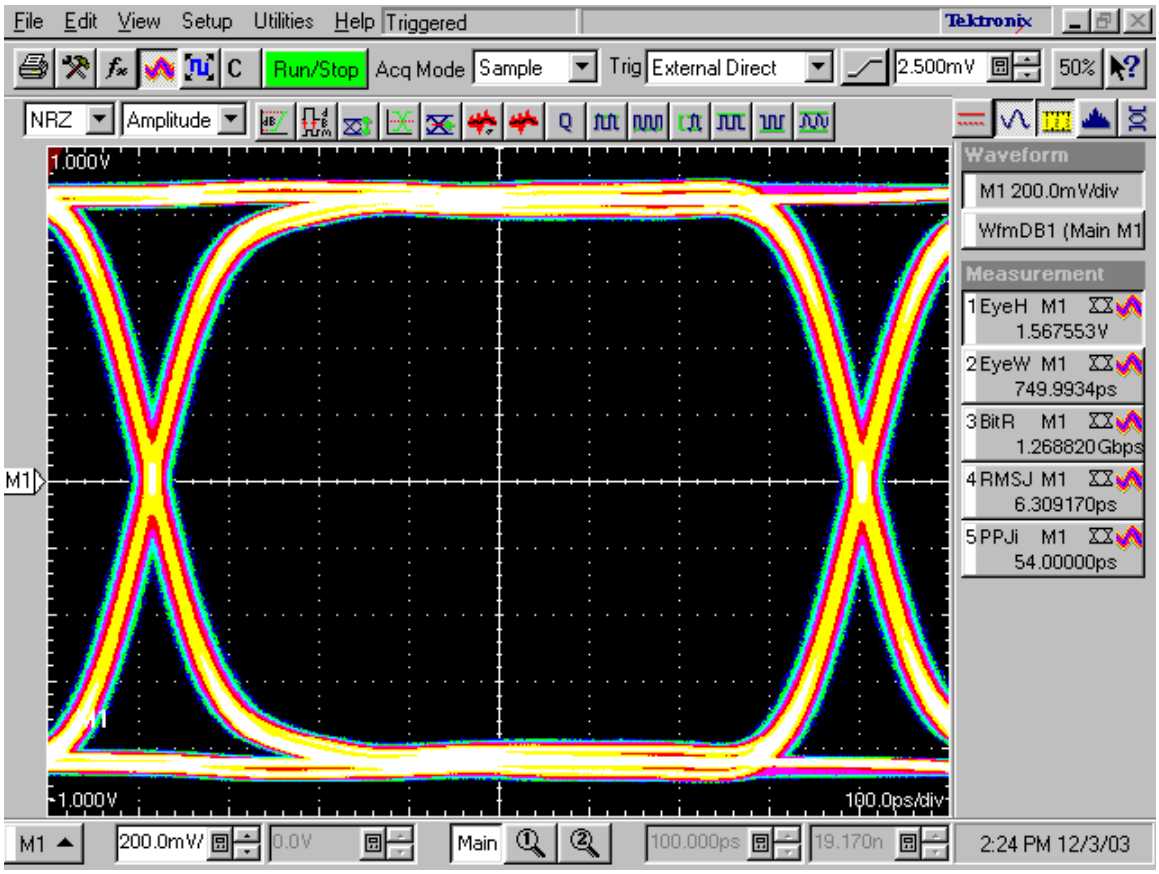


Figure 3-2. MC92603 Data-Eye Using Recommended Test Setup

3.2.2 Quick Setup Bit Error Rate Checking

In addition to having an integrated PN generator, the MC92603 also has a bit error rate checker (BERC). An integrated 23rd order signature analyzer that is synchronized to the incoming PN stream is used to count code group mismatch errors relative to the internal PN reference pattern. The following test procedure will describe how to use this BIST feature. For more information concerning the MC92603 BIST, refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*.

3.2.2.1 Equipment Setup

Connect the MC92603DVB as shown in Figure 3-3 connecting the transmitter outputs of the link under test (XLINK_*x*_P/N) to the receiver under test (RLINK_*x*_P/N).

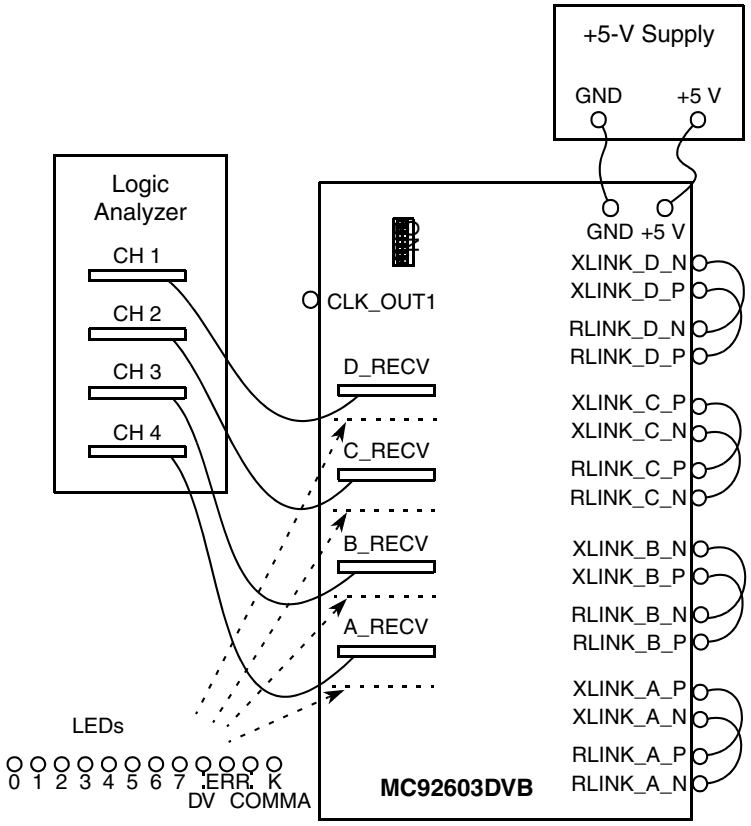


Figure 3-3. Bit Error Rate Check Test Setup

3.2.2.2 Parallel I/O Connections

The bias connections for the parallel inputs to perform the quick setup BERC test are the same as those for the quick setup eye-diagram and shown in Table 3-4.

The parallel outputs are connected to a data analysis system. For a simple quick test, the logic analyzer is not required since the errors are reported and may be observed on the channel status LEDs.

3.2.2.3 Quick Setup BERC Test Procedure

1. Connect the MC92603DVB and the test equipment as described in Section 3.2.2.1, "Equipment Setup." This will place the MC92603 in PN generation mode with the MC92603 held in reset and set the receivers to BERC mode using the recovered clock.

   Step 2 and 3 may be skipped if previously performed when setting up the DVB.
2. Apply +5.0 V to the evaluation board. Verify voltage levels of +3.3 V, +1.8 V, and +V_{DDQ} (3.3 V) regulators at connectors T6, T7, and T8, respectively. If necessary, adjust R12V, R22V, and R22V1 to obtain the desired voltage levels.
3. Verify that the reference clock frequency at CLK_OUT1 is 125 MHz (period = 8.0 ns).
4. Connect the $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a V_{DDQ} access connection on connector PG14. This releases the $\overline{\text{RESET}}$ signal.
5. Observe the parallel outputs on the data analyzer and the status LEDs. As described in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, the MC92603 will start and lock its PLL, initialize the receivers, perform byte alignment, and reset its bit error counter.
6. When the receivers are locked and BIST is running, the recovered clock is observable on RECV_*x*_RCLK. See Table 3-5 for the errors codes and Figure 3-4 for an example of a receiver startup and error detection sequence.
7. Once the receiver has initially locked all receiver data bits, RECV_*x*_[7:0], are set to zero (logic low). Should an error occur, RECV_*x*_[7:0] will increment by one and RECV_*x*_ERR will flag the error during that byte time. The value of RECV_*x*_[7:0] remains constant until another error is detected or the system is reset. If the receiver counter fills with errors, all bits of RECV_*x*_[7:0] stay a logic high (11111111) until the receiver is reset. Refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, for more detail.

Table 3-5. BIST Error Codes

RECV_*x*_DV	RECV_*x*_ERR	RECV_*x*_COMMA	Status Description
Low	Low	Do not care	Not byte/word sync: The receiver is in startup or has lost byte alignment and is searching for alignment.
High	Low	Low	BIST running, no PN mismatch this code group
High	Low	High	BIST running, this code group is a COMMA code group
Low	High	Do not care	Receiver byte/word synchronized, PN analyzer is not locked
High	High	Do not care	BIST running, PN mismatch error this code group

The error count and status may be observed on the channel receiver status LEDs. Simple bit error rate may be calculated. For example, if the error count on the LEDs is 3 and the test has been running for 53 minutes, the BER would be: 3 errors divided by (53 minutes × 60 seconds per minute × 1.25 × 10^9 bits per second), or 2.515^{-13}.

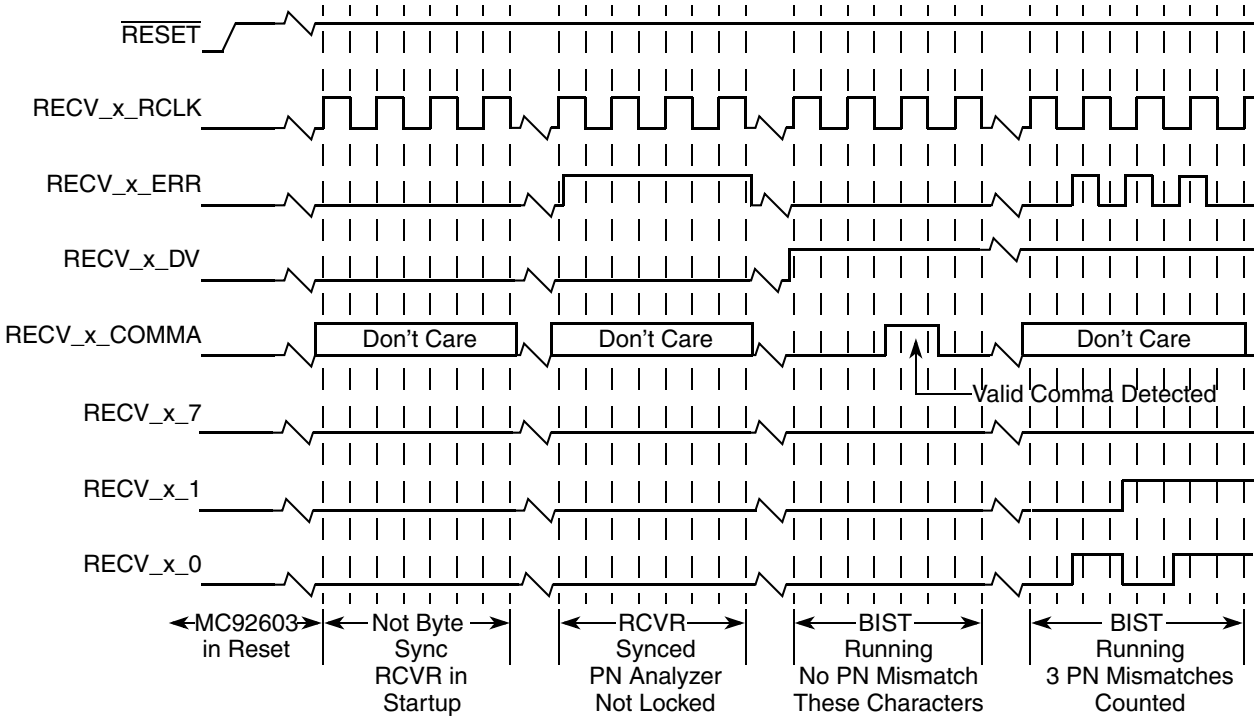


Figure 3-4. Receiver Startup and Error Detection Sequence

Chapter 4
Test Setups

This chapter outlines the laboratory test equipment setup and procedure to evaluate the features of the MC92603 in more depth than those outlined in the previous chapter. These setups are meant to be guidelines only and are not implied to be complete. Details of testing in specific system applications are left to the user.

4.1 Serial Link Verification Using a Serial Bit Error Rate Tester (BERT)

This test setup is used to observe the rate at which the MC92603 produces errors given either pseudo-random (PRBS) patterns or user-defined pattern sets generated by the serial bit error rate tester (BERT). The MC92603 is placed in repeater mode, REPE = high, thereby disabling the parallel receiver and transmitter buses. Testing performed using the ten-bit interface mode does not require the insertion of idle characters for word recognition or byte alignment. If verification using the 8B/10B encoder or other MC92603 features is required, then appropriate idle insertion and timing requirements as outlined in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, must be followed.

4.1.1 Test Setup for Full-Speed Mode

Figure 4-1 depicts the test setup for MC92603 in full-speed mode (HSE = 0). The control bits are set as follows:

- REPE = 1
- TBIE = 1

All other control bits are set to 0, except $\overline{\text{RESET}}$, which is initially set to 0 and then transitioned to 1 to start the MC92603.

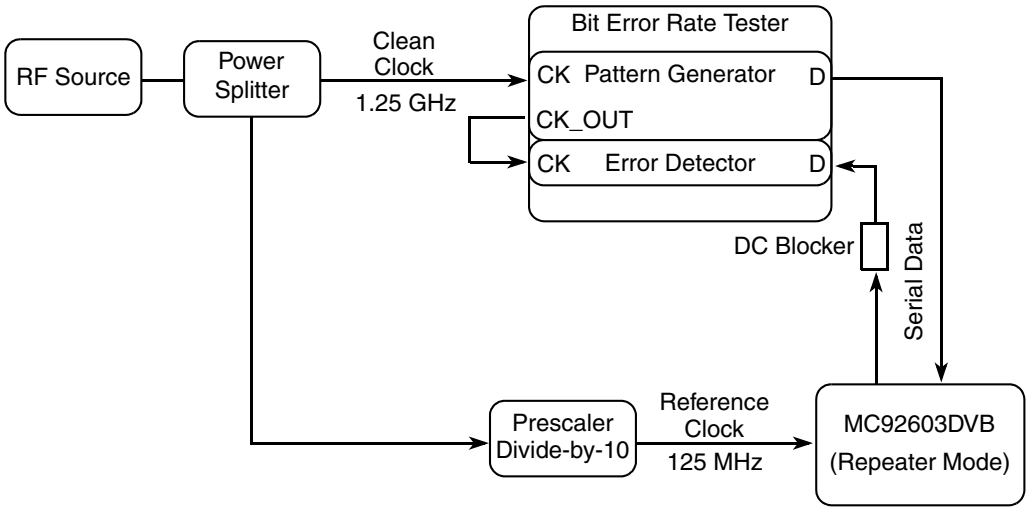


Figure 4-1. Full-Speed Serial Link Test Setup

4.1.2 Test Setup for Half-Speed Modes

Serial link testing may also be performed using half-speed mode (HSE = 1). This reduces all frequencies in the setup by a factor of two. Figure 4-2 depicts the serial link test setup using HSE and a divide-by-10 prescaler. The control bits are set as follows:

- HSE = 1
- REPE= 1
- TBIE = 1

All other control bits are set to 0, except $\overline{\text{RESET}}$, which is initially set to 0 and then transitioned to 1 to start the MC92603.

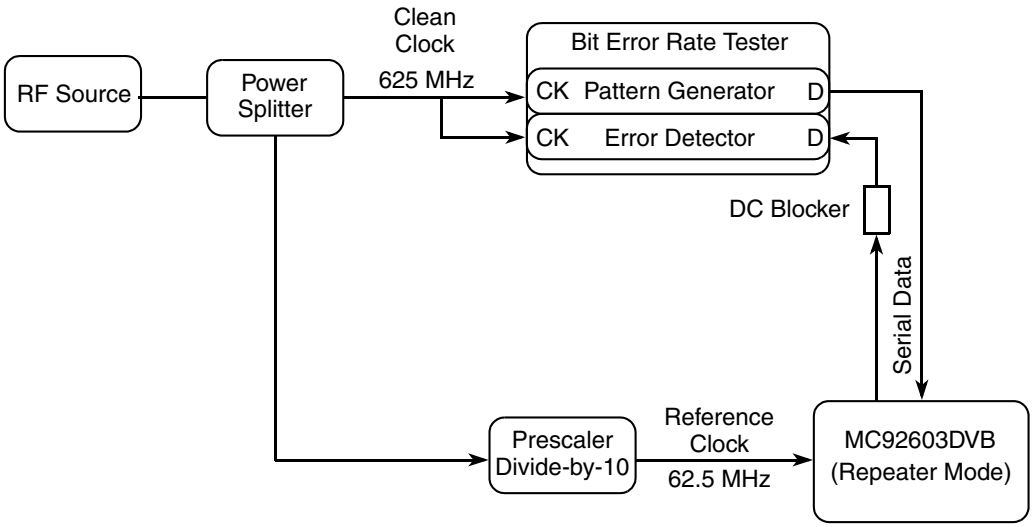


Figure 4-2. Half-Speed Serial Link Test Setup

4.2 Jitter Testing

The following tests are guidelines for verifying the performance of the MC92603 in ‘noisy’ conditions. Results will vary depending on input reference frequencies, MC92603 mode of operation, test setup and equipment, and test environment.

4.2.1 Jitter Test System Calibration

Before beginning any type of jitter measurement, the system must first be calibrated, as shown in Figure 4-3, to produce the desired frequency and amplitude modulation of the jittered source. The amplitude of modulation is then translated into jitter in units of peak-to-peak unit intervals (UIp-p). Different synthesized sweepers have different characteristics at different frequencies. It is possible for certain frequencies to produce spurious side lobes that will affect jitter characterization. It is strongly advised that a bandpass filter centered on the carrier frequency be used at the input to the microwave transition analyzer. Refer to the synthesized sweeper reference Guide for more details.

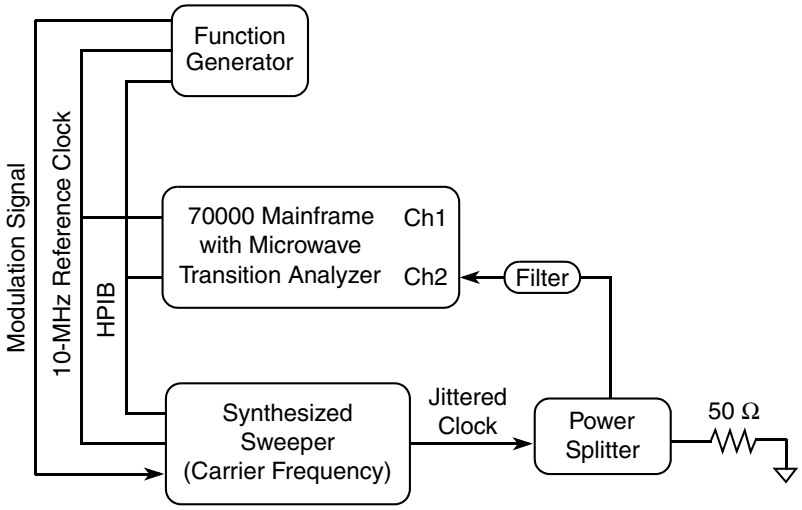


Figure 4-3. Jitter Measurement System Calibration

4.2.2 Reference Clock Jitter Transfer Test

This test setup, shown in Figure 4-4, is used to observe the amount of jitter placed on the reference clock that is transferred to the data outputs. Example frequencies were chosen to match narrow bandpass filters available with the Agilent 71500C jitter analysis system.

All control bits are set to 0, except $\overline{\text{RESET}}$, which is initially set to 0 and then transitioned to 1 to start the MC92603. The XMIT data bits are set as follows:

- XMIT_*x*_ENABLE = 1
- XMIT_*x*_[7:0] = 0xB5
- XMIT_*x*_CLK jumpered to GTX_CLK

This data pattern appears as a 625-MHz clock signal at the serial outputs.

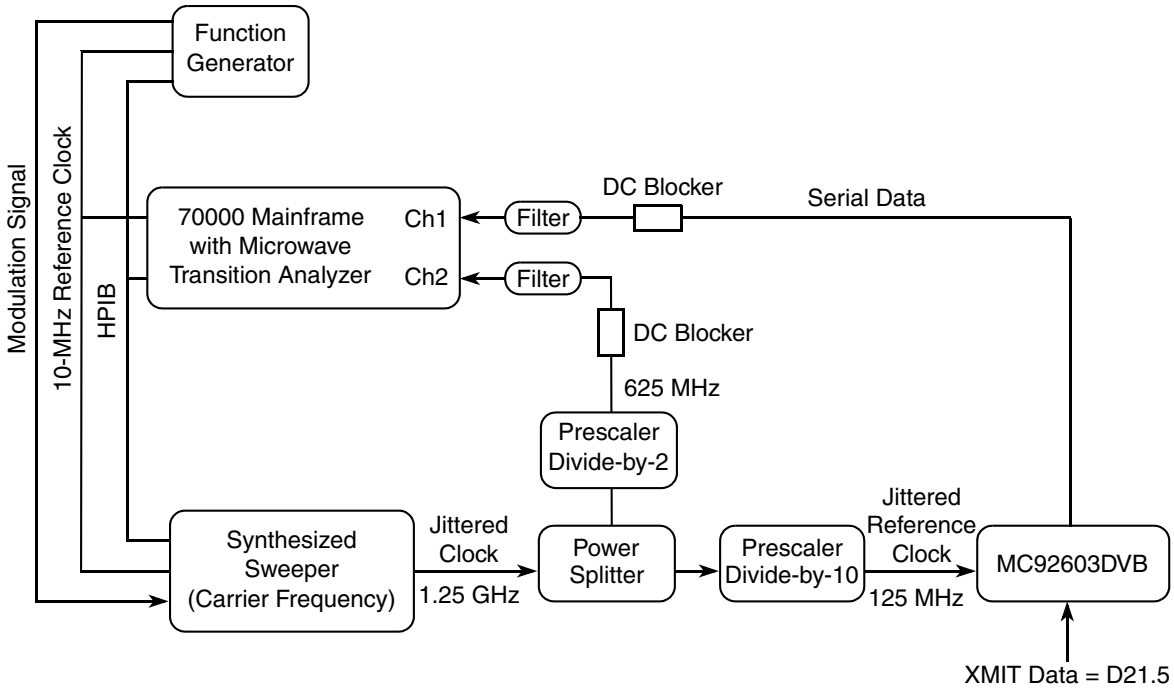


Figure 4-4. Reference Clock Jitter Transfer Test Setup

4.2.3 Reference Clock Jitter Tolerance Test

The test setup in Figure 4-5 is used to observe the amount of jitter placed on the reference clock that does not produce errors on the serial data outputs as compared to the input serial data stream. The MC92603 is placed in ten-bit interface mode (TBIE) and repeater mode (REPE). The serial data stream can be set to either PRBS or user-defined data. The control bits are set as follows:

- REPE = 1
- TBIE = 1

All other control inputs are set to 0.

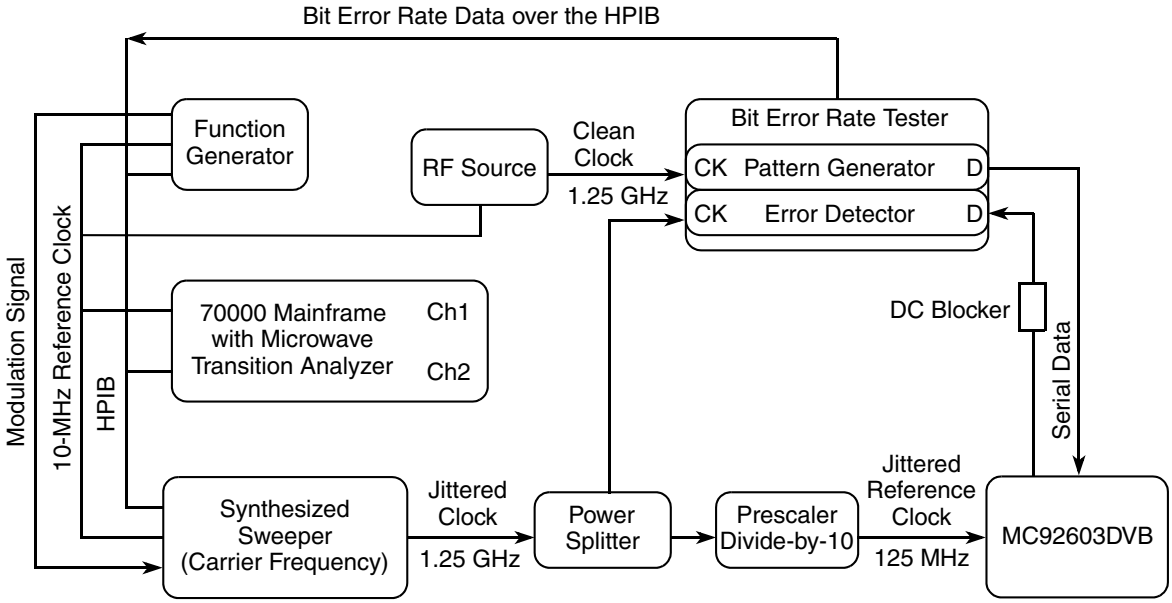


Figure 4-5. Reference Clock Jitter Tolerance Test Setup

4.2.4 Data Jitter Tolerance Test

The test setup shown in Figure 4-6 is used to observe the amount of jitter placed on the serial data inputs that does not produce errors on the serial data outputs. The MC92603 is placed in ten-bit interface mode (TBIE) and repeater mode (REPE). The serial data stream can be set to either PRBS or user-defined data. The control bits are set as follows:

- REPE = 1
- TBIE = 1

All other control inputs are set to 0.

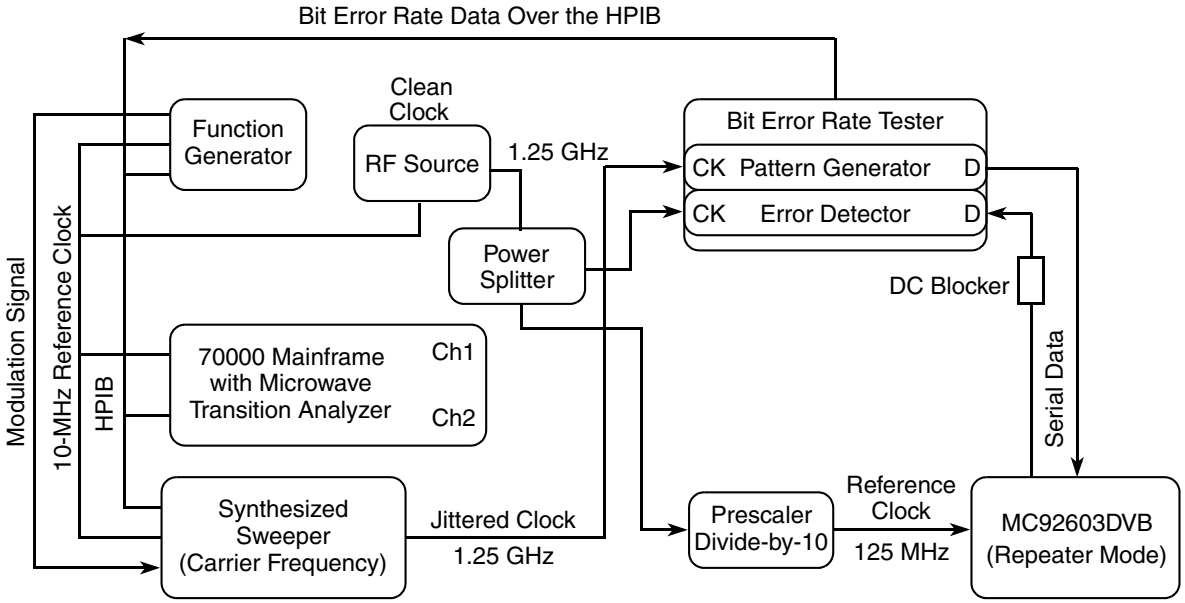


Figure 4-6. Data Jitter Tolerance Test Setup

Appendix A
Connector Signals

The parallel data input and output signals of the MC92603DVB design verification board are listed in the following tables. All the connection test points use the common 2 row 0.100" spaced 3-M type connectors.

A.1 Input: 2×10 (0.100") Connectors

The configuration/control, data and test inputs to the MC92603 are via 2 row by 10 connectors. There are a total of thirteen input connectors on the DVB.

On each connector, the even pin numbers (2, 4, ..., to 20) are connected to the ground plane. The config/control signal inputs (on the odd pin numbers) have 10K pullup resistors on the DVB board. Therefore, if the configuration requires a ‘high’ or logic 1, the pin may be left open. The data inputs, however do not have pullups and will need to be jumpered to V_{DDQ} for a logic 1. If the signal input is required to be ‘low,’ a shorting jumper may be installed.

The signal name, description, and the MC92603 device ‘ball’ (pin) number are listed in the following tables for each of the input connectors.

A.1.1 Control Signal Input Connectors

The signals on connectors CTRL_SIG_0, CTRL_SIG_1, and CTRL-SIG_2 (PG1–PG3 respectively) are control input signals that set the basic configuration to the MC92603. These signals and corresponding connector pins are listed in Table A-1, Table A-2, and Table A-3, respectively.

Table A-1. CTRL_SIG_0 Connector

Connector Pin	MC92603 Pin	Input Signal Name	Description
1	E14	REPE	Repeater mode enable
3	M10	RCCE	Recovered clock enable
5	A12	RECV_CLK_CENT	Center recovered clock relative to data
7	E13	HSE	Half-speed mode enable
9	N12	ADIE	Add/drop idle enable
11	D13	RESET	System reset bar
13	P9	DDR	Enable double data rate
15	P14	STNDBY	Standby mode enable
17	N/C	—	—
19	N/C	GND	Ground connection

Table A-2. CTRL_SIG_1 Connector

Connector Pin	MC92603 Pin	Input Signal Name	Description
1	R12	LBOE	Loopback output enable
3	A15	USE_DIF_CLK	Use differential reference clock inputs
5	N9	MEDIA	Media impedance select
7	P11	TBIE	Ten-bit interface enable
9	T13	COMPAT	IEEE Std. 802.3 compatibility mode enable
11	T10	JPACK	Enable FIFO for jumbo packets
13	N10	RECV_REF_A	Use receiver A as primary clock output
15	E12	XMIT_REF_A	Use transmit A as primary clock input
17	N/C	—	—
19	N/C	GND	Ground connection

Table A-3. CTRL_SIG_2 Connector

Connector Pin	MC92603 Pin	Input Signal Name	Description
1	M11	BSYNC	Byte synchronization mode
3	F12	DROP_SYNC	Drop synchronization
5	T14	TST_1	Test mode—select 1
7	N11	TST_0	Test mode—select 0
9	M12	WSYNC1	Word sync. mode definer
11	P13	WSYNC0	Word sync. mode definer
13	M9	ENAB_AN	Enable auto-negotiate
15	N/C	—	—
17	N/C	—	—
19	N/C	GND	Ground connection

A.1.2 Transmitter Parallel Data Input Connectors

The MC92603 transmitter parallel data input signals for channels A through D are mapped to the 2×10 connectors as listed in the tables below. Table A-4 shows the 8-bit data byte input for the transmitter channels A through D, respectively, on A_XMIT to D_XMIT (PG8, PG10, PG5, and PG7) connectors

Table A-4. A_XMIT, B_XMIT, C_XMIT, and D_XMIT Connectors

Connector Pin No.	MC92603 Ball No.				Input Signal Name	Description
	A_XMIT, (Channel A)	B_XMIT, (Channel B)	C_XMIT, (Channel C)	D_XMIT, (Channel D)		
1	T8	B8	C8	N5	XMIT_*x*_0	Transmitter *x*, data input bit 0
3	R8	A8	D8	P4	XMIT_*x*_1	Transmitter *x*, data input bit 1
5	P8	A9	A7	T3	XMIT_*x*_2	Transmitter *x*, data input bit 2
7	N8	B9	E8	R4	XMIT_*x*_3	Transmitter *x*, data input bit 3
9	M8	C9	B7	P5	XMIT_*x*_4	Transmitter *x*, data input bit 4
11	T7	D9	C7	N6	XMIT_*x*_5	Transmitter *x*, data input bit 5
13	R7	E9	A6	T4	XMIT_*x*_6	Transmitter *x*, data input bit 6
15	P7	A10	B6	R5	XMIT_*x*_7	Transmitter *x*, data input bit 7
17	N/C	N/C	N/C	N/C	—	—
19	N/C	N/C	N/C	N/C	GND	Ground Connection

Table A-5 lists the remaining transmitter input signals for the four channels on A_XCLK through D_XCLK (PG9, PG11, PG6, and PG15) connectors, respectively. Pin 1 of the *x*_XCLK connector is the buffered reference clock output from the MC92603 PLL that may be used as the input clock for the pattern generator. These signals supply the GTX_CLK reference when interfacing to Ethernet MACs.

Alternatively, an external pattern generator clock reference may be supplied to the CLK_*x*_PG, SMA connectors. If these external sources are used, resistors R37, R39, R149, and R151 must be installed and resistors R36, R38, R148, and R150 removed, respectively.

NOTE

If an external clock source is used it must be the same frequency as that of the REF_ CLK to the MC92603 chip. The user can use the 3.3_CLK_OUT*n* clocks provided on the DVB as a source clock to the pattern generator.

Table A-5. A_XCLK, B_XCLK, C_XCLK and D_XCLK Connectors

Connector Pin No.	MC92603 Ball No.				Input Signal Name	Description
	A_XCLK, (Channel A)	B_XCLK, (Channel B)	C_XCLK, (Channel C)	D_XCLK, (Channel D)		
1	T12	C11	T12	C11	Buffered reference clock GTX_CLK0 for channels A and C GTX_CLK1 for channels B and D	
3	N/C	N/C	N/C	N/C	—	—
5	R9	B11	E7	R3	XCVR_*x*_ DISABLE	Transceiver *x*, disable
7	T9	D10	B5	M6	XMIT_*x*_CLK	Transmitter *x*, interface clock
9	T6	A11	C6	M7	XMIT_*x*_K	Transmitter *x*, special character
11	R10	P10	T11	R11	XMIT_*x*_LBE	Transmitter *x*, loopback enable
13	N7	B10	D7	P6	XMIT_*x*_ ENABLE (XMIT_*x*_8)	Transmitter *x*, enable data in (data bit 8 for ten-bit mode)
15	R6	C10	A5	T5	XMIT_*x*_ERR (XMIT_*x*_9)	Transmitter *x*, force code error (data bit 9 for ten-bit mode)
17	N/C	N/C	N/C	N/C	—	—
19	N/C	N/C	N/C	N/C	GND	Ground connection

A.2 Output: 2×20 (0.100") Connectors

The MC92603 receiver parallel data outputs are connected to 2×20, 0.100" connectors. A mapping of these signals are contained in Table A-6.

Table A-6 lists the signals for the A_RECV, B_RECV, C_RECV, and D_RECV (LA1 to LA4) connectors. Note that the receive data clock, RECV_*x*_RCLK, is brought out to two connector pins. Care should be exercised when connecting to both these pins not to exceed the drive capacity of the chip output. Refer to the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, for more details.

Table A-6. A_RECV and B_RECV Connectors

Connector Pin No.	MC92610 Ball No.				Output Signal Name	Description
	A_RECV, (Channel A)	B_RECV, (Channel B)	C_RECV, (Channel C)	D_RECV, (Channel D)		
1	N/C	N/C	N/C	N/C	—	—
3	N3	J4	G3	C3	RECV_*x*_RCLK	XCVR_ *x*, receive data clock
5	N/C	N/C	N/C	N/C	—	—
7	N3	J4	G3	C3	RECV_*x*_RCLK	XCVR_ *x*, receive data clock
9	L5	J3	G2	E5	RECV_*x*_RCLK	XCVR_ *x*, receive data clock_complement
11	N/C	N/C	N/C	N/C	GND	Ground connection
13	N/C	C12	N/C	N/C	GND (on channels A, C, and D) For channel B this pin is TDO (JTAG, test data out)	
15	M5	H1	H4	D6	RECV_*x*_K	Receiver *x*, K detect status
17	N4	J1	H5	B4	RECV_*x*_ COMMA	Receiver x, COMMA detect status
19	P3	H2	H3	A4	RECV_*x*_ERR (bit 9)	Receiver x, error detect (bit 9 in 10-bit mode)
21	M4	J2	G1	C5	RECV_*x*_DV (bit 8)	Receiver *x*, data valid status (bit 8 in 10-bit mode)
23	P2	K1	F1	C2	RECV_*x*_7	Receiver *x*, data bit 7
25	N2	J5	G4	F5	RECV_*x*_6	Receiver *x*, data bit 6
27	M3	K2	F2	E4	RECV_*x*_5	Receiver *x*, data bit 5
29	L4	K3	E1	D3	RECV_*x*_4	Receiver *x*, data bit 4
31	N1	L1	F3	C1	RECV_*x*_3	Receiver *x*, data bit 3
33	K5	L2	G5	D2	RECV_*x*_2	Receiver *x*, data bit 2
35	M2	K4	E2	E3	RECV_*x*_1	Receiver *x*, data bit 1
37	L3	M1	D1	F4	RECV_*x*_0	Receiver *x*, data bit 0
39	N/C	N/C	N/C	N/C	—	—

A.3 JTAG_0 Connector

Table A-7 lists the signals for the JTAG (PG13) connector. This is the MC92603 test access port, TAP, interface for IEEE Std. 1149 JTAG testing.

NOTE

There are 100-KΩ internal pullups on TMS, TDI, and $\overline{\text{TRST}}$. If $\overline{\text{TRST}}$ is not held low during power up or does not receive an active low preset after power up, the test logic may assume an indeterminate state disabling some of the normal transceiver functions. It is recommended that $\overline{\text{TRST}}$ be terminated in one of the following ways:

- $\overline{\text{TRST}}$ be driven by a TAP controller that provides a reset after power up.
- Connect $\overline{\text{TRST}}$ to $\overline{\text{RESET}}$.
- Terminate $\overline{\text{TRST}}$ with a 1-KΩ resistor (or hardwire) to ground.

The DVB has a 10K-pullup on TCLK to provide an input termination to the clock input if the TAP is not used. It is important to use a shorting jumper on the $\overline{\text{TRST}}$ input to comply with the above note. For more information on the test access port, see Section 6.1 in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, for more details.

The JTAG connector also has four configuration pins associated with the redundant link operation. There are 10K-pullups on these configuration pins.

Table A-7. JTAG Connector

Connector Pin	MC92603 Pin	Input Signal Name	Description
1	C4	XCVR_A_RSEL	Use redundant XLINK_C and RLINK_C
3	E6	XCVR_B_RSEL	Use redundant XLINK_D and RLINK_D
5	B3	BROADCAST	Transmit over all links
7	A3	ENAB_RED	Enable redundant links
9	A13	TDI	JTAG test data in
11	D11	TCK	JTAG test clock
13	B12	TMS	JTAG test mode select
15	E10	TRST	JTAG test reset bar
17	N/C	—	—
19	N/C	GND	Ground connection

A.4 MDIO Connector

Table A-8 lists the signals for the MDIO (PG4) connector. These connections are for the MDIO device address configuration and interface for the MC92603. If MDIO is not being used, the MD_ENABLE pin must be terminated low. See Chapter 4 in the *MC92603 Quad Gigabit Ethernet Transceiver Reference Guide*, for details. There are no other connection requirements to the MDIO connector.

Table A-8. MDIO Connector

Connector Pin	MC92603 Pin	Input Signal Name	Description
1	E11	MD_CLK	MDIO clock
3	B14	MD_ENABLE	MDIO enable
5	B13	MD_DATA	MDIO data (bidirectional data)
7	N/C	—	—
9	N/C	—	—
11	A14	MD_ADR_2	MDIO PHY address bit 2
13	C13	MD_ADR_3	MDIO PHY address bit 3
15	D12	MD_ADR_4	MDIO PHY address bit 4
17	N/C	—	—
19	N/C	GND	Ground connection

A.5 SFP_CTRL Connectors

The control signals for the small form-factor pluggable (SFP) sockets are available on the 2 row by 8, SFP_CTRL0 (PG12) and SFP_CTRL1 (PG14) connectors as listed in Table A-9. These are standard signals for the multiple source agreement (MSA) fiber optic modules. The TX_DISABLE pin must be low for the module to operate.

Table A-9. SFP_CTRL0 and SFP_CNTRL1 Connectors

Connector Pin	SFP0 Module Pin	SFP1 Module Pin	Input Signal Name	Description
1	N/C	N/C	—	—
3	N/C	N/C	—	—
5	N/C	N/C	—	—
7	6	6	MOD_DEF_0	Module definition 0
9	5	5	MOD_DEF_1	Module definition 1
11	4	4	MOD_DEF_2	Module definition 2
13	7	7	RATE_SELECT	Rate select. Not connected in most SFPs.
15	3	3	TX_DISABLE	SFP Transmitter disable

Appendix B
Parts List

B.1 Design Verification Board Parts List

Table B-1 shows the parts used in constructing the MC92603DVB design verification board.

Table B-1. MC92603DVB Design Verification Board Parts List (Sheet 1 of 3)

Item	Qty.	Reference	Value	Manufacturer	Part No.	Description
1	2	J2 J4	N/A	Molex Inc.	45241-0001	IEEE Std 1394B bilingual socket
2	4	U4–7	N/A	Fairchild	74VCX16244	Buffer 1.2–3.6 V
3	8	C11–12 C16 C35 C41 C44 C48 C64	0.1 µF		CAP0603, 0.1 µF	0603 ceramic chip capacitor
4	7	C2–6 C15 C17 C25–26 C28–29 C34 C36–40 C42–43 C45–47 C49–53 C58–63 C94 C96 C301-302	0.01 µF		CAP0805, 0.01 µF	0805 chip capacitor
5	14	C73–79 C85–91	0.05 µF		CAP0805, 0.05 µF	0805 chip capacitor
6	14	C9–10 C14 C20 C65 C69 C71–72 C81 C83–84 C92-93 C95	0.1 µF		CAP0805, 0.1 µF	0805 chip capacitor
7	15	C1 C18–19 C24 C27 C30–33 C54–57 C303–304	1 µF		CAP1812, 1 µF	1812 chip capacitor
8	3	C7 C21 C66	100 µF		CAP7343, 100 µF	7343 solid tantalum chip capacitor, low ESR, 10 V
9	9	C8 C13 C22–23 C67–68 C70 C80 C82	10 µF		CAP7343, 10 µF	7343H solid tantalum chip capacitor, low ESR, 35 V
10a	1	Y1	250 MHz	MF Electronics	M2988-250M	250-MHz PECL oscillator
10b	1	Y2	250 MHz	Raltron	CE8950A-LZ-250.000	250-MHz surface mount PECL oscillator
11	1	Y1socket	N/A	TTI	504-AG11D	Socket for oscillators; DIP4(14)
12	1	SW1	N/A	Omron	A6S-7104	SM 7-pole DIP slide switches, 2 positions (open/closed)
13	3	PG12 PG14 PG16	N/A	3M	2516-6002UB	2×8 keyed header with shroud, 0.1" pin spacing
14	13	PG1–11 PG13 PG15	N/A	3M	3428-6002UB	2×10 keyed header with shroud, 0.1" pin spacing
15	4	LA1–4	N/A	3M	2540-6002UB	2×20 keyed header with shroud, 0.1" pin spacing

Table B-1. MC92603DVB Design Verification Board Parts List (Sheet 2 of 3)

Item	Qty.	Reference	Value	Manufacturer	Part No.	Description
16	4	L1–4	1 μH		IND-MOLDED, 1 μH	Inductor-molded, 1 μH
17	3	VR1 VR18 VR33	N/A	Linear Technology	LT1587	Linear voltage regulator, 3 amps, 3-lead DD pak
18	1	U1	N/A	Freescale	MC92603VF	Quad SerDes Gigabit Ethernet transceiver
19	1	U2	N/A	Freescale	MC100ES6222	LV 1:15 differential ECL/PECL clock divider and fanout buffer
20	2	J1 J3	N/A	Molex Inc.	74441-0010	20-pin SFP connector
21	1	U3	N/A	Freescale	MPC9456	2.5–3.3 V LVCMOS clock fanout buffer
22	1	Y1	N/A			Socket for oscillators; DIP4(14)
23	9	T1–9	N/A	SPC Technology	2303/2304/9648/ 9649/9650	4-mm screw terminal binding post, 2-red, 4-black, 1-yellow, 1-blue, 1-green
24	8	R5–6 R62–63 R70–71 R74–75	82 Ω		RES0603, 82 Ω	0603 chip resistor
25	15	R25–26 R36–39 R42 R148–151 R176–179	0 Ω		RES0805, 0 Ω	0805 chip resistor
26	1	R24	100 Ω		RES0805, 100 Ω	0805 chip resistor
27	86	R1 R7–9 R14–18 R28–32 R34–35 R48–49 R52–59 R64–67 R78–84 R88–91 R96–104 R117–129 R142–147 R180–181 R190–195 R200–201 R203–204 R209–210	10 KΩ		RES0805, 10 KΩ	0805 chip resistor
28	64	R3–4 R10 R12 R20 R22 R50–51 R60–61 R68–69 R72–73 R92–95 R105–112 R130–141 R152–175 R196–197	124 Ω		RES0805, 124 Ω	0805 chip resistor
29	1	R27	1650 Ω		RES0805, 1650 Ω	0805 chip resistor
30	2	R11 R13	330 Ω		RES0805, 330 Ω	0805 chip resistor
31	11	R2 R19 R45–47 R85–87 R186–188	36 Ω		RES0805, 36 Ω	0805 chip resistor
32	7	R202 R205–207 R211–213	50 Ω		RES0805, 50 Ω	0805 chip resistor
33	2	R21 R23	68 Ω		RES0805, 68 Ω	0805 chip resistor
34	10	R33 R43–44 R76–77 R184–185 R198–199 R208	1 Ω		RES1206, 1 Ω	1206 chip resistor
35	6	RR40–41 R113 R182–183 R189	1 MΩ		RES1206, 1 MΩ	1206 chip resistor

Table B-1. MC92603DVB Design Verification Board Parts List (Sheet 3 of 3)

Item	Qty.	Reference	Value	Manufacturer	Part No.	Description
36	1	TPA	N/A	Johnson	129-0701-202	Scope PCB test socket
37	60	1394B1_A_N 1394B1_A_P 1394B1_B_N 1394B1_B_P 1394B_A_N 1394B_A_P 1394B_B_N 1394B_B_P CLK_A_PG CLK_B_PG CLK_C_PG CLK_D_PG CLK_IN CLK_OUT1–4 DIFF_CLK_OUT_N DIFF_CLK_OUT_P RX_A_N RX_A_P RX_B_N RX_B_P RX_C_N RX_C_P RX_D_N RX_D_P SFP1_RX_N SFP1_RX_P SFP1_TD_N SFP1_TD_P SFP_RX_N SFP_RX_P SFP_TD_N SFP_TD_P SMA1–9 TST1–8 TX_A_N TX_A_P TX_B_N TX_B_P TX_C_N TX_C_P TX_D_N TX_D_P	N/A	Johnson	SMA	SMA 50-Ω RF PCB jack socket
38	45	D1–14 D16 D18–30 D32 D34–36 D38 D40–48 D50 D52–53	N/A	Dialight	597-5311-402	Green SM LED
39	4	D15 D31 D37 D49	N/A	Dialight	597-5111-402	Red SM LED
40	4	D17 D33 D39 D51	N/A	Dialight	597-5411-402	Yellow SM LED
41	1	R12V	1 KΩ	Bourns	3214W-1-502E	Surface mount trim resistor
42	2	R22V R22V1	500 Ω	Bourns	3214W-1-502E	Surface mount trim resistor
43	2	JC1 JC3	N/A	Molex Inc.	73927-0009	SFP cage assembly 15 press-fit legs and 3 EMI clips
44	85	N/A	N/A	3M	929950-00	0.100" shunts
45	6	N/A	N/A	Pomona	4741-12-0/ 4741-12-2	Square pin receptacle patch cord

Appendix C
Prescaler for Jitter Measurement

C.1 Divide-by-*xx* Prescaler Description

Evaluating jitter in a system requires that all clocks within the system be based on one common source. For this reason, it is often necessary to use prescalers to derive the needed reference clock. Freescale has developed a small programmable prescaler with a maximum input frequency of 4.4 GHz which can be assembled using commercially available parts. Figure C-1 depicts the block diagram of this prescaler.

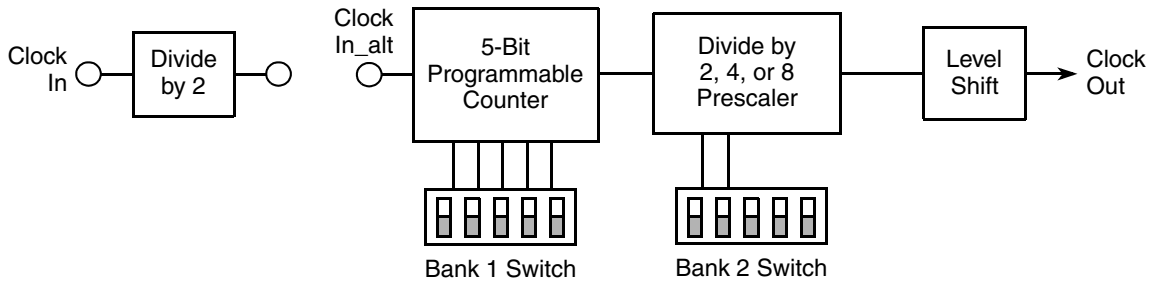


Figure C-1. Divide-by-*xx* Prescaler Block Diagram

The input to the prescaler can be either through a divide-by-2 or directly into the 5-bit programmable counter. The bank 1 and bank 2 DIP switches can be used to select a variety of prescaler values based on the following formula:

$$\text{Modulus} = 2 \cdot (A + 1) \cdot N$$

where A = 1 to 31 and N = 2, 4, or 8.

For values commonly used in 1.0-Gbit systems refer to Table C-1.

Table C-1. Switch Settings for 1.0-Gbit SerDes Prescalers

Input	Bank 1					Bank 2		Modulus
	SW5	SW4	SW3	SW2	SW1	SW2	SW1	
Clock In_alt	0	0	1	0	0	1	1	$5 \times 2 = 10$
Clock In	0	0	1	0	0	1	1	$2 \times 5 \times 2 = 20$
Clock In	0	0	1	0	0	0	1	$2 \times 5 \times 4 = 40$
Clock In	0	1	0	0	1	1	1	$2 \times 10 \times 2 = 40$

Schematics for this prescaler are available from your Freescale field applications engineer.

C.2 Prescaler Components

Table C-2 lists the major integrated circuit components needed for the prescaler.

Table C-2. Major Components for Divide-by-*xx* Prescaler

Part No.	Manufacturer	Supplier	Comments
MC12093	Freescale	Newark	1.1-GHz prescaler (divide by 2, 4, or 8)
MC100ELT23	On Semiconductor	Newark	Dual differential PECL to TTL translator, with separate inputs.
MC100ELT21	On Semiconductor	Newark	Single differential PECL to TTL translator. Alternative to above part.
MC100ELT26	On Semiconductor	Newark	Dual differential PECL to TTL translator, with common inputs. Alternative to above part.
HMMC-3122	Agilent	Arrow	12-GHz divide-by-2 prescaler, GaAs HBT MMIC.
HMC364S8G	Hittite Microwave	Hittite	12-GHz divide-by-2 prescaler, GaAs HBT MMIC. Pin-for-pin alternative to above part.
HMC394LP4	Hittite Microwave	Hittite	2.2-GHz programmable 5-bit counter, GaAs HBT MMIC.

Appendix D
Revision History

This appendix provides a list of the major differences between revisions of the *MC92603 Quad GEt Design Verification Board User's Guide* (MC92603DVBUM).

Table D-1 provides a revision history for this document.

Table D-1. MC92603DVB Revision History

Rev. No.	Date	Substantive Change(s)
0	3/2004	Initial release
1	12/2004	Reformatted to Freescale with minor edits. Added note to Figure 2-1. Top Side Part Location Diagram.

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