


**Table
Number**
LIST OF TABLES
**Page
Number**

3-1 MC68336/376 Pin Characteristics	3-7
3-2 MC68336/376 Output Driver Types.....	3-8
3-3 MC68336/376 Power Connections	3-8
3-4 MC68336/376 Signal Characteristics	3-9
3-5 MC68336/376 Signal Functions.....	3-11
4-1 Unimplemented MC68020 Instructions.....	4-10
4-2 Instruction Set Summary	4-11
4-3 Exception Vector Assignments	4-17
4-4 BDM Source Summary	4-21
4-5 Polling the BDM Entry Source	4-22
4-6 Background Mode Command Summary.....	4-23
4-7 CPU Generated Message Encoding.....	4-26
5-1 Show Cycle Enable Bits.....	5-3
5-2 Clock Control Multipliers	5-7
5-3 System Frequencies from 4.194 MHz Reference.....	5-9
5-4 Bus Monitor Period	5-13
5-5 MODCLK Pin and SWP Bit During Reset.....	5-15
5-6 Software Watchdog Ratio	5-15
5-7 MODCLK Pin and PTP Bit at Reset.....	5-16
5-8 Periodic Interrupt Priority	5-17
5-9 Size Signal Encoding.....	5-21
5-10 Address Space Encoding	5-21
5-11 Effect of DSACK Signals	5-23
5-12 Operand Alignment.....	5-25
5-13 DSACK, BERR, and HALT Assertion Results	5-34
5-14 Reset Source Summary.....	5-40
5-15 Reset Mode Selection.....	5-41
5-16 Module Pin Functions During Reset	5-45
5-17 SIM Pin Reset States.....	5-46
5-18 Chip-Select Pin Functions	5-56
5-19 Pin Assignment Field Encoding	5-57
5-20 Block Size Encoding	5-58
5-21 Chip-Select Base and Option Register Reset Values.....	5-62
5-22 CSBOOT Base and Option Register Reset Values.....	5-63
6-1 SRAM Array Address Space Type	6-2
7-1 ROM Array Space Type.....	7-2
7-2 Wait States Field.....	7-2
8-1 Multiplexed Analog Input Channels	8-5



Table Number	Page Number
8-2 Analog Input Channels	8-12
8-3 Queue 1 Priority Assertion.....	8-17
8-4 QADC Clock Programmability	8-26
8-5 QADC Status Flags and Interrupt Sources.....	8-32
9-1 Effect of DDRQS on QSM Pin Function	9-5
9-2 QSPI Pins	9-9
9-3 Bits Per Transfer.....	9-19
9-4 SCI Pins.....	9-26
9-5 Serial Frame Formats.....	9-27
10-1 CTM4 Time Base Bus Allocation	10-3
10-2 DASM Modes of Operation.....	10-11
10-3 Channel B Data Register Access	10-11
10-4 PWMSM Divide By Options.....	10-15
10-5 PWM Pulse and Frequency Ranges (in Hz) Using $\div 2$ Option (20.97 MHz) ...	10-17
10-6 PWM Pulse and Frequency Ranges (in Hz) Using $\div 3$ Option (20.97 MHz) ...	10-18
10-7 CTM4 Interrupt Priority and Vector/Pin Allocation	10-20
11-1 TCR1 Prescaler Control.....	11-14
11-2 TCR2 Prescaler Control.....	11-15
11-3 TPU Function Encodings	11-16
11-4 Channel Priority Encodings	11-17
13-1 Common Extended/Standard Format Frames.....	13-4
13-2 Message Buffer Codes for Receive Buffers.....	13-5
13-3 Message Buffer Codes for Transmit Buffers.....	13-5
13-4 Extended Format Frames	13-6
13-5 Standard Format Frames.....	13-6
13-6 Receive Mask Register Bit Values.....	13-8
13-7 Mask Examples for Normal/Extended Messages	13-8
13-8 Example System Clock, CAN Bit Rate and S-Clock Frequencies	13-9
13-9 Interrupt Sources and Vector Addresses	13-20
A-1 Maximum Ratings.....	A-1
A-2 Typical Ratings.....	A-2
A-3 Thermal Characteristics	A-2
A-4 Clock Control Timing.....	A-3
A-5 DC Characteristics	A-4
A-6 AC Timing	A-6
A-7 Background Debug Mode Timing.....	A-18
A-8 ECLK Bus Timing	A-19
A-9 QSPI Timing	A-21
A-10 Time Processor Unit Timing	A-24
A-11 QADC Maximum Ratings	A-25
A-12 QADC DC Electrical Characteristics (Operating)	A-26

Table Number	Page Number
A-13 QADC AC Electrical Characteristics (Operating)	A-27
A-14 QADC Conversion Characteristics (Operating).....	A-28
A-15 FCSM Timing Characteristics.....	A-29
A-16 MCSM Timing Characteristics.....	A-29
A-17 SASM Timing Characteristics.....	A-30
A-18 DASM Timing Characteristics	A-30
A-19 PWMSM Timing Characteristics.....	A-31
B-1 MC68336 Ordering Information.....	B-4
B-2 MC68376 Ordering Information.....	B-5
D-1 Module Address Map	D-1
D-2 T[1:0] Encoding	D-3
D-3 SIM Address Map.....	D-4
D-4 Show Cycle Enable Bits	D-7
D-5 Port E Pin Assignments	D-10
D-6 Port F Pin Assignments.....	D-11
D-7 Software Watchdog Timing Field	D-12
D-8 Bus Monitor Time-Out Period.....	D-13
D-9 Pin Assignment Field Encoding	D-15
D-10 CSPAR0 Pin Assignments.....	D-15
D-11 CSPAR1 Pin Assignments	D-16
D-12 Reset Pin Function of CS[10:6].....	D-16
D-13 Block Size Field Bit Encoding	D-17
D-14 BYTE Field Bit Encoding.....	D-18
D-15 Read/Write Field Bit Encoding	D-19
D-16 DSACK Field Encoding	D-19
D-17 Address Space Bit Encodings.....	D-20
D-18 Interrupt Priority Level Field Encoding	D-20
D-19 SRAM Address Map.....	D-21
D-20 RASP Encoding	D-22
D-21 MRM Address Map	D-23
D-22 ROM Array Space Field	D-24
D-23 Wait States Field.....	D-25
D-24 QADC Address Map.....	D-27
D-25 Queue 1 Operating Modes.....	D-31
D-26 Queue 2 Operating Modes.....	D-33
D-27 Queue Status	D-35
D-28 Input Sample Times	D-36
D-29 Non-multiplexed Channel Assignments and Pin Designations	D-37
D-30 Multiplexed Channel Assignments and Pin Designations.....	D-38
D-31 QSM Address Map.....	D-39
D-32 PQSPAR Pin Assignments	D-46
D-33 Effect of DDRQS on QSM Pin Function.....	D-47
D-34 Bits Per Transfer	D-48
D-35 CTM4 Address Map	D-54



Table Number	Page Number
D-36 Interrupt Vector Base Number Bit Field	D-56
D-37 Time Base Register Bus Select Bits	D-56
D-38 Prescaler Division Ratio Select Field	D-57
D-39 Drive Time Base Bus Field.....	D-58
D-40 Counter Clock Select Field.....	D-59
D-41 Drive Time Base Bus Field.....	D-60
D-42 Modulus Load Edge Sensitivity Bits	D-60
D-43 Counter Clock Select Field.....	D-61
D-44 DASM Mode Flag Status Bit States	D-62
D-45 Edge Polarity.....	D-64
D-46 DASM Mode Select Field	D-64
D-47 DASMA Operations.....	D-65
D-48 DASMB Operations.....	D-66
D-49 PWMSM Output Pin Polarity Selection	D-68
D-50 PWMSM Divide By Options	D-69
D-51 TPU Register Map.....	D-71
D-52 TCR1 Prescaler Control Bits	D-72
D-53 TCR2 Prescaler Control Bits	D-72
D-54 FRZ[1:0] Encoding	D-73
D-55 Breakpoint Enable Bits.....	D-74
D-56 Channel Priorities.....	D-78
D-57 Parameter RAM Address Map	D-79
D-58 TPURAM Address Map.....	D-79
D-59 TouCAN Address Map	D-81
D-60 RX MODE[1:0] Configuration	D-86
D-61 Transmit Pin Configuration.....	D-86
D-62 Transmit Bit Error Status	D-91
D-63 Fault Confinement State Encoding	D-92

