



Figure Number	LIST OF FIGURES	Page Number
3-1	MC68336/376 Block Diagram	3-4
3-2	MC68336 Pin Assignments for 160-Pin Package	3-5
3-3	MC68376 Pin Assignments for 160-Pin Package	3-6
3-4	MC68336/376 Address Map	3-13
3-5	Overall Memory Map	3-14
3-6	Separate Supervisor and User Space Map	3-15
3-7	Supervisor Space (Separate Program/Data Space) Map	3-16
3-8	User Space (Separate Program/Data Space) Map	3-17
4-1	CPU32 Block Diagram	4-2
4-2	User Programming Model	4-3
4-3	Supervisor Programming Model Supplement	4-4
4-4	Data Organization in Data Registers	4-5
4-5	Address Organization in Address Registers	4-6
4-6	Memory Operand Addressing	4-8
4-7	Loop Mode Instruction Sequence	4-15
4-8	Common In-Circuit Emulator Diagram	4-20
4-9	Bus State Analyzer Configuration	4-20
4-10	Debug Serial I/O Block Diagram	4-25
4-11	BDM Serial Data Word	4-26
4-12	BDM Connector Pinout	4-26
5-1	System Integration Module Block Diagram	5-2
5-2	System Clock Block Diagram	5-4
5-3	System Clock Oscillator Circuit	5-5
5-4	System Clock Filter Networks	5-6
5-5	LPSTOP Flowchart	5-12
5-6	System Protection Block	5-12
5-7	Periodic Interrupt Timer and Software Watchdog Timer	5-16
5-8	MCU Basic System	5-19
5-9	Operand Byte Order	5-24
5-10	Word Read Cycle Flowchart	5-27
5-11	Write Cycle Flowchart	5-28
5-12	CPU Space Address Encoding	5-30
5-13	Breakpoint Operation Flowchart	5-32
5-14	LPSTOP Interrupt Mask Level	5-33
5-15	Bus Arbitration Flowchart for Single Request	5-38
5-16	Preferred Circuit for Data Bus Mode Select Conditioning	5-42
5-17	Alternate Circuit for Data Bus Mode Select Conditioning	5-43
5-18	Power-On Reset	5-48
5-19	Basic MCU System	5-54
5-20	Chip-Select Circuit Block Diagram	5-55
5-21	CPU Space Encoding for Interrupt Acknowledge	5-60

Figure Number	Page Number
8-1 QADC Block Diagram	8-1
8-2 QADC Input and Output Signals	8-3
8-3 Example of External Multiplexing	8-11
8-4 QADC Module Block Diagram	8-13
8-5 Conversion Timing	8-14
8-6 Bypass Mode Conversion Timing	8-15
8-7 QADC Queue Operation with Pause	8-18
8-8 QADC Clock Subsystem Functions	8-24
8-9 QADC Clock Programmability Examples	8-26
8-10 QADC Conversion Queue Operation	8-29
8-11 QADC Interrupt Vector Format	8-33
9-1 QSM Block Diagram	9-1
9-2 QSPI Block Diagram	9-6
9-3 QSPI RAM	9-8
9-4 Flowchart of QSPI Initialization Operation	9-11
9-5 Flowchart of QSPI Master Operation (Part 1)	9-12
9-6 Flowchart of QSPI Master Operation (Part 2)	9-13
9-7 Flowchart of QSPI Master Operation (Part 3)	9-14
9-8 Flowchart of QSPI Slave Operation (Part 1)	9-15
9-9 Flowchart of QSPI Slave Operation (Part 2)	9-16
9-10 SCI Transmitter Block Diagram	9-24
9-11 SCI Receiver Block Diagram	9-25
10-1 CTM4 Block Diagram	10-1
10-2 CPSM Block Diagram	10-5
10-3 FCSM Block Diagram	10-6
10-4 MCSM Block Diagram	10-8
10-5 DASM Block Diagram	10-12
10-6 Pulse-Width Modulation Submodule Block Diagram	10-14
11-1 TPU Block Diagram	11-1
11-2 TCR1 Prescaler Control	11-14
11-3 TCR2 Prescaler Control	11-14
13-1 TouCAN Block Diagram	13-1
13-2 Typical CAN Network	13-2
13-3 Extended ID Message Buffer Structure	13-3
13-4 Standard ID Message Buffer Structure	13-4
13-5 TouCAN Interrupt Vector Generation	13-19
A-1 CLKOUT Output Timing Diagram	A-8
A-2 External Clock Input Timing Diagram	A-8
A-3 ECLK Output Timing Diagram	A-9
A-4 Read Cycle Timing Diagram	A-10
A-5 Write Cycle Timing Diagram	A-11



Figure Number	Page Number
A-6 Fast Termination Read Cycle Timing Diagram	A-12
A-7 Fast Termination Write Cycle Timing Diagram	A-13
A-8 Bus Arbitration Timing Diagram — Active Bus Case	A-14
A-9 Bus Arbitration Timing Diagram — Idle Bus Case	A-15
A-10 Show Cycle Timing Diagram	A-16
A-11 Chip-Select Timing Diagram	A-17
A-12 Reset and Mode Select Timing Diagram	A-17
A-13 Background Debugging Mode Timing — Serial Communication	A-18
A-14 Background Debugging Mode Timing — Freeze Assertion	A-18
A-15 ECLK Timing Diagram	A-20
A-16 QSPI Timing — Master, CPHA = 0	A-22
A-17 QSPI Timing — Master, CPHA = 1	A-22
A-18 QSPI Timing — Slave, CPHA = 0	A-23
A-19 QSPI Timing — Slave, CPHA = 1	A-23
A-20 TPU Timing Diagram	A-24
B-1 MC68336 Pin Assignments for 160-Pin Package	B-1
B-2 MC68376 Pin Assignments for 160-Pin Package	B-2
B-3 160-Pin Package Dimensions	B-3
D-1 User Programming Model	D-2
D-2 Supervisor Programming Model Supplement	D-3
D-3 TouCAN Message Buffer Address Map	D-82



