User's Manual

M9328MX1ADSUM/D
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M9328MX1ADS/A Application Development System

User's Manual

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Section 1 General Information

1.1 Description

This user's manual explains connection and operation of:

- The Motorola M9328MX1ADS/A DragonBall MX1 Application Development System (ADS) Standard Edition

This is a development tool which is designed to run software applications designed for DragonBall MX1 (MC9328MX1) microcontroller unit (MCU).

The M9328MX1ADS/A Standard Edition includes more than 15 interface ports or sockets that support application software, target-board debugging, or optional extra memory. It comes with a separate LCD display panel which includes the model LQ035Q7DB02 TFT LCD display from Sharp Corporation.

1.2 Features

MX1ADS features include:

- MC9328MX1 DragonBall MX1 MCU.
- Two clock-source crystals: 32 kilohertz and 16 megahertz.
- Voltage regulator that steps down the 3.0-volt VCC to the 1.8-volt QVDD core voltage.
- Two 8-megabyte × 16-bit Flash memory devices, configured as one 32-bit device.
- Two 16-megabyte × 16-bit SDRAM devices, configured as one 32-bit device.
- SODIMM connector for SDRAM or EIM memory expansion.
- Connectors for SD/MCC, Memory Stick, and SIM memory cards.

- Two UART ports, each with RS232 transceiver and DB9 connector.
- An IrDA transceiver that conforms to Specification 1.0 of the Infra-red Data Association.
- ISP1105W USB transceiver and series B USB connector
- Separate LCD panel assembly with a ribbon cable that connects to the main board and interfaces directly with the MC9328MX1ADS/A.
- Bluetooth RF module connector.
- CMOS Image Sensor (CSI) Connector.
- MultiICE and MultiTrace debug support connectors.
- DAC3550A CD Quality DAC that interfaces with SSI. System support includes two clock-source crystal oscillators and a 3.5mm speaker/headphone jack.
- Cirrus Logic CS8900A Ethernet controller, with a RJ-45 connector for connecting to a system hub.
- Microphone/voice interface amplifier circuity, with 3.5mm voice out and microphone in jacks.
- 32 × 3-pin DIN expansion connector with most MX1 I/O signals.
- LED indicators for power, external bus activity, Bluetooth data transfer, Ethernet activity, and two LEDs for user defined status indiction.
- Universal power supply with 3.0-volt output @1500ma.
- PC compatible USB cable.
- PC compatible RS232 serial cable.
- Metrowerks CodeWarrior™ IDE software (evaluation copy).

1.3 System and User Requirements

To use an M9328MX1ADS/A Application Development System, you need:

- An IBM PC or compatible computer that has:
  - a Windows® 98, Windows ME™, Windows XP™, Windows 2000, or Windows NT® (version 4.0) operating system.

  - a parallel port if you are using a MultiICE device

    or

  - an RS-232 serial port, capable of operation at 9600 to 115200 bits per second operation, if you are using MetroTRK.

- A + 3.0-volt-to +3.3-volt power supply, at 1500mA, with a 2mm female (inside positive) power connector (included).
- An RS-232 cable (DB9 male-female, included) for connecting to the internal UART while using bootstrap mode or Metrowerks' MetroTRK.
- Hyperterminal (or a comparable terminal-emulation program) for downloading the MetroTRK image to MX1ADS Flash memory.

CAUTION: *Never supply more than +3.3-volts power to your MX1ADS. Doing so could damage board components.*

1.4 MX1ADS Diagram

Figure 1-1 shows the connectors and other major parts of the M9328MX1ADS/A.

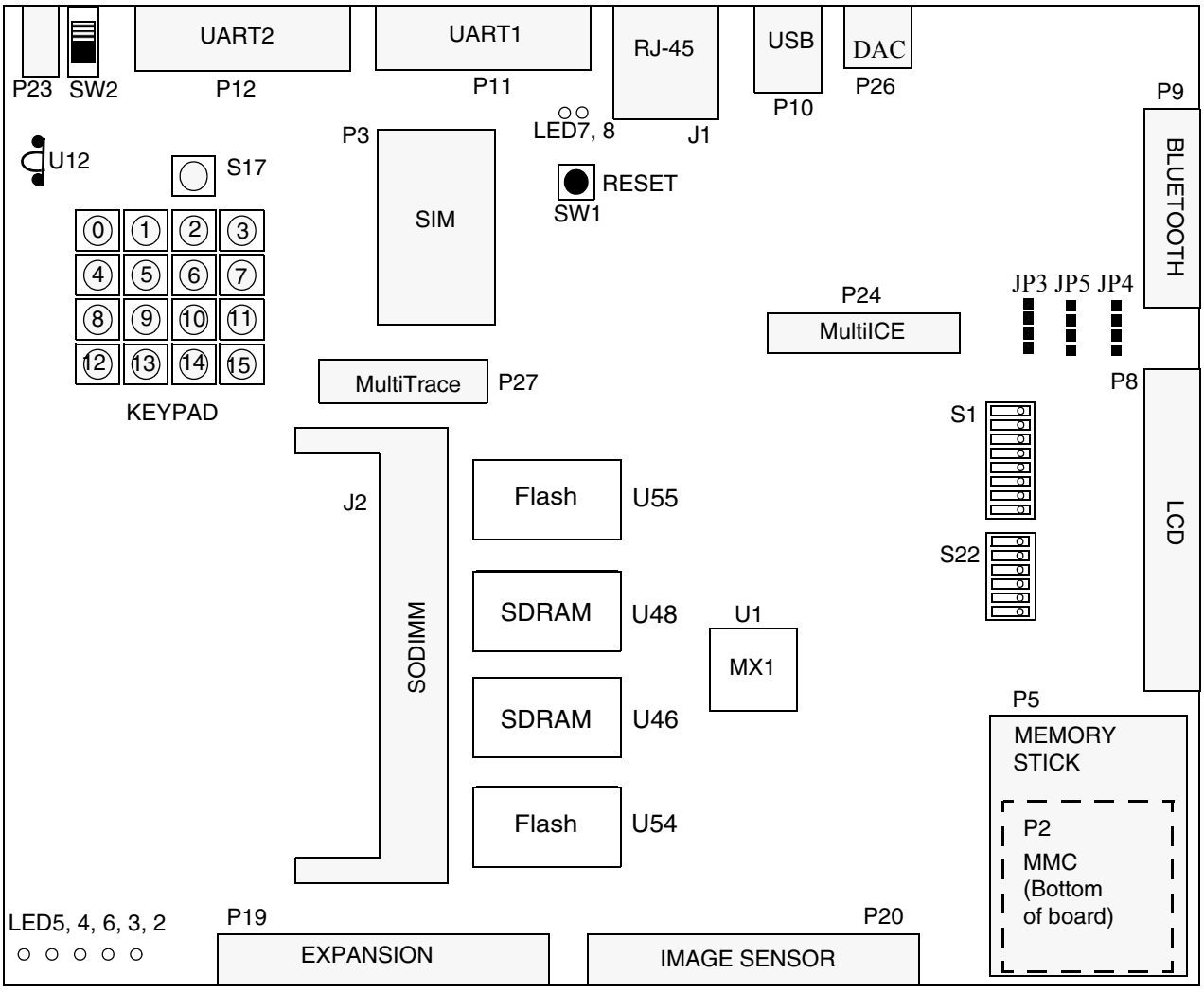


Figure 1-1 M9328MX1ADS/A Application Development System

Important board components are:

- U1 — DragonBall MX1 MCU

- P2 — SD/MCC connector (on bottom of board)
- P3 — SIM card connector
- P5 — Memory Stick connector
- P8 — LCD/touch panel connector
- P9 — BlueTooth connector
- P10 — USB connector
- P11, P12 — RS232 connectors to on chip UARTs
- P26 — DAC out connectors
- P19 — I/O expansion connector
- P20 — image sensor connector
- P23 — 3.0-volt input power connector
- P24 — ARM MultiICE connector
- P27 — ARM MutliTrace connector
- J1 — RJ-45 Ethernet connector
- J2 — Custom SODIMM memory expansion connector
- S1 — peripherals enable switches
- S5 - S16, S18 - S21 — 16 push button keypad keys
- S17 — General function push button switch
- S22 — boot and big/little endian mode select switch
- SW1 — reset switch
- SW2 — power switch
- LED2 and LED3 — general-purpose LEDs (yellow)
- LED4 — external bus activity LED (red)
- LED5 — power LED (green)
- LED6 — Bluetooth activity LED (yellow)
- LED7, LED8 — Ethernet activity LEDs (green, orange)
- U12 — IrDA transceiver

1.5 Specifications

Table 1-1 lists M9328MX1ADS/A specifications

Table 1-1 Specifications

Characteristic	Specifications
Clock speed	96/48 MegaHertz
Ports	10Base-T (RJ-45), RS-232 serial
Temperature operating storage	 -10° to +50° C -40° to +85° C
Relative humidity	0 to 90% (noncondensing)
Power requirements	3.0V — 3.3 VDC at 1 A
Dimensions	7.28 x 6.0 inches (18.5 x 15.3centimeters)

Section 2 Configuration and Operation

2.1 Introduction

This section consists of configuration information, connection descriptions, and other operational information that may be useful in your development activities.

2.2 Configuring Board Components

Table 2-1 is a summary of configuration settings; subsections 2.2.1 through 2.2.2 give additional information.

Table 2-1 Component Configuration Settings

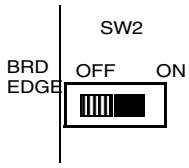
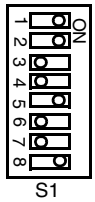
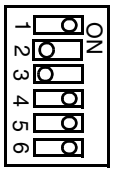
Component	Position	Effect
System Power Switch, SW2		Move this switch to the ON position to enable the power source connected to P23 to power the system. Factory setting is OFF.
System Reset Switch, SW1		Push to reset the MX1ADS.
Peripheral Selection Switch, S1		Enables UART1 transceiver, UART2 transceiver, Flash memory, and the buzzer. Disables IrDA module. Factory setting is shown. Subsection 2.2.1 explains other settings for this switch.

Table 2-1 Component Configuration Settings (Continued)

Component	Position	Effect
Mode Switch, S22	S22  S22	Configures 32-bit Flash as the boot device, configures Little Endian mode, and Normal mode operation. Factory setting is shown Subsection 2.2.2 explains other settings for this switch.

2.2.1 Peripheral Selection Switch (S1)

Switch S1 enables or disables the UART transceivers, the IRDA buffers, and the buzzer.

Table 2-2 lists the functionality of these subswitches.

.

Table 2-2 S1 Subswitch Settings

Subswitch, Function	Setting	Effect
S1-1, UART1 transceiver	ON	Forces the UART1 transceiver to be enabled.
	OFF	UART1_EN bit of U42 controls the UART1 transceiver. Active low.*
S1-2, UART2 transceiver	ON	Forces the UART2 transceiver to be enabled.**.
	OFF	UART2_EN bit of U42 controls the UART2 transceiver. Active low.*
S1-3, IrDA module	ON	Forces the IrDA module buffers to be enabled.**
	OFF	IrDA_EN bit of U42 controls the IrDA buffers. Active low.*
S1-4, LCD	ON	Forces the LCD to be enabled.
	OFF	LCD_ON bit of U42 controls the power regulator on the LCD board. Active low.
S1-5, Buzzer	ON	Enables the buzzer to be controlled by the PWMO output.
	OFF	PMWO is disconnected from the buzzer circuit.
S1-6, PEN_CS	—	No effect
S1-7, PEN_IRQ	—	No effect

Table 2-2 S1 Subswitch Settings

Subswitch, Function	Setting	Effect
S1-8	ON	Flash memory is connected to $\overline{CS0}$
	OFF	Flash memory is disabled, CS0 is no longer connected to Flash.

* Setting the associated bit high (power on reset default) disables the interface. Setting the bit low will enable the interface.

** ***Warning:*** *Do not enable UART2 and IRDA at the same time. Neither circuit will function properly and circuit damage could result.*

Figure 2-1 shows a possible configuration: the UART1 transceiver, Flash memory, and the IrDA module enabled; the UART2 transceiver and buzzer disabled.

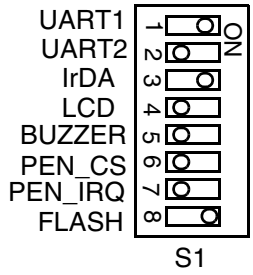


Figure 2-1 Switch S1

2.2.2 Mode Switch (S22)

Switch S22 configures boot mode, configures endian state, and enables test mode. These switches only take effect on power up or after a reset is applied.

Table 2-3 lists settings for the boot-mode subswitches, S22-1 through S22-4. Table 2-4 lists the settings for subswitches S22-5 and S22-6.

Table 2-3 Boot Mode Subswitch Settings

Boot Mode, Device	S22-4 Boot 3	S22-3 Boot 2	S22-2 Boot 1	S22-1 Boot0
Internal bootstrap ROM	ON	ON	ON	ON

Table 2-3 Boot Mode Subswitch Settings

Boot Mode, Device	S22-4 Boot 3	S22-3 Boot 2	S22-2 Boot 1	S22-1 Boot0
16-bit, D[15—0] SyncFlash on CS3	ON	ON	ON	OFF
32-bit SyncFlash on CS3	ON	ON	OFF	ON
8-bit, D[7—0] on CS0	ON	ON	OFF	OFF
16-bit, D[32—16] on CS0	ON	OFF	ON	ON
16-bit, D[15—0] on CS0	ON	OFF	ON	OFF
32-bit on CS0	ON	OFF	OFF	ON

Table 2-4 Subswitch S22-5, S22-6 Settings

Subswitch, Function	Setting	Effect
S22-5, Endian mode	ON	Configures Little Endian mode.
	OFF	Configures Big Endian mode.
S22-6, CPU Mode	ON	Selects Normal mode.
	OFF	Selects CPU Test mode.

Warning: *Do not select CPU Test mode. Nothing good will come of it.*

Figure 2-2 shows a possible configuration:

- Subswitches S22-1 through S22-4 configure the boot mode to be CS0, 8-bit, D[7] through D[0].
- Subswitch S22-5 configures Little Endian mode.
- Subswitch S22-6 selects Normal mode.

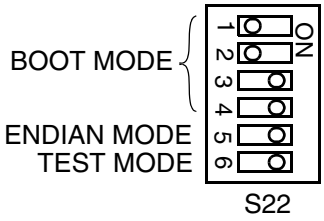


Figure 2-2 Switch S22

2.3 Operation

2.3.1 Functional Block Diagram

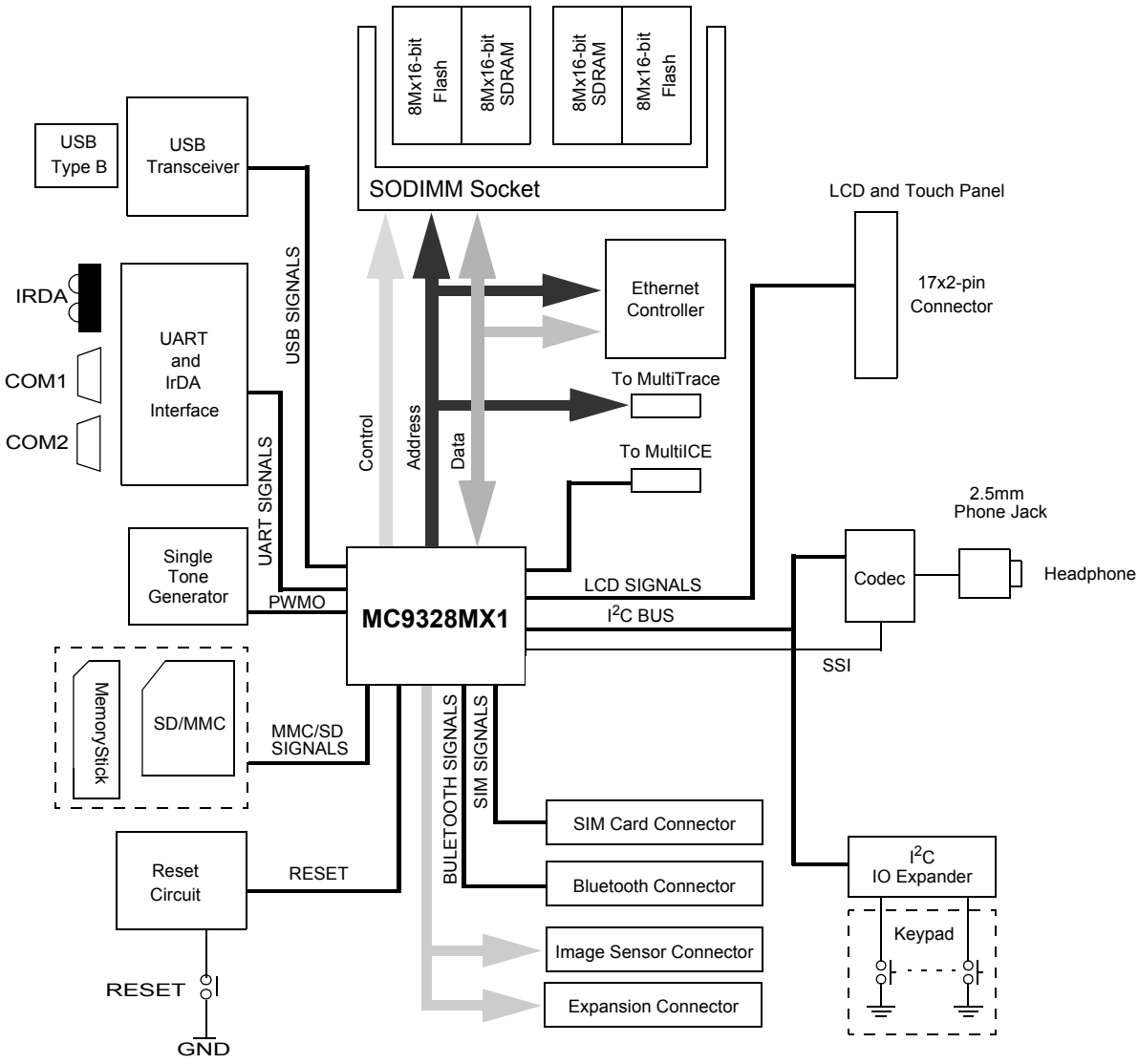


Figure 2-3 Functional Block Diagram of MX1ADS

2.3.2 On Board Memory

Figure 2-4 and Figure 2-5 show the interface of the on-board memory. The ADS is equipped with 8Mx32-bit Flash and 16Mx32-bit SDRAM. The chip select $\overline{CS0}$ and $\overline{CS2}$ ($\overline{CSD0}$) are used for Flash and SDRAM chip selects respectively. Furthermore S1-8 can disable Flash memory by disconnecting $\overline{CS0}$, making $\overline{CS0}$ available for other functions.

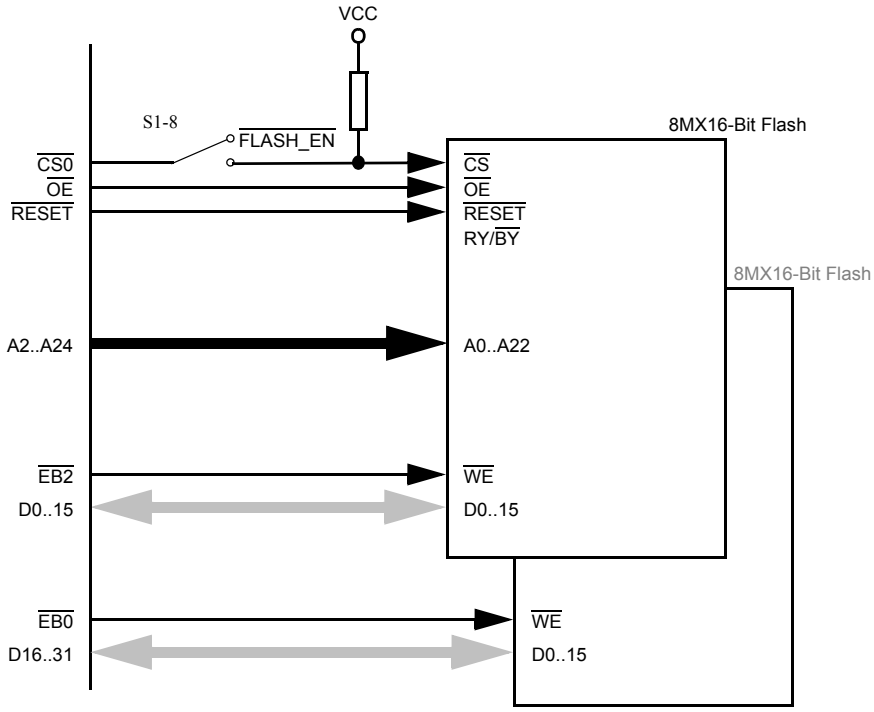


Figure 2-4 Flash Interface

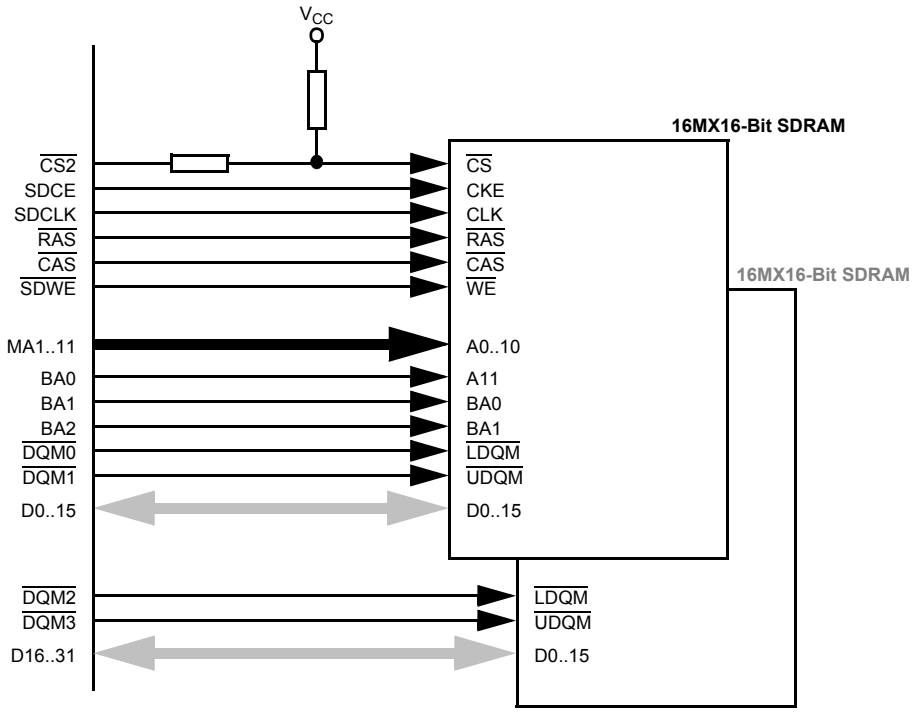


Figure 2-5 SDRAM Interface

2.3.3 Memory Map

Table 2-5 represents the memory mapping for the external peripherals on the M9328MX1ADS/A board. Note the Ethernet Controller has repeated memory blocks due to the fact it does not take up the entire address space of the associated chip select, $\overline{CS4}$. This chip select covers 16 MB allowing many repetitions of the Ethernet Controller's internal registers.

Table 2-5 M9328MX1ADS/A Memory Map

Peripheral	Chip Select	Address Range (HEX)	Act Mem Size
SDRAM	$\overline{CS2}$ ($\overline{CSD0}$)	0x0800 0000 to 0x0BFF FFFF	64MB
Flash	$\overline{CS0}$*	0x1000 0000 to 0x11FF FFFF	32MB
Ethernet Controller	$\overline{CS4}$	0x1500 0000 to 0x15FF FFFF	16 BYTES
Internal SRAM	NA	0x0030 0000 to 0x0031 FFFF	128 KB

* S1-8 must be on to enable CS0 to control the Flash

2.3.4 USB Interface

The USB Device Module of the MC9328MX1 interfaces the with a Phillips USB transceiver, ISP1105W, connected to a USB type B connector, P10. For details on the operation of USB interface, please refer to MC9328MX1 data sheet. Figure 2-6 illustrates the USB interface connection.

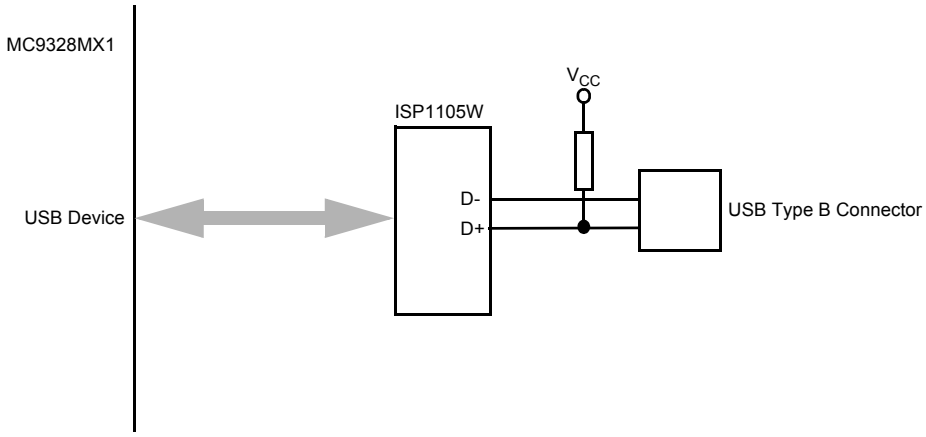


Figure 2-6 USB Interface

2.3.5 UART and IrDA

Figure 2-7 shows how the UART and the IrDA circuits are connected.

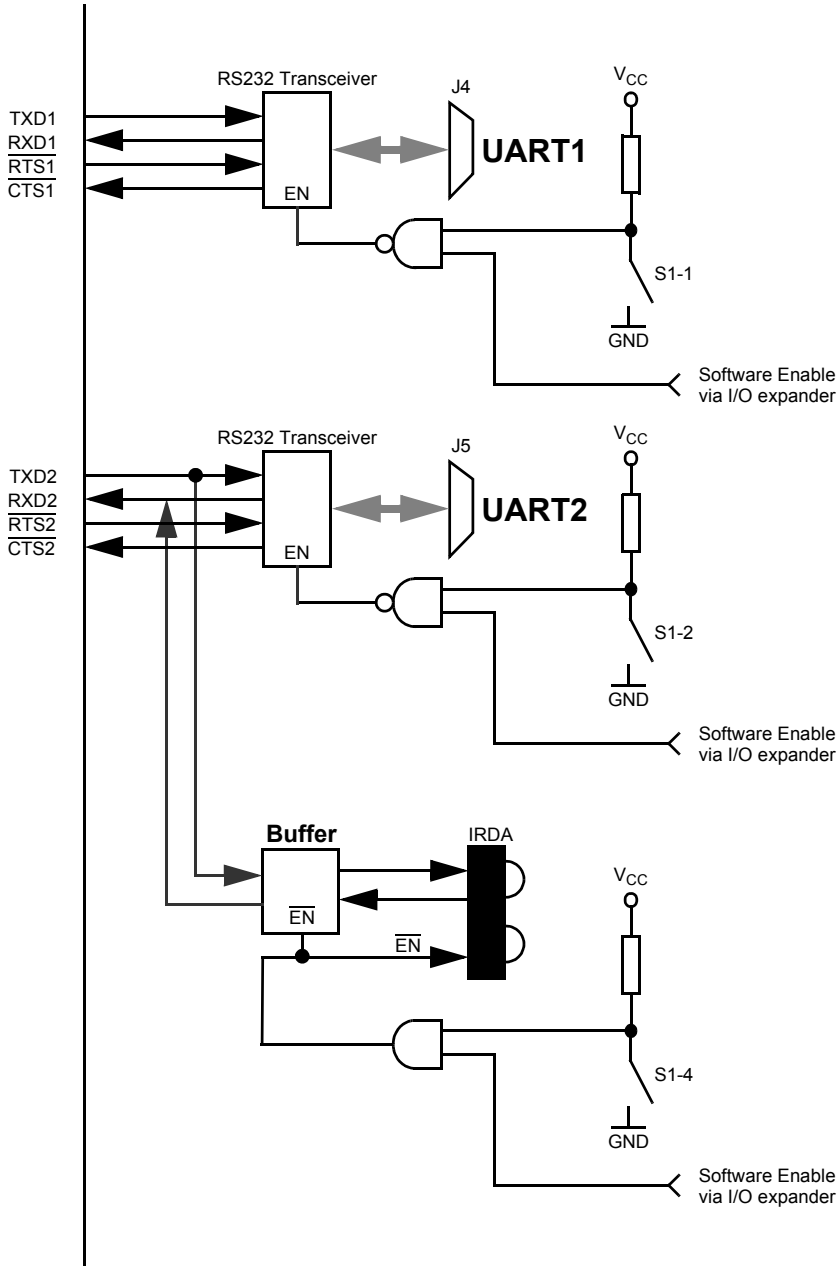


Figure 2-7 UARTs and IrDA Interface

2.3.6 Ethernet

The M9328MX1ADS/A is equipped with Cirrus Logic CS8900A Crystal LAN ISA Ethernet Controller. The CS8900A has 10BaseT transmit and receive filters and can interface with the M9328MX1. The CS8900A is operating in I/O mode. A serial EEPROM (AT93C46A) is provided in the ADS to store initial configuration for the CS8900A. Figure 2-8 shows an overview of the Ethernet interface.

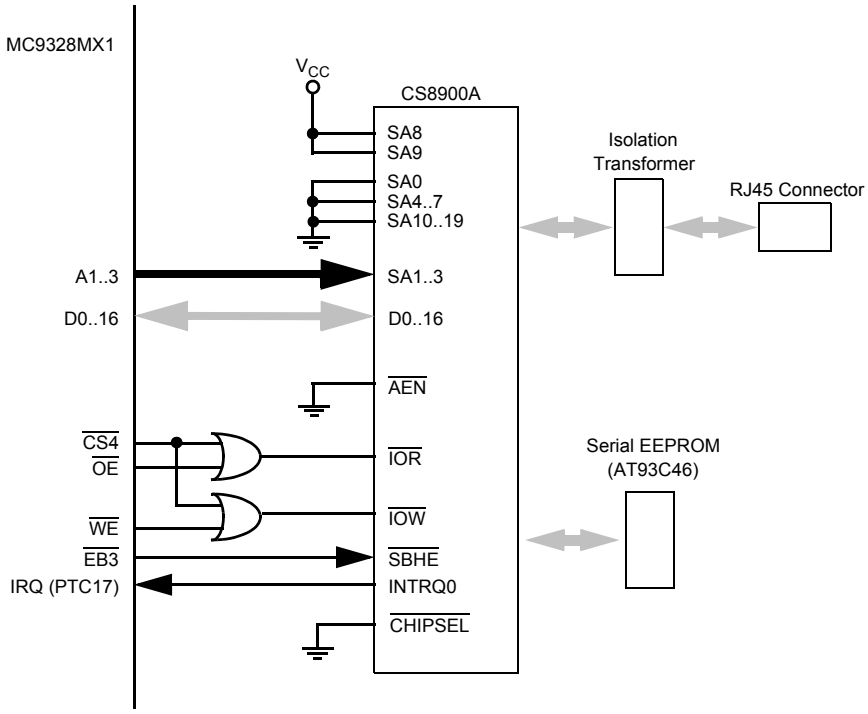


Figure 2-8 Ethernet Interface

2.3.7 CD Quality DAC

The M9328MX1ADS/A is equipped with Micronas Stereo Audio DAC. The DAC3350A, U32, is controlled by the MX1 which sends the DAC digital audio data via the I^2C bus. The I^2C slave address of the DAC3350A is 0x9A.

The DAC also provides volume control and a headphone amplifier output. This amplifier is connected to the P26 audio connector. A filtered low level audio output is connected to the JP3 header.

The mixing of external analog audio sources to the converted DAC signal is supported. These signals can be input at the JP4 and JP5 headers. Table 2-6 through Table 2-8 describe the header pin outs.

Table 2-6 Audio Header JP3 Signal Descriptions

Pin	Mnemonic	Signal
1	FINR	Filtered op amp output right, line out
2,3	AGND	Analog Ground
4	FINL	Filtered op amp output left, line out

Table 2-7 Audio Header JP4 Signal Descriptions

Pin	Mnemonic	Signal
1	AUX1R	Auxiliary Input 1, right channel
2,3	AGND	Analog Ground
4	AUX1L	Auxiliary Input 1, left channel

Table 2-8 Audio Header JP5 Signal Descriptions

Pin	Mnemonic	Signal
1	AUX2R	Auxiliary Input 2, right channel
2,3	AGND	Analog Ground
4	AUX2L	Auxiliary Input 2, left channel

For the details on the operation of DAC3550A, please refer to its data sheet. The data sheet is available on the web:

http://www.micronas.com/

2.3.8 Keypads and IO Expander

The M9328MX1ADS/A is equipped with two Phillips PCF8575 I/O expanders. One is for the keypad array and the other is for peripheral control. The keypad array consist of a matrix of momentary push button switches mounted directly to the ADS board. Figure 2-9 and Table 2-9 shows the interface of the I/O expander to the keypads. The read slave address is 0x49. The PCF8575 can be used to generated an interrupt whenever a key is pressed or released. The interrupt signal is connected to the SIM_PD signal of the MX1 which should be configured as GPIO, PB15. There is an additional push button switch, S17, that is connected to the SPI_RDY signal of the MX1. That pin should be configured as GPIO, PC13, to use it with S17. When any switch is depressed it will cause a low (zero) to appear at the associated input pin. These switches have no hardware debounce so that function must be handled by the software.

Table 2-10 and Figure 2-10 shows the interface to software controlled peripheral enables. Peripherals can be enable or disable by programming the I/O expander. This depends on the state of the associated enable switch (S1) which can override software control. The write slave address is 0x44 and the read address is 0x45.

The PCF8575 consists of a 16-bit quasi-bidirectional port and an I^2C-bus interface. On power up all pins are configured as inputs. A non power up reset has no effect on the PCF8575 which communicates with the MC9328MX1 through the I^2C interface. For the details on the operation of PCF8575, please refer to its data sheet. The data sheet is available on the web:

http://www.semiconductors.philips.com

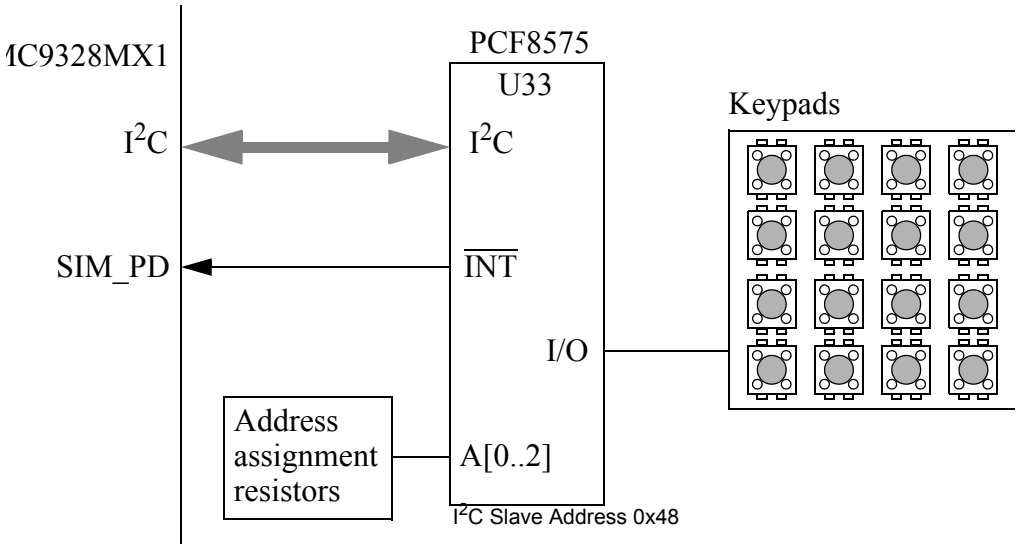


Figure 2-9 Keypads and I/O Expander Interface

Table 2-9 Keypad I/O Expander Interface

I/O Expander Port	Key Read	I/O Expander Port	Key Read
P00	Key 0 / S8	P10	Key 8 / S16
P01	Key 1 / S7	P11	Key 9 / S15
P02	Key 2 / S6	P12	Key 10 / S14
P03	Key 3 / S5	P13	Key 11 / S13
P04	Key 4 / S12	P14	Key 12 / S21
P05	Key 5 / S11	P15	Key 13 / S20
P06	Key 6 / S10	P16	Key 14 / S19
P07	Key 7 / S9	P17	Key 15 / S18

Table 2-10 I/O Expander to Peripherals (U42)

I/O Expander Port	Mnemonic	Signal
P00	UART1_EN	UART1 enable
P01	UART2_EN*	UART2 enable*

Table 2-10 I/O Expander to Peripherals (U42)

I/O Expander Port	Mnemonic	Signal
P02	IrDA_EN*	IrDA enable*
P03	LCD_ON	Not used (reserved)
P04	BTRF_EN	Not used (reserved)
P05	SD_SPI_EN	Enables SPI interface to the SD/MMC card connector
P06,P07, P12-P17	NC	NO CONNECTION
P10	SD_WP	Secure Data Write Protect
P11	SD_CD	Secure Data Card Detect (In default state, this signal is disconnected by a zero ohm resistor.)

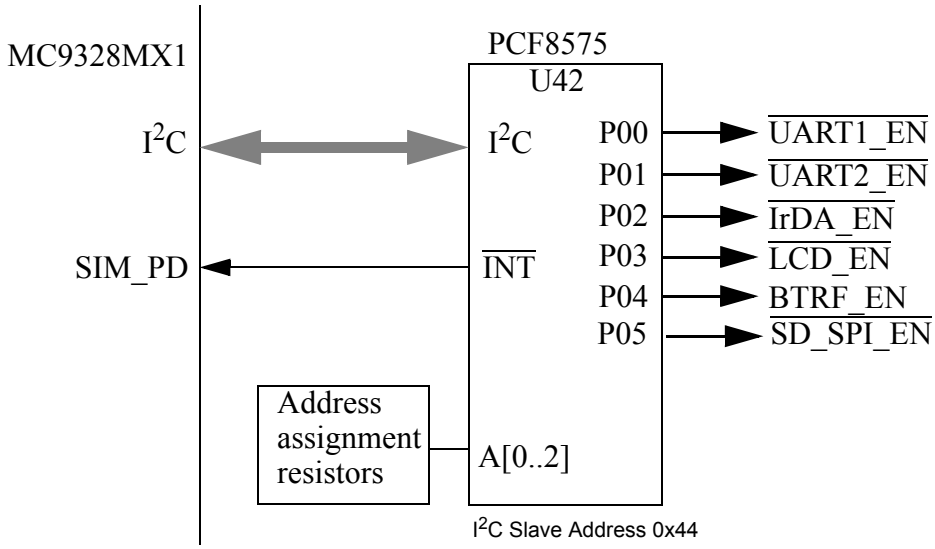


Figure 2-10 Software Controlled Peripheral Enables

2.3.9 Led Indicators

Table 2-11 lists the meanings of the MX1ADS LED indicators.

Table 2-11 Function of LED Indicators

Reference #	Color	Name	Function
LED2	Yellow	PA2	User status controlled by PA2*
LED3	Yellow	PA23	User status controlled by PA23*
LED4	Red	EXT BUS	Blinking indicates external bus activity
LED5	Green	PWR	Power is applied to the system with right polarity
LED6	Yellow	BTA	Blinking indicates Bluetooth activity
LED7	Green	ACTIVE	Blinking indicates LAN Activity
LED8	Orange	LINK	Link good or host controlled output 0

* A logic high level at the controlling pin will turn on the LED. A logic low turns it off. The schematic shows LED2 connected to PWMO and LED3 connected to $\overline{CS5}$ which are alternate functions for PA2 and PA23.

2.4 Using The Board Connectors

Table 2-12 lists the MX1ADS connectors, explaining their function, and any special instructions for using the connector. Figure 1-1 shows the connector locations on the board along with their reference designators.

Table 2-12 MX1ADS Connectors

Connector	Purpose	Comments
J1	Ethernet	Standard Ethernet connector.
J2	SODIMM	Slide the SODIMM card into the connector until it snaps into place. Not compatible with off the shelf DIMM modules.

Table 2-12 MX1ADS Connectors (Continued)

Connector	Purpose	Comments
JP3	FOUTR, FOUTL	Filtered output of right and left channels from the DAC3550A.
JP4	AUX1R, AUX1L,	Auxiliary audio input channel 1 with left and right stereo inputs. Compatible with low level outputs of most audio electronics.
JP5	AUX2R, AUX2L	Auxiliary audio input channel 2 with left and right stereo inputs. Compatible with low level outputs of most audio electronics.
P2	SD/MMC	Connector is on bottom of board, directly below the P5 memory stick connector. Slide the MMC unit into the connector until it snaps into place. Shares signals with the Memory Stick card interface.
P3	SIM	Unsnap latch, swing lid up. Slide SIM card inside, matching alignment of contacts at the connector base. Close the lid and push down to latch.
P5	Memory Stick	Slide the memory stick into the connector until it snaps into place. Shares signals with the SD/MMC card interface.
P8	LCD panel	Connect LCD ribbon cable between this connector and the corresponding connector of the LCD display panel, J11.
P9	BlueTooth module	Connect a compatible Bluetooth daughter board into this connector.
P10	USB	Standard USB connector.
P11	UART1	Standard DB9 connector set up for DCE operation.
P12	UART2	Standard DB9 connector set up for DCE operation.
P19	Expansion	Standard 48 pin, three row, male DIN connectors. Can connect directly or be cabled to a custom circuit board.
P20	Image sensor	Connect an image-sensor daughter board to this connector.
P23	Power	Plug the 3-volt power-supply jack end into this connector.
P24	MultiICE	Standard ARM MultiICE connector.*
P26	Headphone	Standard 3.5 mm connector for stereo audio. This is the amplified stereo output of the DAC3550A. Use headphones with a 16 to 32 ohms impedance.
P27	MultiTrace	Standard ARM MultiTrace connector.*

* For information on ARM supplied devices that are compatible with these connectors please visit ARM's web site at: http://www.arm.com

2.5 Add On Module Connections and Usage

2.5.1 Using the TFT LCD Display Panel

Your MX1ADS come equipped with a touch control enabled TFT (Thin Film Transistor) LCD display assembly. The TFT LCD component is from Sharp Corporation, model number LQ035Q7DB02 . A detailed specification has been included on the documentation CD that came with your ADS.

To begin using your MX1ADS LCD module you must connect the 34 conductor ribbon cable (RE11057C) that came with your MX1ADS between connectors J11 on the LCD module and P8 on the MX1ADS main board.

Warning: *Be sure input power to the main board is disconnected or switched off before the LCD module is connected. Connecting the module with power applied could damage the LCD module and/or the main board.*

The potentiometer VR1 which is to the left of the LCD panel just below J11 is used to control flickering of the display screen. This control is set at the factory and should not require any adjustment. However should your TFT LCD module exhibit flickering you may correct it by adjusting this control. You will need to use a suitable flat head or phillips head screwdriver. This may be done with power applied but caution is advised when using a metal tool. A plastic bladed tools is recommend.

2.5.2 Using a SODIMM Card

This connector provide a way to add new circuit boards that may be developed in the future. Users can also develop compatible DIMM cards as well.

Caution should be used when developing such boards to avoid addressing conflicts with peripherals that already exits on the main board.

Warning: *To avoid circuit damage, do not plug in SODIMM cards with power applied to the board.*

2.5.3 Using a SIM, SD/MMC, or Memory Stick Card

The users must obtain their own compatible cards for use with these connectors. Please note the power is connected to VCC which is 3.0-volts when using the power supply provide with your kit.

Warning: *To avoid circuit damage, do not plug in SIM, SD/MMC, or Memory Stick cards with power applied to the board.*

2.5.4 Using the BlueTooth Daughter Board

This connector, P9, comes configured to operate directly with the Motorola Bluetooth RF module that is not included in the M9328MX1ADS/A. There are zero ohm resistor components that may be removed and/or added to change what signals are connected. This can be used to adapt the connector to other RF modules from other vendors.

2.5.5 Using Image Sensor Daughter Boards

This connector can be configured to operate directly with third party Image Sensor daughter boards. The communication with theses cards takes place through the I^2C interface.

Section 3 Support Information

3.1 Introduction

This section consists of connector pin assignments, connector signal descriptions, and other information that may be useful in your development activities.

3.2 S.O.DIMM Socket

Connector J2 is the MX1ADS SODIMM connector. Figure 3-1 gives pin assignments for this connector and Table 3-1 gives signal descriptions for this connector. Please note this in not an industry standard pin out and that it is unlikely to be compatible with off the self DIMM cards

J2

GND	1	2	GND
D0	3	4	~EB0
D1	5	6	~EB1
D2	7	8	~EB2
D3	9	10	~EB3
VCC	11	12	VCC
D4	13	14	~OE
D5	15	16	~WE
D6	17	18	~ECB
D7	19	20	~LBA
GND	21	22	GND
DQM0	23	24	A0
DQM1	25	26	A1
VCC	27	28	VCC
A2	29	30	A5
A3	31	32	A6
A4	33	34	A7
GND	35	36	GND
D8	37	38	~BAA
D9	39	40	~BCLK
D10	41	42	NC
D11	43	44	NC
VCC	45	46	VCC
D12	47	48	~CS0
D13	49	50	~CS1
D14	51	52	~CS4
D15	53	54	~CS5
GND	55	56	GND
~RESETSF	57	58	MOSI
MISO	59	60	SS
SDCLK	61	62	SDCKE0
VCC	63	64	VCC
~RAS	65	66	~CAS
~SDWE	67	68	SDCKE1
~CS2	69	70	A13
~CS3	71	72	SPI_RDY
~RESET	73	74	SDCLK
GND	75	76	GND
CLKOUT	77	78	SIM_TX
NC	79	80	SIM_RX
VCC	81	82	VCC

D16	83	•	•	84	SIM_SVEN
D17	85	•	•	86	SIM_PD
D18	87	•	•	88	SIM_CLK
D19	89	•	•	90	SIM_RST
GND	91	•	•	92	GND
D20	93	•	•	94	A16
D21	95	•	•	96	A17
D22	97	•	•	98	A18
D23	99	•	•	100	A19
VCC	101	•	•	102	VCC
A8	103	•	•	104	A9
A10	105	•	•	106	NC*
GND	107	•	•	108	GND
MA10	109	•	•	110	NC*
MA11	111	•	•	112	NC*
VCC	113	•	•	114	VCC
DQM2	115	•	•	116	A11
DQM3	117	•	•	118	A12
GND	119	•	•	120	GND
D24	121	•	•	122	A14
D25	123	•	•	124	A15
D26	125	•	•	126	A20
D27	127	•	•	128	A21
VCC	129	•	•	130	VCC
D28	131	•	•	132	A22
D29	133	•	•	134	A23
D30	135	•	•	136	A24
D31	137	•	•	138	NC
GND	139	•	•	140	GND
NC	141	•	•	142	NC
VCC	143	•	•	144	VCC

Figure 3-1 SODIMM Connector J2 Pin Assignments

*These connector pins may be connected to address lines with the addition of a zero ohm resistor. For more details please refer to the M9328MX1ADS/A schematic, sheet 11 of 14.

Table 3-1 SODIMM Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1, 2, 21, 22, 35, 36, 55, 56, 75, 76, 91, 92, 107, 108, 119, 120, 139, 140	GND	GROUND

Table 3-1 SODIMM Connector J2 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
3, 5, 7, 9, 13, 15, 17, 19, 37, 39, 41, 43, 47, 49, 51, 53, 83, 85, 87, 89, 93, 95, 97, 99, 121, 123, 125, 127, 131, 133, 135, 137	D0 — D31	DATA BUS (lines 0—31) — Bidirectional signals for transferring data between the processor and an external device.
4, 6, 8, 10	~EB0 — ~EB3	ENABLE BYTE (lines 0—3) — Active-low outputs that indicate active data bytes for the current access. ~EB0 corresponds to DATA[31—24], ~EB1 corresponds to DATA[23—16], ~EB2 corresponds to DATA[15—8], and ~EB3 corresponds to DATA[7—0]
11, 12, 27, 28, 45, 46, 63, 64, 81, 82, 101, 102, 113, 114, 129, 130, 143, 144	VCC	VCC (3.0-volts)
14	~OE	OUTPUT ENABLE — Active-low output that indicates that a bus access is a read access; enables slave devices to drive the data bus.
16	~WE	WRITE ENABLE — Active-low output
18	~ECB	END CURRENT BURST — Active-low input signal asserted by external burst devices; indicates the end of a burst sequence
20	~LBA	LOAD BURST ADDRESS — Active-low signal asserted during burst mode accesses; causes the external burst device to load a new starting burst address
23, 25, 115, 117	DQM0 — DQM3	SDRAM enable bytes (0-3) - Active-low output signals.
24, 26, 29 — 34, 70, 94, 96, 98, 100, 103 — 105, 116, 118, 122, 124, 126, 128, 132, 134, 136	A{0 — A24 (not in exact order)	ADDRESS BUS (0-24) - Output lines for addressing external devices.
38	~BAA	BURST ADDRESS ADVANCE — Active-low signal asserted during burst mode accesses; causes the external burst devices to increment internal burst counters.
40	~BCLK	BURST CLOCK — Output signal to external burst devices; synchronizes burst loading and incrementing
42, 44, 77, 79, 106, 110, 112, 138, 141, 142	NC	NO CONNECTION

Table 3-1 SODIMM Connector J2 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
48, 50, 52, 54, 69, 71	~CS0—~CS5 (not in exact order)	CHIP SELECTS (lines 0 - 5) - Chip-select signals, active-low outputs.
57	~RESETSF	RESET Flash - Active low output
58	MOSI	MASTER OUT / SLAVE IN - SPI data signal (bidirectional)
59	MISO	MASTER IN / SLAVE OUT - SPI data signal (bidirectional)
60	SS	SLAVE SELECT - bidirectional, active low, input in slave mode, output in master mode
61, 74	SDCLK	SDRAM clock - output to SDRAM
62, 68	SDCKE0, SDCKE1	SDRAM CLOCK ENABLE 0 & 1 - Active high outputs to SDRAM
65	~RAS	ROW ADDRESS STROBE -clocks row address to SDRAM
66	~CAS	COLUMN ADDRESS STROBE - clocks column address to SDRAM
67	SDWE	SDRAM WRITE ENABLE - write data strobe to SDRAM, active low
72	SPI_RDY	SPI READY - CSPI serial burst trigger, active low input
73	~RESET	RESET — Active-low reset signal to the processor
78,80	SIM_TX,SIM_RX	SIM TRANSMITTED/ SIM RECEIVED DATA - SIM card data, tied together externally through zero ohm resistor.
84	SIM_SVEN	SIM VCC ENABLE - enable power to the SIM card, active low
86	SIM_PD	SIM PRESENCE DETECT - Active low input
88	SIM_CLK	SIMCLOCK - output clock to SIM card
90	SIM_RST	SIM RESET - Active low output to SIM card
109, 111	MA10, MA11	MUXED ADDRESS 10 & 11 - Multiplexed addresses to SDRAM

3.3 UART Connectors

Connectors P11 and P12 are the MX1ADS UART connectors. Figure 3-2 gives the pin assignments and Table 3-2 gives the signal descriptions for UART1 connector P11 and UART2 connector P12.

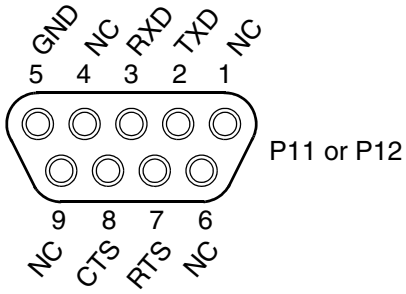


Figure 3-2 Connector P11 (UART1), P12 (UART2) Pin Assignments

Table 3-2 Connector P11 (UART1), P12 (UART2) Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 6, 9	NC	NO CONNECTION
2	TXD	TRANSMITTED DATA — RS232 serial data output signal.
3	RXD	RECEIVED DATA – RS232 serial data input signal.
5	GND	GROUND
7	RTS	READY TO SEND — Active-positive, RS232 input signal.
8	CTS	CLEAR TO SEND — Active-positive RS232 output signal.

***Waning**: UART2 can not be used if IrDA is enabled.*

3.4 MultiICE Connector

Connector P24 is the MX1ADS MultiICE connector. Figure 3-3 gives the pin assignments and Table 3-3 gives the signal descriptions for this connector.

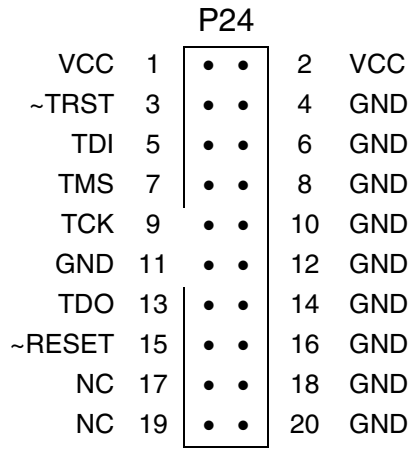


Figure 3-3 MultiICE Connector P24 Pin Assignments

Table 3-3 MultiICE Connector P24 Signal Descriptions

Pin	Mnemonic	Signal
1, 2	VCC	3.0-VOLT POWER
3	~TRST	TARGET RESET — Active-low output signal that resets the target.
4, 6, 8, 10 — 12, 14, 16, 18, 20	GND	GROUND
5	TDI	TEST DATA INPUT — Serial data output line, sampled on the rising edge of the TCK signal.
7	TMS	TEST MODE SELECT – Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
9	TCK	TEST CLOCK — Output timing signal, for synchronizing test logic and control register access.
13	TDO	JTAG TEST DATA OUTPUT — Serial data input from the target.
15	~RESET	RESET — Active-low reset signal.
17, 19	NC	NO CONNECTION

3.5 Ethernet Connector

Connector J1 is the RJ-45 MX1ADS Ethernet connector. Figure 3-4 gives the pin assignments and Table 3-4 gives the signal descriptions for this connector.

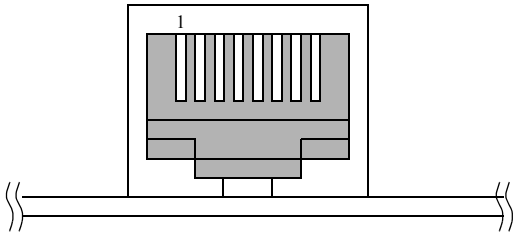


Figure 3-4 Ethernet Connector J1 Pin Assignments

Table 3-4 Ethernet Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1	TPO+	DIFFERENTIAL OUTPUT PLUS
2	TPO-	DIFFERENTIAL OUTPUT MINUS
3	TPI+	DIFFERENTIAL INPUT PLUS
4, 5, 7, 8	NC	NO CONNECTION
6	TPI-	DIFFERENTIAL INPUT MINUS
9,10	GND	GROUND

3.6 USB Connector

Connector P10 is the USB connector. Figure 3-5 gives the pin assignments and Table 3-5 gives the signal descriptions for this connector.

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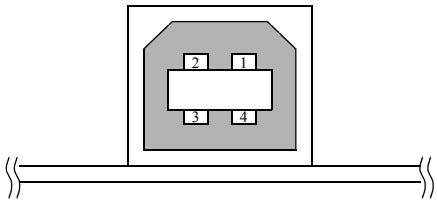

Figure 3-5 USB Connector P10 Pin Assignments

Table 3-5 USB Connector P10 Signal Descriptions

Pin	Mnemonic	Signal
1	NC	NO CONNECTION
2	D-	USB DATA MINUS

Table 3-5 USB Connector P10 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
3	D+	USB DATA PLUS
4	GND	GROUND

3.7 BlueTooth Connector

M9328MX1ADS/A provides a 20-pin connector, P9, for interfacing the MC9328MX1 with Motorola bluetooth Module.

The selection of the used interface is determined via software by programming internal registers. Note on the schematic several zero ohm resistors allow the user to reconfigure the pin out to accommodate a different RF module. Figure 3-6 gives the pin assignments and Table 3-6 gives the signal descriptions for this connector.

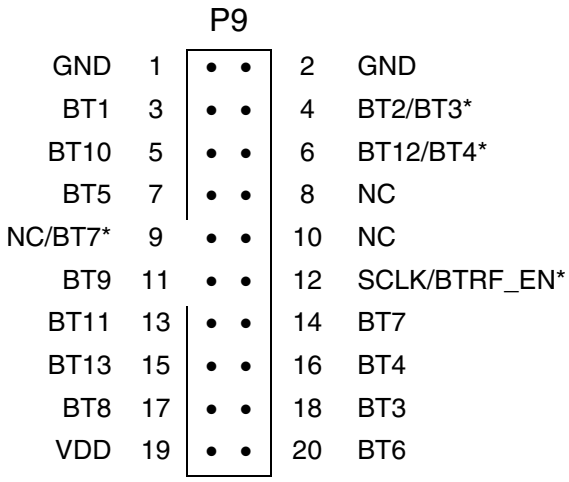

Figure 3-6 BlueTooth Connector P9 Pin Assignments

* Controlled by zero ohm resistors. The inside signal is the one connected when the system is shipped from the factory.

Table 3-6 BlueTooth Connector P9 Signal Descriptions

Pin	Mnemonic	Signal
1, 2	BTRF GND	GROUND for BT RF module
3	BT1	Ref_Clk (24Mhz)
4	BT2	Transmit Data
5	BT10	Inverse BT_RF_OSC_EN/GPO2
6	BT12	SPI data out
7	BT5	Frame synch
8, 10	NC	NO CONNECTION
9,14	BT7	Diversity/BT_RF_OSC_EN
11	BT9	RxTx_en/HOP_SRB
12	SCLK	Should be configured as GPIO, PC14
13	BT11	SPI enable
15	BT13	SPI clock
16	BT4	SPI data in
17	BT8	PWM_RSSI/TXEN
18	BT3	Receive Data
19	BTRF VDD	Power supply for BT RF module
20	BT6	PWM_Tx/GPO1

3.8 MultiTrace Connector

Connector P27 is the MX1ADS MultiTrace connector. Figure3-7 gives the pin assignments and Table 3-7 gives the signal descriptions for this connector.

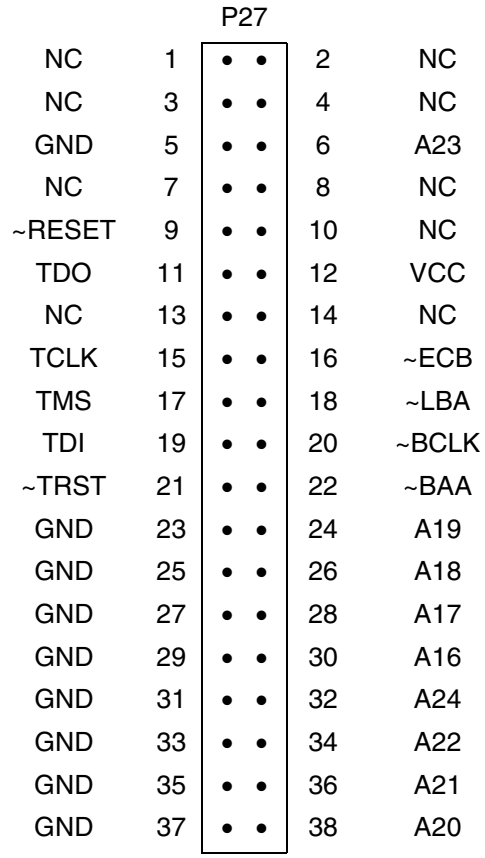

Figure 3-7 MultiTrace Connector P27 Pin Assignments

Table 3-7 MultiTrace Connector P27 Signal Descriptions

Pin	Mnemonic	Signal
1 — 4, 7, 8, 10, 13, 14,	NC	NO CONNECTION
5, 23, 25, 27, 29, 31, 33, 35, 37	GND	GROUND
6, 24, 26, 28, 30, 32, 34, 36, 38	A16 — A24 (not in exact order)	ADDRESS BUS (lines 16—24) — Output lines for addressing external devices.
9	~RESET	RESET — Active-low reset signal.
11	TDO	JTAG TEST DATA OUTPUT — Serial data input from the target
12	VCC	3.3-VOLT POWER
15	TCLK	TEST CLOCK — Output timing signal, for synchronizing test logic and control register access.

Table 3-7 MultiTrace Connector P27 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
16	~ECB	END CURRENT BURST — Active-low input signal asserted by external burst devices; indicates the end of a burst sequence.
17	TMS	TEST MODE SELECT – Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
18	~LBA	LOAD BURST ADDRESS — Active-low signal asserted during burst mode accesses; causes the external burst device to load a new starting burst address.
19	TDI	TEST DATA INPUT — Serial data output line, sampled on the rising edge of the TCK signal.
20	~BCLK	BURST CLOCK — Output signal to external burst devices; synchronizes burst loading and incrementing.
21	~TRST	TARGET RESET — Active-low output signal that resets the target.
22	~BAA	BURST ADDRESS ADVANCE — Active-low signal asserted during burst mode accesses; causes the external burst devices to increment internal burst counters.

3.9 LCD Panel Connector

Connector P8 is the MX1ADS LCD panel connectors. Figure 3-8 gives the pin assignments and Table 3-8 gives the signal descriptions this connector.

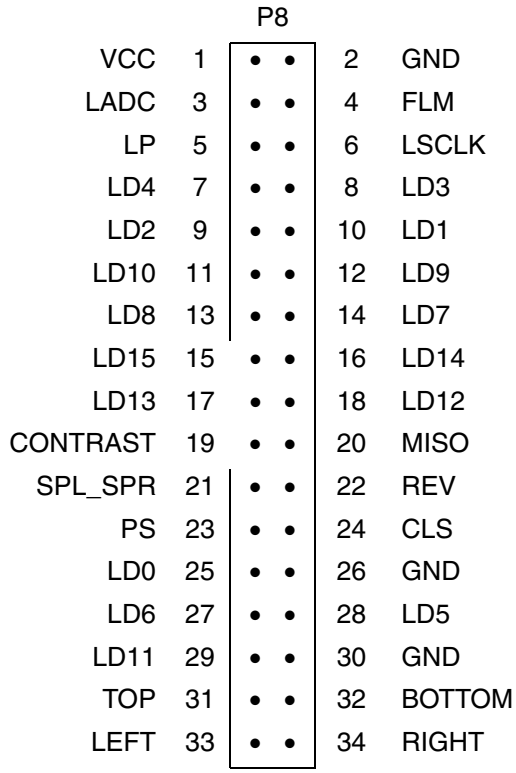

Figure 3-8 LCD Panel Connector P8 Pin Assignments

Table 3-8 LCD Panel Connector P8 Signal Descriptions

Pin	Mnemonic	Signal
1	VCC	Input power (3.0-volts)
2, 26,30	GND	GROUND
3	LADC	ACD/OE Alternate Crystal Direction/Output Enable*
4	FLM	FLM/VSYNC First Line Marker/Vertical Synchronization*
5	LP	LP/HSYNC Line Pulse/Horizontal Synchronization *
6	LSCLK	SCLK Shift Clock
7 — 18, 25, 27 — 29	LD0 — LD15 (not in exact order)	LCD data bus
19	CONTRAST	LCD bias voltage used as contrast control
20	MISO	Configure as GPIO, PC16. Used for an LCD enable
21	SPL_SPR	Horizontal scan direction (Sharp panel dedicated signal)
22	REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal)

Table 3-8 LCD Panel Connector P8 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
23	PS	Control signal output for source driver (Sharp panel dedicated signal)
24	CLS	Start signal output for gate driver. This signal is inverted version of PS (Sharp panel dedicated signal)
31	TOP	Negative pen-Y analog input
32	BOTTOM	Positive pen-Y analog input
33	LEFT	Negative pen-X analog input
34	RIGHT	Positive pen-X analog input

* Passive/Active LCD matrix functions, signal function depends on the LCD type configuration selected.

3.10 SIM Card Connector

Connector P3 is the MX1ADS SIM card connector. Figure 3-9 gives the pin assignments and Table 3-9 gives the signal descriptions for this connector.

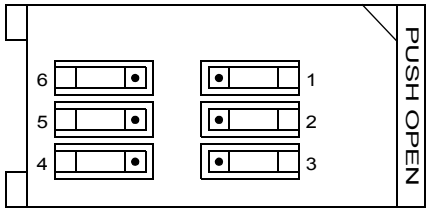

Figure 3-9 SIM Card Connector P3 Pin Assignments

Table 3-9 SIM Card Connector P3 Signal Descriptions

Pin	Mnemonic	Signal
1	SIM_TX/SIM_RX	SIM TRANSMITTED/ SIM RECEIVED DATA - SIM card data, tied together externally through zero ohm resistor.l
2, 4	VCC	VCC (3.0-volts) SIM card power
3	GND	GROUND
5	SIM_RST	SIM RESET - Active low output to SIM card
6	SIM_CLK	SIMCLOCK - output clock to SIM card

3.11 Memory Stick Connector

Connector P5 is the MX1ADS memory stick connector. Figure 3-10 gives the pin assignments and Table 3-10 gives the signal descriptions for this connector.

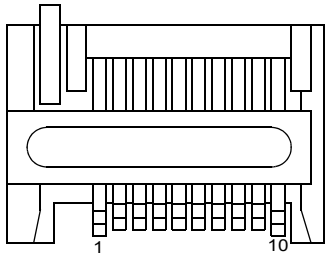

Figure 3-10 Memory Stick Connector P5 Pin Assignments

Table 3-10 Memory Stick Connector P5 Signal Descriptions

Pin	Mnemonic	Signal
1,10	GND	Ground
2	SD_CMD	BS Memory Stick Bus Status (Connected to SD_CMD)
3,9	VCC	VCC (3.0-volts)
4	SD_DAT3	SDIO Memory Stick Serial Data Input/Output (Connected to SD_DAT3)
5,7	NC	NO CONNECTION
6	SD_DAT0	INS Stick Detect (Connected to SD_DAT0)
8	SD_CLK	SCLK Memory Stick Serial Clock (Connected to SD_CLK)

3.12 SD/MMC Connector

Connector P2 is the MX1ADS SD/MMC connector. Figure 3-11 gives the pin assignments and Table 3-11 gives the signal descriptions for this connector.

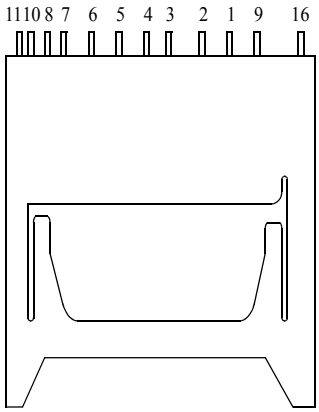

Figure 3-11 SD/MMC Connector P2 Pin Assignments

Table 3-11 SD/MMC Connector P2 Signal Descriptions

Pin	Mnemonic	Signal		
		MMC Card	SD Card	
			1-Bit Mode	4-Bit Mode
1	SD_DAT3	Reserved	Not Used	Data Line DAT3
2	SD_CMD	Command / Response		
3	GND	Ground		
4	VCC	Supply Voltage (3.0-volts)		
5	SD_CLK	Clock		
6	GND	Ground		
7	SD_DAT0	Data Line DAT0		
8	SD_DAT1	Not Used	Interrupt (IRQ)	Data Line DAT1 or Interrupt (IRQ)
9	SD_DAT2	Not Used	ReadWait (RW)	Data Line DAT2 or Read Wait (RW)
10	SIM_RX	Card Detect, configured as GPIO, PB17		
11	GND	Ground		
16	SD_WP	Write Protect Detect, connects to I/O Expander, U42-13 (P10)		

3.13 Expansion Connector

Connector P19 is the Expansion connector. All the signals of MC9328MX1 are connected to this 16x3-pin connector except data bus, address bus, EIM control signals and SDRAM control signals. Figure 3-12 gives the pin assignment and Table 3-12. gives the signal descriptions for this connector.

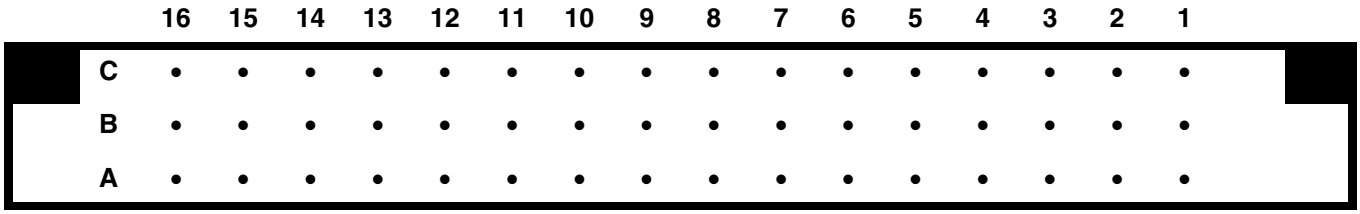

Figure 3-12 Connectors P19 and P20 Pin Assignments

Table 3-12. Expansion Connector P19 Signal Description

Pin	Mnemonic	Signal
A1,B1,C1	GND	GROUND
A2	PWMO	PULSE WIDTH MODULATED OUTPUT - Output of the PWM module
A3	MOSI	MASTER OUT / SLAVE IN - SPI data signal (bidirectional)
A4	SCLK	SERIAL CLOCK
A5	UART1_TXD	UART1 TRANSMITTED DATA - Serial output signal.
A6	SSI_TXCLK	SYCHRONOUS SERIAL INTERFACE TRANSMITTER CLOCK - Bidirectional
A7	SSI_RXDAT	SYCHRONOUS SERIAL INTERFACE RECEIVED DATA - Serial input signal
A8	UART2_RXD	UART2 RECEIVED DATA - Serial output signal
A9	UART2_CTS	UART2 CLEAR TO SEND - Active low output signal
A10	USBD_VM	USB VOLTAGE MINUS INPUT
A11	USBD_RCV	USB RECEIVED DATA INPUT
A12	SIM_CLK	SIMCLOCK - Output clock to SIM card
A13,C12	SIM_TX,SIM_RX	SIM TRANSMITTED/ SIM RECEIVED DATA - SIM card data, tied together externally through zero ohm resistor.
A14	SD_CMD	SD/MMC COMMAND - Serial command bit to SD/MMC card, bidirectional

Table 3-12. Expansion Connector P19 Signal Description

A15	SD_DAT2	SD/MMC DATA BIT 2 - Serial data bit to SD/MMC card, bidirectional
A16,B16,C16	VCC	VCC (3.0-volts)
B2	TIN	TIMER INPUT CAPTURE - Timer input
B3	MISO	MASTER IN / SLAVE OUT - SPI data signal (bidirectional
B4	SPI_RDY	SPI READY - CSPI serial burst trigger, active low input
B5	UART1_RTS	UART1 REQUEST TO SEND - Active low input signal
B6	SSI_TXFS	SYCHRONOUS SERIAL INTERFACE TRANSMITTER FRAME SYNC
B7	SSI_RXCLK	SYCHRONOUS SERIAL INTERFACE RECEIVER CLOCK - Bidirectional
B8	UART2_TXD	UART2 TRANSMITTED DATA - Serial output signal
B9	USBD_VMO	USB VOLTAGE MINUS OUPUT
B10	USBD_VP	USB VOLTAGE POSITIVE INPUT
B11	USBD_ROE	USB DATA RECEIVED OUTPUT ENABLE - Active low output
B12	SIM_RST	SIM RESET - Active low output to SIM card
B13	SIM_PD	SIM PRESENCE DETECT - Active low input
B14	SD_CLK	SD/MMC CLOCK - Clock output to SD/MMC card
B15	SD_DAT1	SD/MMC DATA BIT 1 - Serial data bit to SD/MMC card, bidirectional
C2	TOUT12	TIMER OUTPUT COMPARE
C3	SS	SLAVE SELECT - Bidirectional, active low, slave mode input, master mode output.
C4	UART1_RXD	UART1 RECEIVED DATA - Serial output signal
C5	UART1_CTS	UART1 CLEAR TO SEND - Active low output signal
C6	SSI_TXDAT	SYCHRONOUS SERIAL INTERFACE TRANSMITTED DATA - Serial output signal
C7	SSI_RXFS	SYCHRONOUS SERIAL INTERFACE RECEIVER FRAME SYNC - Bidirectional
C8	UART2_RTS	UART2 REQUEST TO SEND - Active low input signal
C9	USBD_VPO	USB VOLTAGE POSITIVE OUTPUT
C10	USBD_SUSPND	USB SUSPEND OUTPUT
C11	USBD_AFE	USB ANALOG FRONT END ENABLE
C13	SIM_SVEN	SIM VCC ENABLE - Enable power to the SIM card, active low

Table 3-12. Expansion Connector P19 Signal Description

C14	SD_DAT3	SD/MMC DATA BIT 3 - Serial data bit to SD/MMC card, bidirectional
C15	SD_DAT0	SD/MMC DATA BIT 0 - Serial data bit to SD/MMC card, bidirectional

3.14 Image Sensor Connector

P20 is a 16x3-pin connector. P20 is assigned with signals for an Image Sensor daughter card. Several different image sensor can plugged to this connectors. Figure 3-12 gives the pin assignment of this connector and Table 3-13. gives the signal descriptions for this connector.

Table 3-13. Image Sensor Connector P20 Signal Description

Pin	Mnemonic	Signal
A1,B1,C1	GND	GROUND
A2	CSI_D0	CMOS SENSOR INTERFACE DATA 0 - Data input from Image Sensor
A3	CSI_D2	CMOS SENSOR INTERFACE DATA 2- Data input from Image Sensor
A4	CSI_D4	CMOS SENSOR INTERFACE DATA 4- Data input from Image Sensor
A5	CSI_D6	CMOS SENSOR INTERFACE DATA 6- Data input from Image Sensor
A6	CSI_PIXCLK	CMOS SENSOR INTERFACE PIXAL CLOCK - Data latch strobe
A7	CSI_VSYNC	CMOS SENSOR INTERFACE VERTICAL SYNC - Control input
A8	I2C_CLK	I SQUARED C CLOCK - Serial clock, bidirectional
A9	MOSI/PC17	MASTER OUT / SLAVE IN or PORT C BIT 17 - Not used by CSI daughter card
A10	~CS4/PA22	CHIP SELECT 4 / PORT A BIT 23 - Not used by CSI daughter card
A11-A15	NC	NO CONNECTION
A16,B16,C16	VCC	VCC (3.0-volts)
B2-B15	NC	NO CONNECTION
C2	CSI_D1	CMOS SENSOR INTERFACE DATA 1- Data input from Image Sensor
C3	CSI_D3	CMOS SENSOR INTERFACE DATA 3- Data input from Image Sensor
C4	CSI_D5	CMOS SENSOR INTERFACE DATA 5 - Data input from Image Sensor
C5	CSI_D7	CMOS SENSOR INTERFACE DATA 7 - Data input from Image Sensor
C6	CSI_HSYNC	CMOS SENSOR INTERFACE HORIZONTAL SYNC- Active low input

Table 3-13. Image Sensor Connector P20 Signal Description

C7	CSI_MCLK	CMOS SENSOR INTERFACE MASTER CLOCK - Clock output to sensor card
C8	I2C_DAT	I SQUARED C DATA - Serial data, bidirectional
C9	TIN/PA1	TIMER INPUT CAPTURE/ PORT A BIT 1 - - Not used by CSI daughter card
C10	~CS5/PA23	CHIP SELECT 5 / PORT A BIT 23 - Configured for GPIO to act as a SYNC signal
C11	SIM_RST	SIM RESET - Configured as GPIO for Image sensor's Unit signal.
C12	SIM_CLK	SIM CLOCK -
C13-C15	NC	NO CONNECTION

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