56F826

Evaluation Module User Manual

56F800
16-bit Digital Signal Controllers

DSP56F826EVMUM
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semiconductor

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Preface

This reference manual describes in detail the hardware on the 56F826 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F826 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction -** provides an overview of the 56F826EVM and its features.
- **Chapter 2, Technical Summary -** describes the 56F826EVM hardware in detail.
- **Appendix A, 56F826EVM Schematics -** contains the schematics of the 56F826EVM.
- **Appendix B, 56F826EVM Bill of Material -** provides a list of the materials used on the 56F826EVM board.

Suggested Reading

More documentation on the 56F826 and the 56F826EVM kit may be found at URL:

http://www.freescale.com

Notation Conventions

This manual uses the following notational conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{\text{WE}}$ $\overline{\text{OE}}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a “$” symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter “b” attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Blue Text	Linkable on-line	...refer to **Figure 1-1**	
Bold	Reference sources, paths, emphasis	...see: **http://www.freescale.com/...**	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference:

codec	COder/DECoder, a part used to convert analog signals to digital (Coder) and digital signals to analog (Decoder)
EEPROM	Electrically Erasable Programmable Read-Only Memory
EVM	Evaluation Module, a hardware platform which allows a customer to evaluate the silicon and develop their application
GPIO	General Purpose Input and Output Port; does not share pin functionality with any other peripheral on the chip and can only be set as an input, output or level-sensitive interrupt input
IC	Integrated Circuit
JTAG	Joint Test Action Group, a bus protocol/interface used for test and debug
LQFP	Low-profile Quad Flat Pack
MPIO	Multi-Purpose Input and Output Port; shares package pins with other peripherals on the chip and can function as a GPIO
OnCE™	On-Chip Emulation, a debug bus and port created by Freescale to enable designers to create a low-cost hardware interface for a professional-quality debug environment
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RAM	Random Access Memory
ROM	Read-Only Memory
SCI	Serial Communications Interface Port
SPI	Serial Peripheral Interface Port
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface Port
WS	Wait State

References

The following sources were used to produce this manual:

[1] *DSP56800 Family Manual*, , DSP56800FM, Freescale Semiconductor

[2] *56F826/827 User's Manual*, DSP56F826-827UM, Freescale Semiconductor

[3] *56F826 Technical Data*, DSP56F826, Freescale Semiconductor

Chapter 1
Introduction

The 56F826EVM is used to demonstrate the abilities of the 56F826 and to provide a hardware tool allowing the development of applications that use the 56F826.

The 56F826EVM is an evaluation module board that includes a 56F826 part, 16-bit stereo codec, external memory and a daughter card expansion interface. The daughter card expansion connectors are for signal monitoring and user feature expandability.

The 56F826EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the 56F826EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full-speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, allowing the user to reassign any and all of the hybrid controller's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the chip are available to the user.

1.1 56F826EVM Architecture

The 56F826EVM facilitates the evaluation of various features present in the 56F826 part. The 56F826EVM can be used to develop real-time software and hardware products based on the 56F826. The 56F826EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The 56F826EVM is flexible enough to allow a user to fully exploit the 56F826's features to optimize the performance of his product, as shown in **Figure 1-1**.

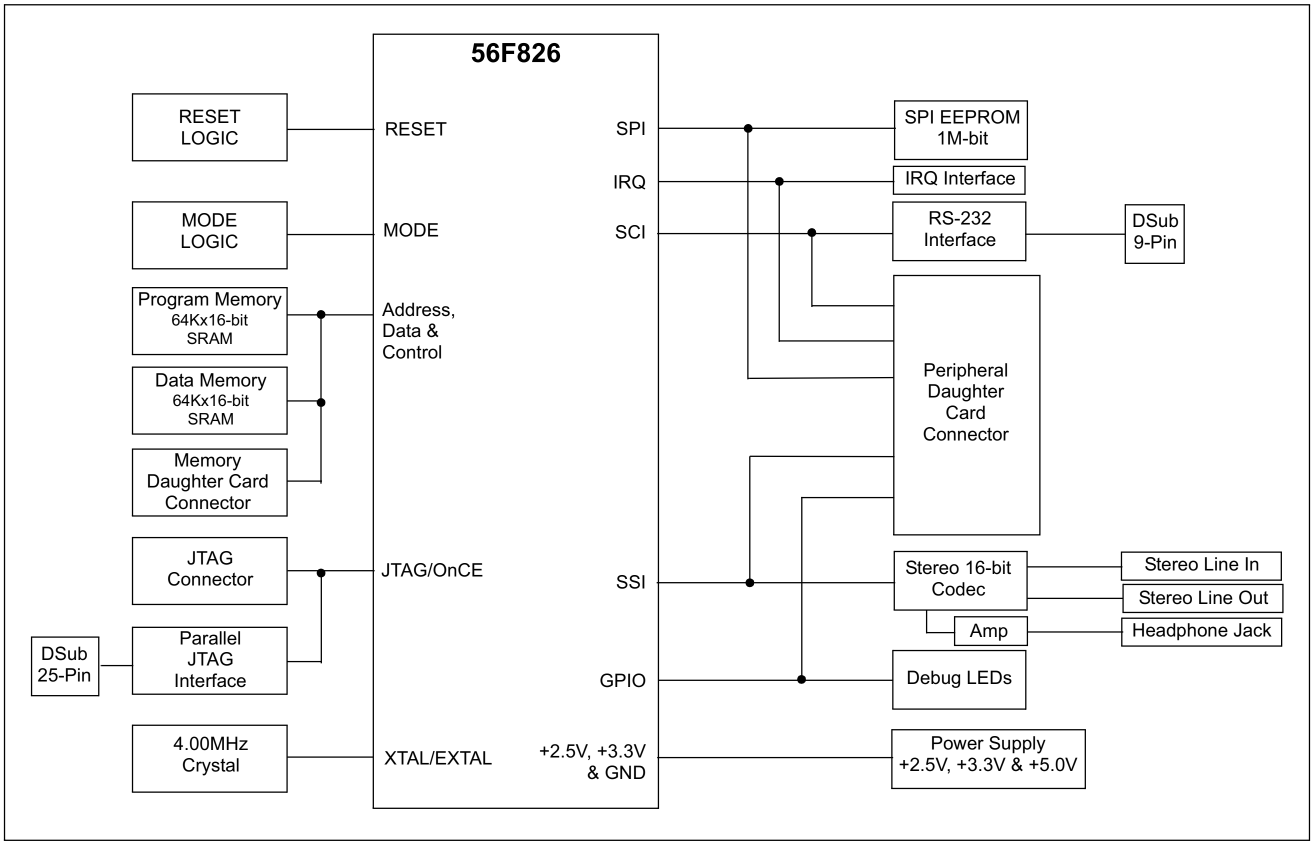

56F826
RESET LOGIC
MODE LOGIC
Program Memory 64Kx16-bit SRAM
Data Memory 64Kx16-bit SRAM
Memory Daughter Card Connector
JTAG Connector
DSub 25-Pin
Parallel JTAG Interface
4.00MHz Crystal
RESET
MODE
Address, Data & Control
JTAG/OnCE
XTAL/EXTAL
SPI
IRQ
SCI
SSI
GPIO
+2.5V, +3.3V & GND
SPI EEPROM 1M-bit
IRQ Interface
RS-232 Interface
DSub 9-Pin
Peripheral Daughter Card Connector
Stereo 16-bit Codec
Amp
Stereo Line In
Stereo Line Out
Headphone Jack
Debug LEDs
Power Supply +2.5V, +3.3V & +5.0V

Figure 1-1. Block Diagram of the 56F826EVM

1.2 56F826EVM Configuration Jumpers

Seven jumper groups, (JG1-JG7), shown in **Figure 1-2**, are used to configure various features on the 56F826EVM board. **Table 1-1** describes the default jumper group settings.

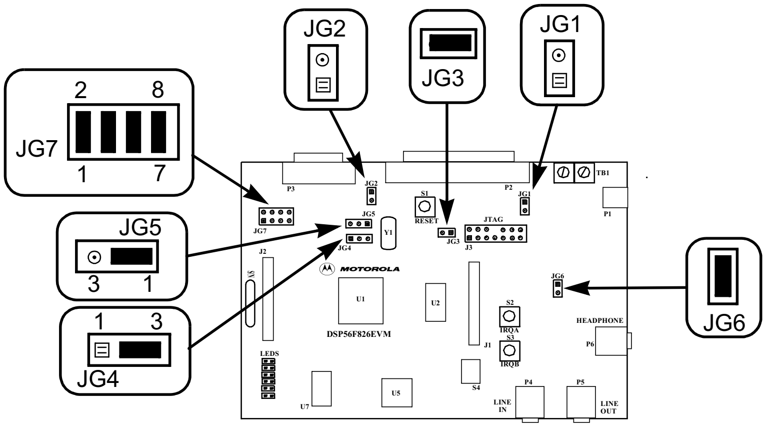

JG2
JG3
JG1
2
8
JG7
1
7
JG5
3
1
1
3
JG4
JG6
P3
JG2
P2
JG1
TB1
P1
S1
RESET
JG7
JG5
JG4
Y1
JG3
JTAG
J3
J2
MOTOROLA
U1
U2
JG6
S2
IRQA
S3
IRQB
HEADPHONE
P6
DSP56F826EVM
J1
LEDS
U7
U5
S4
P4
P5
LINE IN
LINE OUT

Figure 1-2. 56F826EVM Jumper Reference

Table 1-1. 56F826EVM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	Enable on-board Parallel JTAG Host/Target Interface	NC
JG2	Enable RS-232 output	NC
JG3	Enable on-board SRAM	1–2
JG4	Use on-board EXTAL crystal input for oscillator	2–3
JG5	Use on-board XTAL crystal input for oscillator	1–2
JG6	Selects device’s Mode 0 operation upon exit from reset	1-2
JG7	Enable SPI EEPROM	1–2, 3–4, 5–6 & 7–8

1.3 56F826EVM Connections

An interconnection diagram is shown in Figure 1-3 for connecting the PC and the external +12.0V DC power supply or external +5.0V DC lab power supply to the 56F826EVM board.

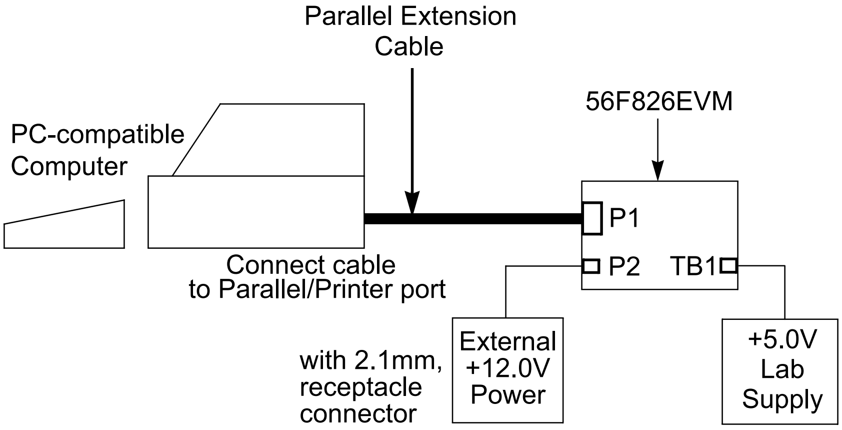

Parallel Extension Cable
56F826EVM
PC-compatible Computer
P1
P2
TB1
Connect cable to Parallel/Printer port
with 2.1mm, receptacle connector
External +12.0V Power
+5.0V Lab Supply

Figure 1-3. Connecting the 56F826EVM Cables

Perform the following steps to connect the 56F826EVM cables:

1. Connect the parallel extension cable to the parallel port of the host computer
2. Connect the other end of the parallel extension cable to P1 on the 56F826EVM board as shown in **Figure 1-3**. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12.0V DC, 2.1A switching power supply or the external +5.0V DC, 1A lab power supply is not plugged into a +120V AC power source
4. Connect the 2.1mm output power plug from the external switching power supply into P2 on the 56F826EVM board, as shown in **Figure 1-3**. Optionally, attach an external +5.0V DC lab power supply via the 2-pin terminal block, TB1.
5. Apply power to the external power supply. The green Power-On LED, LED7, will illuminate when power is applied correctly.

Chapter 2
Technical Summary

The 56F826EVM is designed as a versatile controller development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F826 device, combined with the on-board 64K × 16-bit external program static RAM (SRAM), 64K × 16-bit external data SRAM, RS-232 interface, stereo 16-bit codec interface, Daughter Card Expansion interface and parallel JTAG interface, makes the 56F826EVM ideal for developing and implementing many audio and voice algorithms, as well as for learning the architecture and instruction set of the 56F826 processor.

The main features of the 56F826EVM, with board and schematic reference designators, include:

- 56F826EVM 16-bit +2.5V/+3.3V controller operating at 80MHz [U1]
- External fast static RAM (FSRAM) memory [U2], configured as:
    - 64K×16 bits of Program memory with 0 wait states at 70MHz
    - 64K×16 bits of Data memory with 0 wait states at 70MHz
- 1Mbit Serial EEPROM [U4]
- 4.00MHz crystal oscillator for device frequency generation [Y1]
- Optional external oscillator frequency input connector [JG4 and JG5]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J3]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P2]
- RS-232 interface for easy connection to a host processor [U3 and P3]
- 16-bit stereo codec interface [U5, P4 and P5]
- Stereo headphone interface [U6 and P6]

- Codec sample rate selector [S4]
- Peripheral Daughter Card Expansion Connector, to allow the user to connect his own SCI, SSI, SPI or GPIO-compatible peripheral to the controller[J2]
- Memory Daughter Card Expansion Connector, to allow the user to connect his own memory or memory device to the controller[J1]
- On-board power regulation from an external +12V DC-supplied power input [P1]
- On-board power regulation from an optional +5V DC-supplied power input [TB1]
- Light Emitting Diode (LED) power indicator [LED7]
- Six on-board real-time user debugging LEDs [LED1-6]
- Manual RESET push-button [S1]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push-button for $\overline{\text{IRQB}}$ [S3]

2.1 56F826

The 56F826EVM uses a Freescale DSP56F826BU80 part, designated as U1 on the board and in the schematics. This part will operate at a maximum speed of 80MHz. A full description of the 56F826, including functionality and user information, is provided in these documents:

- *56F826 Preliminary Technical Data Sheet*, (DSP56F826-827 UM)**:** Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements and available packaging.
- *56F826/827 16-Bit Digital Signal Processor User's Manual*, (56F826UM): Provides an overview description of the and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control/status register descriptions for each subsystem.
- *DSP56F800Family Manual*, (DSP56F800FM): Provides a detailed description of the core processor, including internal status and control registers and a detailed description of the family instruction set.

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

http://www.freescale.com

2.2 Program and Data Memory

The 56F826EVM uses one bank of 128K×16-bit Fast Static RAM (GSI GS72116, labeled U2) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-1**. This physical memory bank is split into two logical memory banks of 64Kx16-bits: one for Program memory and the other for Data memory. By using the controller's program strobe, $\overline{\text{PS}}$, signal line along with the memory chip's A0 signal line, half of the memory chip is selected when program memory accesses are requested and the other half of the memory chip is selected when data memory access are requested. This memory bank will operate with zero wait state accesses while the 56F826 is running at 70MHz. However, when running at 80MHz, the memory bank operates with four wait state accesses. This memory bank can be disabled by removing the jumper at JG3.

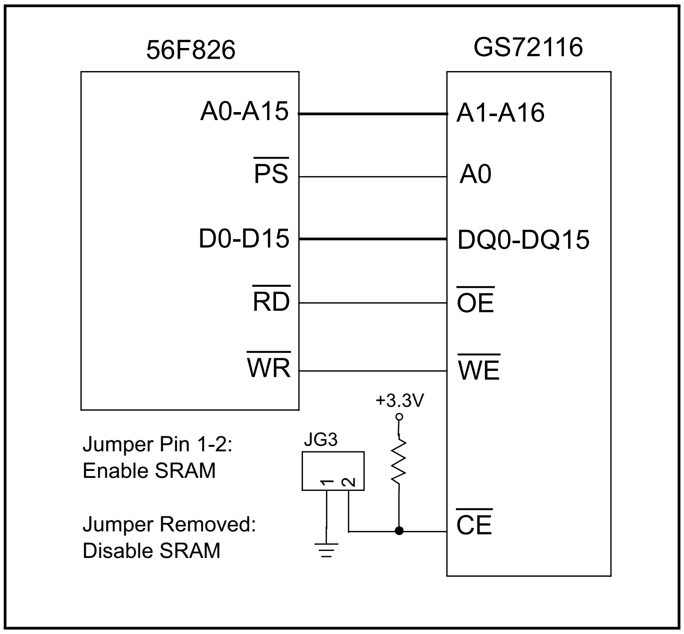

56F826
GS72116
A0-A15
A1-A16
PS
A0
D0-D15
DQ0-DQ15
RD
OE
WR
WE
+3.3V
JG3
1
2
CE
Jumper Pin 1-2:
Enable SRAM
Jumper Removed:
Disable SRAM

Figure 2-1. Schematic Diagram of the External Memory Interface

2.3 SPI EEPROM Memory

A 1Mbit, +3.3V, SPI, serial EEPROM Memory, Atmel AT45DB011-SC, is provided on the 56F826EVM; reference **Figure 2-2**. This memory connects directly to the SPI Port through a header on the 56F826. It can be used to load program code and data into the 56F826's internal or external memory spaces. A jumper block, JG7, is provided, which allows the user to disconnect the on-board SPI EEPROM from the SPI port and to connect his own SPI port peripheral. The header details are shown in **Table 2-1**.

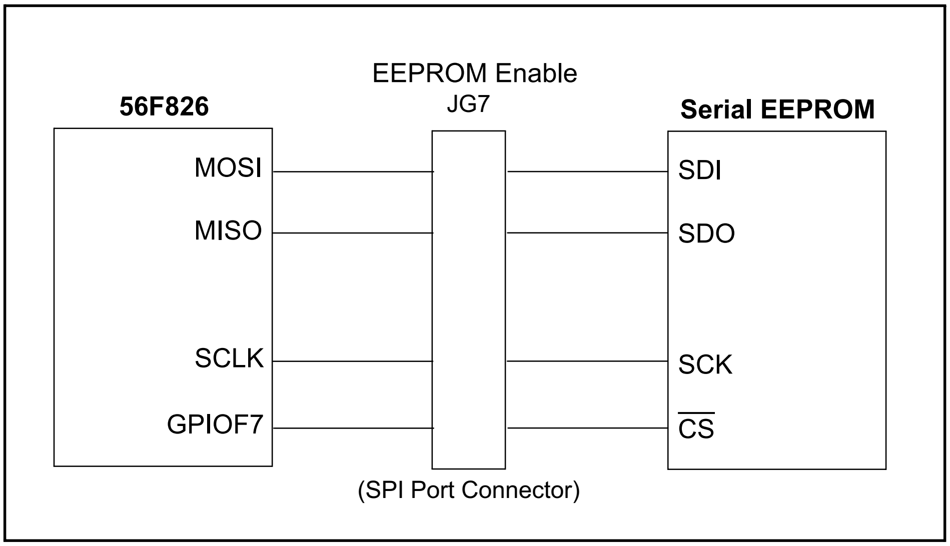

EEPROM Enable
JG7
56F826
Serial EEPROM
MOSI
MISO
SCLK
GPIOF7
SDI
SDO
SCK
$\overline{CS}$
(SPI Port Connector)

Figure 2-2. SPI EEPROM Memory Block Diagram

Table 2-1. SPI Port Connector Description

JG7			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{SS}$/GPIO7	2	$\overline{CS}$
3	MISO	4	SDO
5	MOSI	6	SDI
7	SCLK	8	SCK

2.4 RS-232 Serial Communications

The 56F826EVM provides an RS-232 interface by the use of an RS-232 level converter, (Maxim MAX3245EEAI, designated as U3). Refer to the RS-232 schematic diagram in **Figure 2-3**. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232 compatible signal levels and connects to the host's serial port via connector P3. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The pinout of connector P3 is listed in **Table 2-2**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG2.

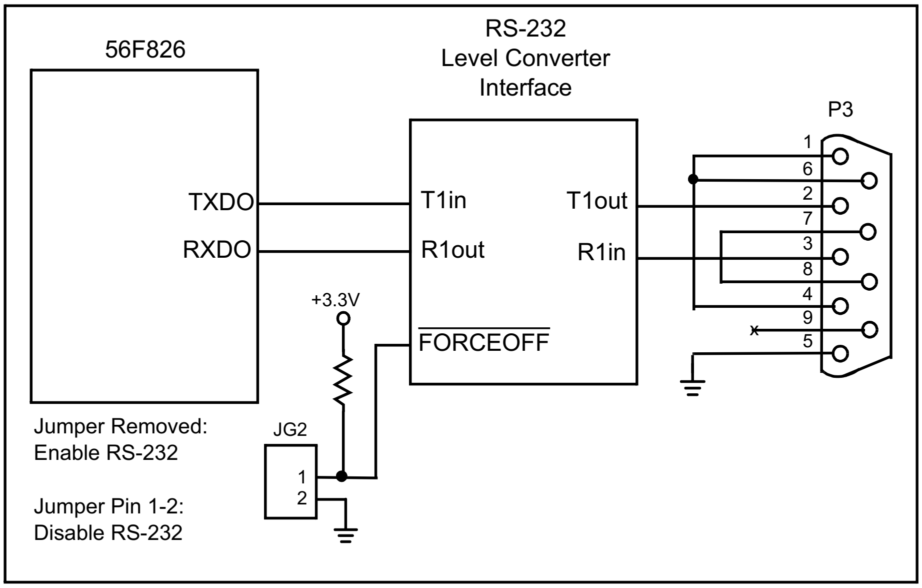

56F826
RS-232
Level Converter
Interface
P3
TXDO
RXDO
T1in
R1out
T1out
R1in
+3.3V
FORCEOFF
1
6
2
7
3
8
4
9
5
Jumper Removed:
Enable RS-232
Jumper Pin 1-2:
Disable RS-232
JG2
1
2

Figure 2-3. Schematic Diagram of the RS-232 Interface

Table 2-2. RS-232 Serial Connector Description

P3			
Pin #	**Signal**	**Pin #**	**Signal**
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD	7	Jumper to 8
3	RXD	8	Jumper to 7
4	Jumper to 1 & 6	9	N/C
5	GND		

2.5 Clock Source

The 56F826EVM uses a 4.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. To achieve its 80MHz maximum operating frequency, the 56F826 uses its internal PLL to multiply the input frequency by 20. An external oscillator source can be connected to the controller by using the oscillator bypass connectors, JG4 and JG5; see **Figure 2-4**. If the input frequency is above 4MHz, then the EXTAL input should be jumpered to ground by adding a jumper between JG4 pins 2 and 3. The input frequency would then be injected on JG5's pin 2. If the controller needs to be synchronized to the codec's sample frequency, then the controller's input frequency should be jumpered using the 12.2280MHz codec frequency. If the input frequency is below 4MHz, then the input frequency can be injected on JG4's pin 2.

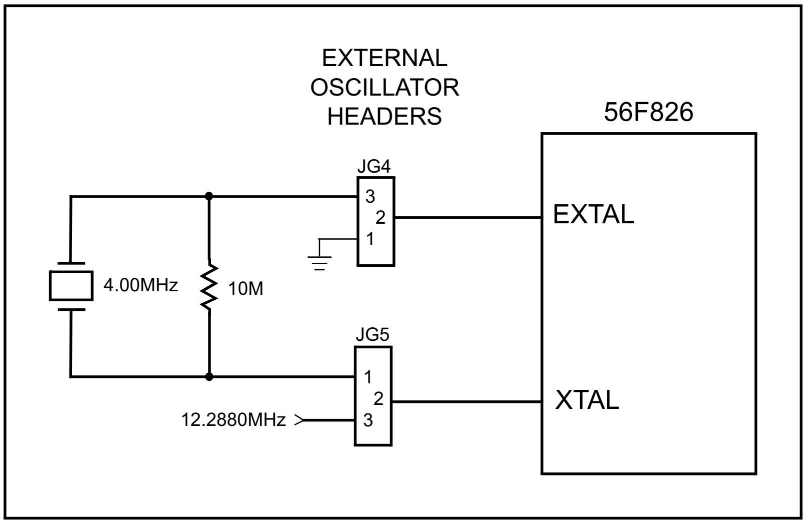


Figure 2-4. Schematic Diagram of the Clock Interface

2.6 Operating Mode

The 56F826EVM provides a boot-up MODE selection jumper, JG6. This jumper is used to select the operating mode of the controller as it exits RESET. Refer to the DSP56F826 User's Manual for a complete description of the chip's operating modes. **Table 2-3** shows the two operating modes available on the 56F826.

Table 2-3. Operating Mode Selection

Operating Mode	JG6	Comment
0	1–2	Bootstrap from internal memory
3	No Jumper	Bootstrap from external memory

2.7 Debug LEDs

Six on-board Light-Emitting Diodes (LEDs) are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-5**. User LED1 is controlled by Port B's PB0 signal. User LED2 is controlled by PB1. User LED3 is controlled by PB2. User LED4 is controlled by PB3. User LED5 is controlled by PB4. User LED6 is controlled by PB5. Setting PB0, PB1, PB2, PB3, PB4 or PB5 to a Logic One value will turn on the associated LED.

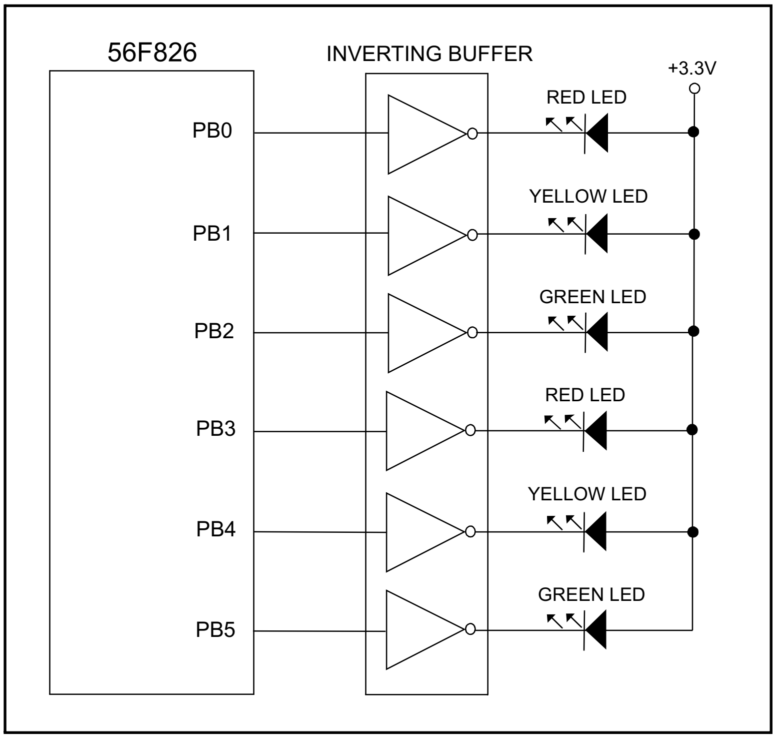


Figure 2-5. Schematic Diagram of the Debug LED Interface

2.8 Debug Support

The 56F826EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.8.1 JTAG Connector

The JTAG connector on the 56F826EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F826's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. **Table 2-4** shows the pin-out for this connector.

Table 2-4. JTAG Connector Description

J3			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	NC	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG1. Reference **Table 2-5** for this jumper's selection options.

Table 2-5. Parallel JTAG Interface Disable Jumper Selection

JG1	Comment
No jumpers	On-board Parallel JTAG Interface Enabled
1–2	Disable on-board Parallel JTAG Interface

2.8.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P2, allows the 56F826 to communicate with a Parallel Printer Port on a Windows PC; reference **Figure 2-6**. By using this connector, the user can download programs and work with the 56F826's registers. **Table 2-6** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG1 should be removed, as shown in **Table 2-5**.

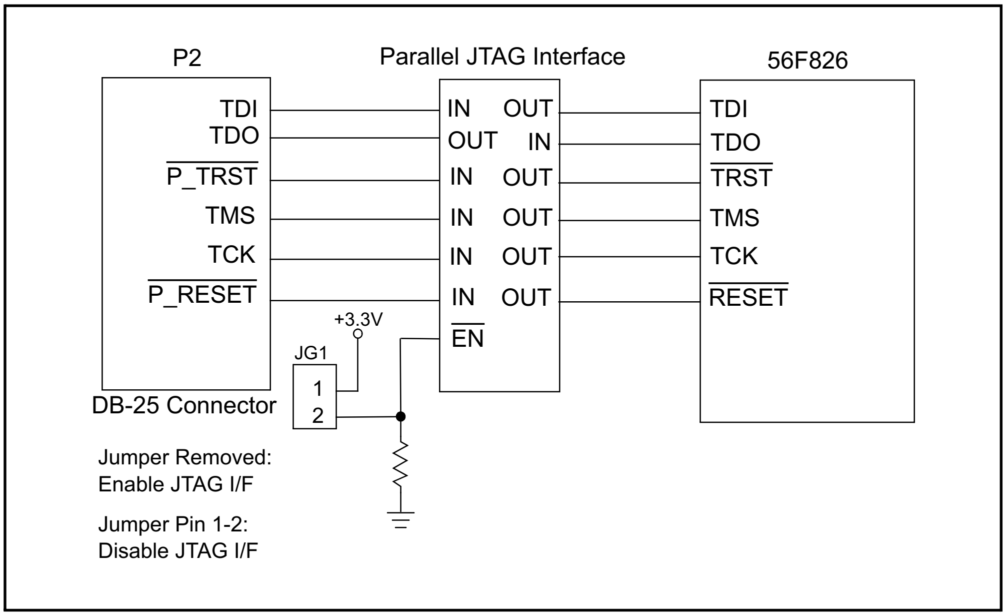

P2
Parallel JTAG Interface
56F826
TDI
TDO
P_TRST
TMS
TCK
P_RESET
DB-25 Connector
IN OUT
OUT IN
IN OUT
IN OUT
IN OUT
IN OUT
EN
+3.3V
JG1
1
2
TDI
TDO
TRST
TMS
TCK
RESET
Jumper Removed:
Enable JTAG I/F
Jumper Pin 1-2:
Disable JTAG I/F

Figure 2-6. Block Diagram of the Parallel JTAG Interface

Table 2-6. Parallel JTAG Interface Connector Description

P2			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	NC
4	PORT_TCK	17	NC
5	PORT_TDI	18	GND
6	$\overline{\text{PORT\_TRST}}$	19	GND

Table 2-6. Parallel JTAG Interface Connector Description (Continued)

P2			
Pin #	**Signal**	**Pin #**	**Signal**
7	NC	20	GND
8	PORT_IDENT	21	GND
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

2.9 External Interrupts

Two on-board push-button switches are provided for external interrupt generation, as shown in Figure 2-7. SW2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. SW3 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

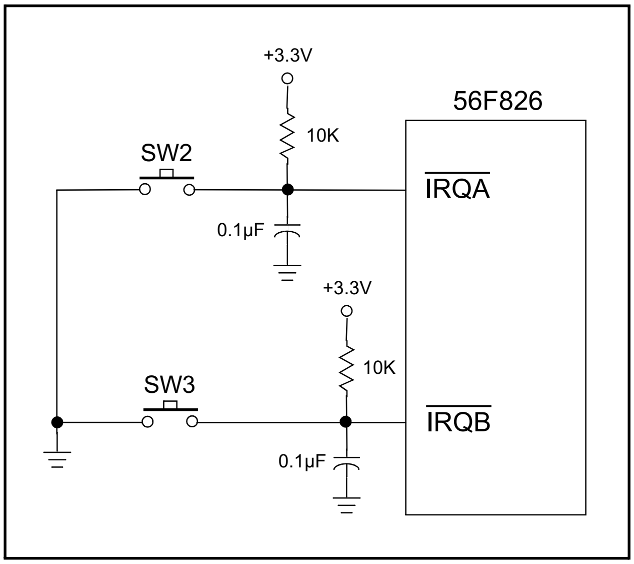


Figure 2-7. Schematic Diagram of the User Interrupt Interface

2.10 Reset

Logic is provided on the 56F826 to generate an internal Power-On RESET. Additional reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button; refer to **Figure 2-8**.

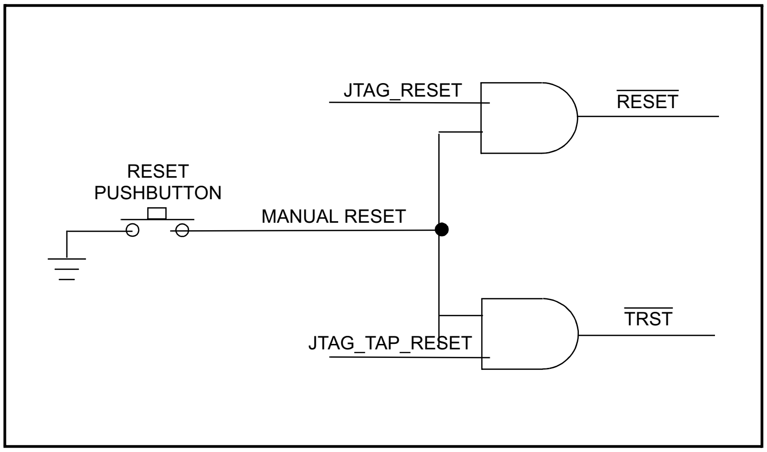

JTAG_RESET
$\overline{\text{RESET}}$
RESET PUSHBUTTON
MANUAL RESET
$\overline{\text{TRST}}$
JTAG_TAP_RESET

Figure 2-8. Schematic Diagram of the RESET Interface

2.11 Power Supply

The main power input, +12.0V DC, to the 56F826EVM is through a 2.1mm coax power jack. An optional +5.0V DC power supply input is available through a 2-pin terminal block, TB1. A 1.2A power supply is provided with the 56F826EVM; however, less than 500mA is required by the EVM. The remaining current is available for the user's custom daughter card application, when connected to the daughter card interface. The power regulation on the 56F826EVM provides +5.0V DC voltage regulation for the codec's analog circuits and to the additonal voltage regulation logic on the EVM. The additional voltage regulation logic provides +2.5V DC voltage regulation for the controller's core and +3.3V DC voltage regulation for the controller's I/O, memory, parallel JTAG interface and supporting logic; refer to **Figure 2-9**. Power applied to the 56F826EVM is indicated with a Power-On LED, referenced as LED7.

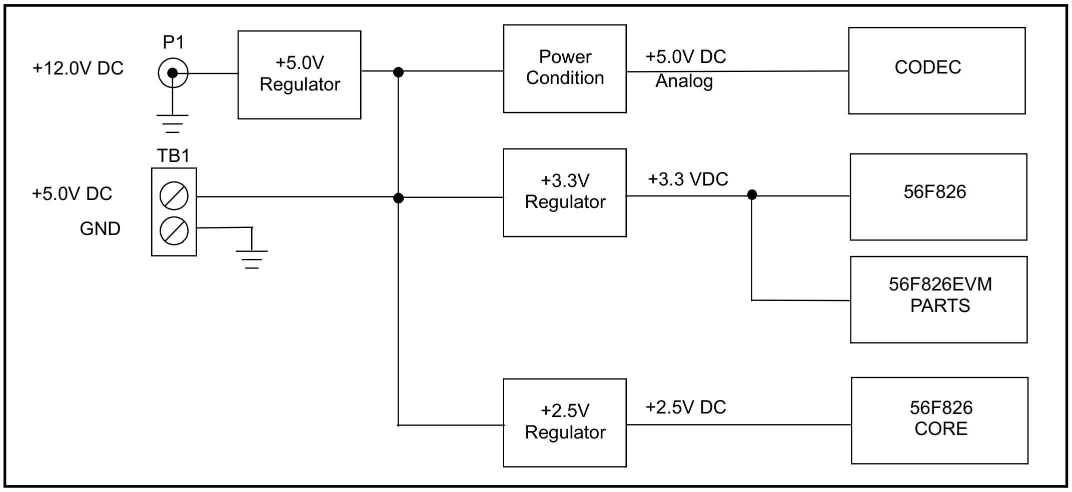

+12.0V DC
P1
+5.0V Regulator
Power Condition
+5.0V DC Analog
CODEC
TB1
+5.0V DC
GND
+3.3V Regulator
+3.3 VDC
56F826
56F826EVM PARTS
+2.5V Regulator
+2.5V DC
56F826 CORE

Figure 2-9. Schematic Diagram of the Power Supply

2.12 Stereo Codec

A 16-bit audio quality stereo codec, Crystal Semiconductor CS4218, is connected to the 56F826's SSI port to support audio, voice and signal analysis applications. The codec is clocked with a 12.288MHz oscillator, allowing the codec to operate between a sample frequency of 8kHz and 48kHz. The sample rate can be manually set using the appropriate switch positions on dip switch S4. This three position dip switch makes the sample rate selections detailed in **Table 2-7** possible. The codec supports +3.3V digital levels, eliminating the need for voltage level translation circuitry. Additionally, a set of zero ohm resistors are provided on the EVM to allow a user to disconnect the on-board codec from the SSI port and to connect his own codec to the SSI port; see **Figure 2-11**. The on-board codec has analog signal-conditioning logic, allowing direct connection to its line level input and line level output signals through two 1/8" stereo jacks; reference **Figure 2-10**.

Table 2-7. Codec Sample Rate Selector

SW 4 Position 3 (MF6)	**SW 4 Position 2** (MF7)	**SW 4 Position 3** (MF8)	**Sample Rate**
ON	ON	ON	48.00kHz
ON	ON	OFF	32.00kHz
ON	OFF	ON	24.00kHz
ON	OFF	OFF	19.20kHz
OFF	ON	ON	16.00kHz
OFF	ON	OFF	12.00kHz
OFF	OFF	ON	9.60kHz
OFF	OFF	OFF	8.00kHz

2.12.1 Analog Input/Output

The 56F826EVM uses jacks for line level stereo input, line level stereo output and stereo headphone output. A National Semiconductor LM4880 provides the drive required for the use of headphones. This device offers a THD, which is superior to the CS4218's on-chip headphone drive circuitry by a factor of two. The basic analog codec connections are shown in **Figure 2-10**.

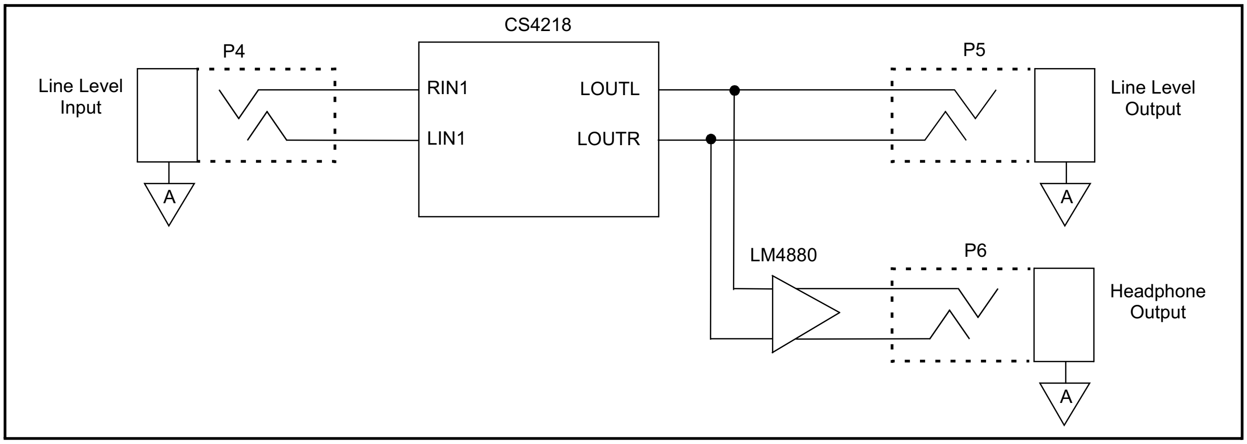


Figure 2-10. Codec Analog Connections

2.12.2 Digital Interface

The serial interface of the codec transfers digital audio data and control data into and out of the device. The SSI port, which consists of independent transmitter and receiver sections, is used for serial communication with the codec.

On the controller side, the Serial Transmit Data, STD, pin is an output when data is being transmitted to the codec. The Serial Receive Data, SRD, pin is an input when data is being received from the codec. These two pins are connected to the codec Serial Data Input, SDIN, and Serial Data Output, SDOUT, pins.

The controller's Transmit Serial Clock, STCK, pin provides the serial bit rate clock for the SSI interface. It is connected to the codec Serial Port Clock, SCLK, pin. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK.

The controller's GPIO PORT D Bit 0 pin, PD0, is programmed to control the codec's Active Low Reset, RESET, signal.

The Serial Transmit Frame Sync pin, STFS, is programmed to control the codec's Frame Sync, FSYNC, signal. FSYNC is sampled by SCLK, with a rising edge indicating that a new frame is about to start. The FSYNC frequency is always the system’s sample rate. It may be an input to the codec, or it may be an output from the codec in data mode.

The basic codec digital connections are shown in **Figure 2-11**.

The codec’s MODE is set by the three MODE selection resistors, R96-R98. In the factory default setting of MODE 4, the codec is set to be the Master of the SPI bus with its data word set at 32 bits per frame; i.e., 16 bits, Left channel and 16 bits, Right channel. The sample rate is selected on Sample Rate Selector switch S4; reference **Table 2-7** for selection options. Codec control information is sent over a separate serial port using: PD1 as the Control Chip Select, CCS, signal; PD2 as the Control Data Input, CDIN, signal; and PD3 as the Control Clock, CCLK, signal.

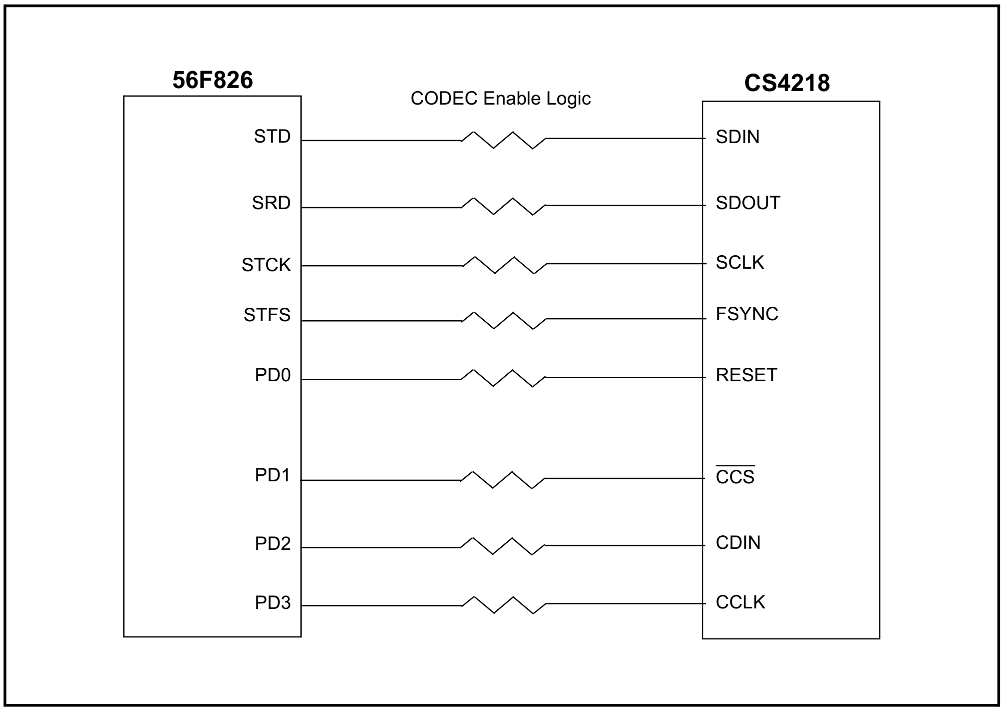


Figure 2-11. CS4218 Stereo Audio Codec

2.13 Daughter Card Connectors

The EVM board contains two daughter card expansion connectors. One connector, J1, contains the controller’s external memory bus signals. The other connector, J2, contains the controller’s peripheral port signals.

2.13.1 Memory Daughter Card Expansion Connector

The controller's external memory bus signals are connected to the Memory Daughter Card Expansion connector, J1. Table 2-8 shows the port signal to pin assignments.

Table 2-8. Memory Daughter Card Connector Description

J1			
Pin #	**Signal**	**Pin #**	**Signal**
1	A10	2	A11
3	A9	4	$\overline{DS}$
5	A8	6	A15
7	A7	8	A14
9	GND	10	GND
11	$\overline{WR}$	12	A13
13	D0	14	A12
15	D1	16	D8
17	D2	18	D9
19	GND	20	GND
21	D3	22	D10
23	D4	24	D11
25	D5	26	D12
27	D6	28	D13
29	GND	30	GND
31	D7	32	D14
33	$\overline{PS}$	34	D15
35	A0	36	$\overline{RD}$
37	A1	38	A6
39	GND	40	GND
41	A2	42	A5

Table 2-8. Memory Daughter Card Connector Description (Continued)

J1			
Pin #	**Signal**	**Pin #**	**Signal**
43	A3	44	A4
45	GND	46	GND
47	+3.3V	48	+3.3V
49	GND	50	GND
51	GND		

2.13.2 Peripheral Daughter Card Expansion Connector

The controller's peripheral port signals are connected to the Peripheral Daughter Card Expansion connector, J2. Table 2-9 shows the port signal to pin assignments.

Table 2-9. Peripheral Daughter Card Connector Description

J2			
Pin #	**Signal**	**Pin #**	**Signal**
1	PB0	2	PB1
3	CLKO	4	PB2
5	TA0	6	TA1
7	PB3	8	PB4
9	TA2	10	TA3
11	PB5	12	PB6
13	GND	14	GND
15	SRD	16	PB7
17	SRFS	18	PD0
19	SCLK	20	PD1
21	GND	22	GND
23	MOSI	24	PD2

Table 2-9. Peripheral Daughter Card Connector Description (Continued)

J2			
Pin #	**Signal**	**Pin #**	**Signal**
25	MISO	26	PD3
27	GND	28	GND
29	$\overline{\text{SS}}$	30	PD4
31	SRCK	32	PD5
33	STFS	34	PD6
35	$\overline{\text{RESET}}$	36	PD7
37	GND	38	GND
39	STD	40	RXD1
41	STCK	42	TXD1
43	$\overline{\text{IRQB}}$	44	RXD0
45	$\overline{\text{IRQA}}$	46	TXD0
47	+3.3V	48	+3.3V
49	GND	50	GND
51	GND		

2.14 Test Points

The 56F826EVM board has a total of seven test points. Three digital GND test points are located in corners of the board. The +5.0VA and AGND test points are located in the analog corner of the board. The +2.5V and +3.3V test points are located in the power supply section of the board.

Appendix A
56F826EVM Schematics

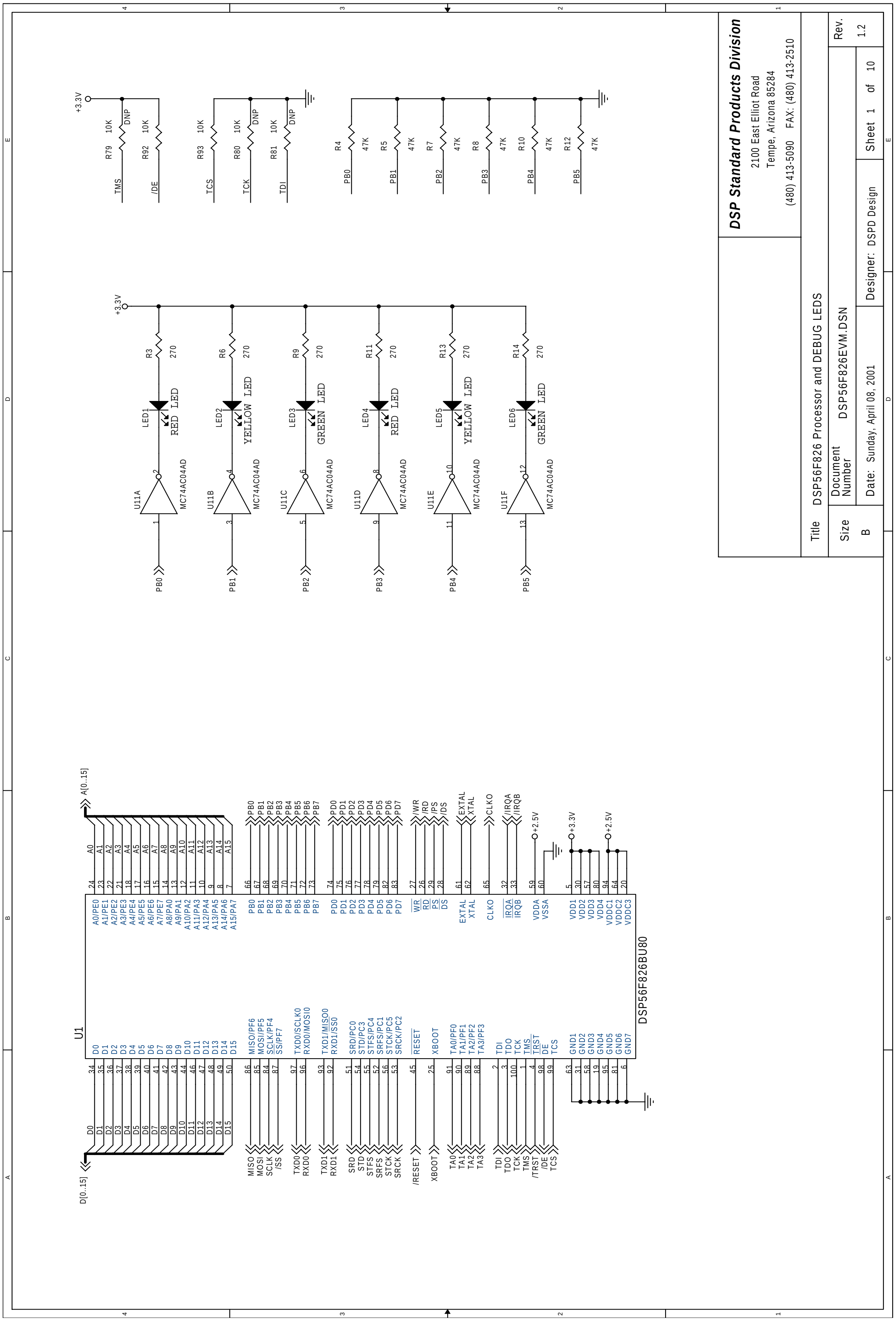

DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title
DSP56F826 Processor and DEBUG LEDS
Size
B
Document Number
DSP56F826EVM.DSN
Rev.
1.2
Date: Sunday, April 08, 2001
Designer: DSPD Design
Sheet 1 of 10
U1
DSP56F826BU80
A[0..15]
D[0..15]
+3.3V
+2.5V
U11A
U11B
U11C
U11D
U11E
U11F
MC74AC04AD
LED1
LED2
LED3
LED4
LED5
LED6
RED LED
YELLOW LED
GREEN LED
R3
R6
R9
R11
R13
R14
270
R79
R92
R93
R80
R81
10K
DNP
TMS
/DE
TCS
TCK
TDI
R4
R5
R7
R8
R10
R12
47K
PB0
PB1
PB2
PB3
PB4
PB5

Figure A-1. 56F826 Processor

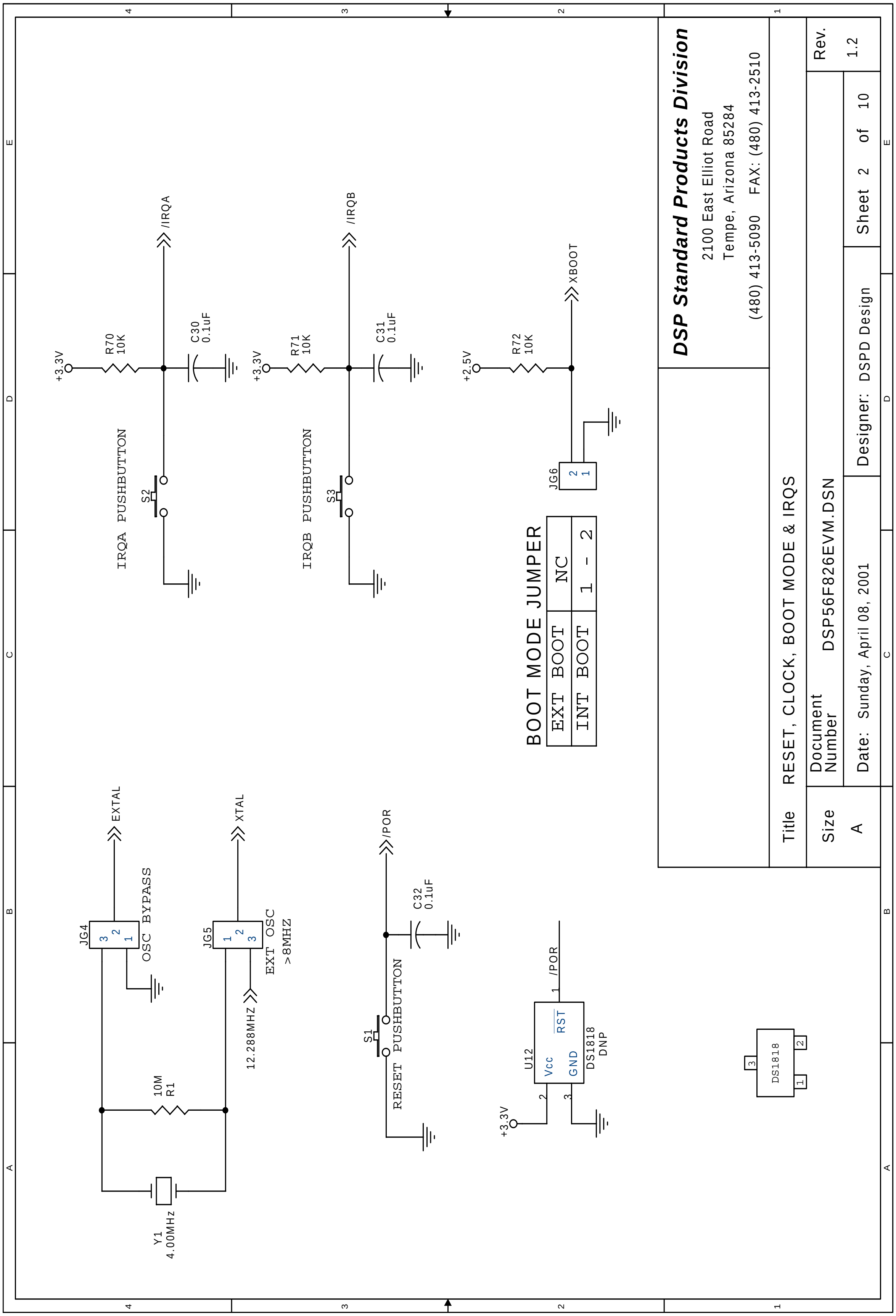
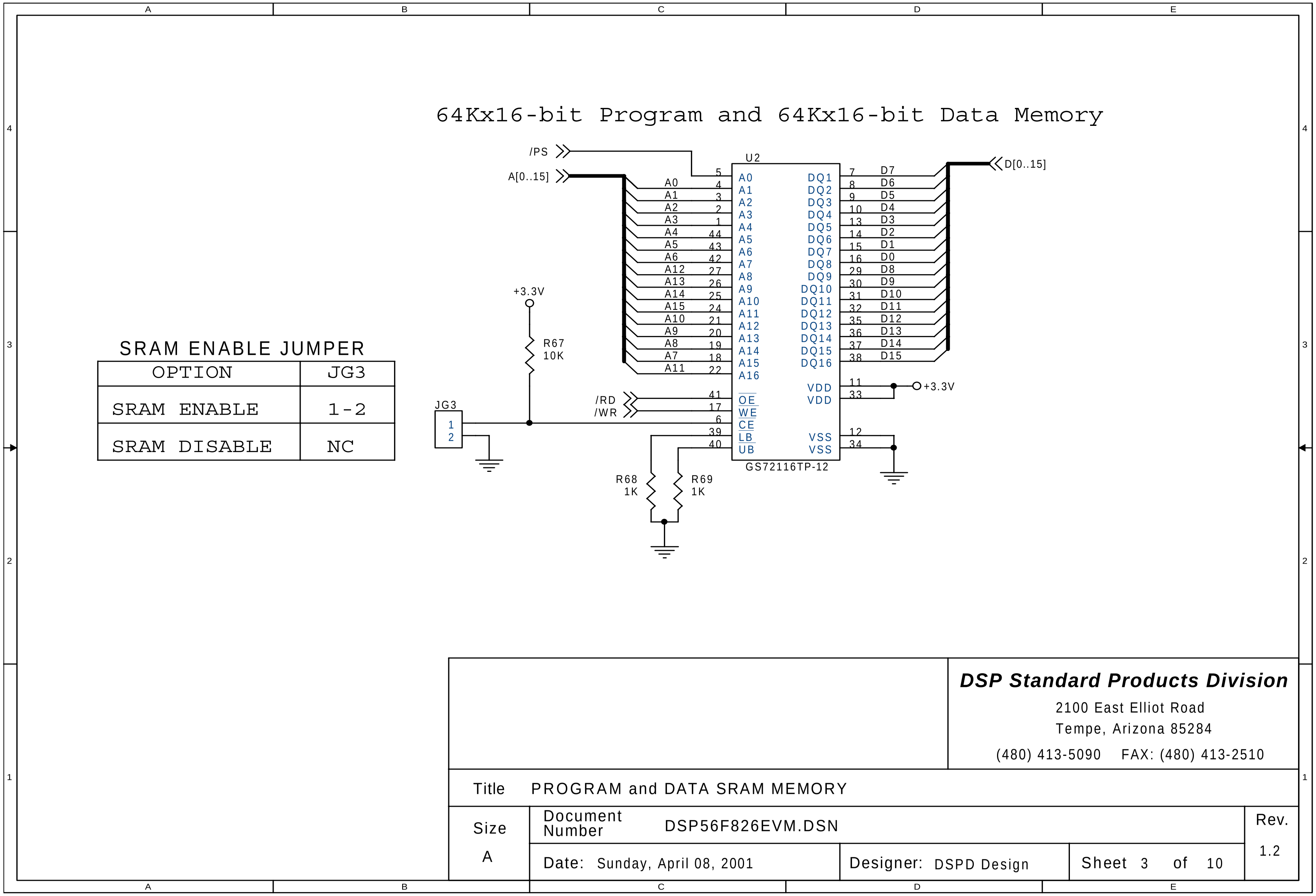

DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title
RESET, CLOCK, BOOT MODE & IRQS
Size
A
Document Number
DSP56F826EVM.DSN
Rev.
1.2
Date: Sunday, April 08, 2001
Designer: DSPD Design
Sheet 2 of 10
IRQA PUSHBUTTON
S2
+3.3V
R70
10K
C30
0.1uF
/IRQA
IRQB PUSHBUTTON
S3
+3.3V
R71
10K
C31
0.1uF
/IRQB
+2.5V
R72
10K
XBOOT
JG6
2
1
BOOT MODE JUMPER
EXT BOOT
NC
INT BOOT
1 - 2
JG4
3
2
1
OSC BYPASS
EXTAL
JG5
1
2
3
EXT OSC
>8MHZ
XTAL
12.288MHZ
10M
R1
Y1
4.00MHz
/POR
C32
0.1uF
S1
RESET PUSHBUTTON
U12
Vcc
GND
RST
2
3
1
/POR
+3.3V
DS1818
DNP
DS1818
3
2
1
A
B
C
D
E
1
2
3
4

Figure A-2. Reset, Mode, Clock & IRQs


64Kx16-bit Program and 64Kx16-bit Data Memory
/PS
A[0..15]
D[0..15]
U2
GS72116TP-12
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16
OE WE CE LB UB
VDD VDD VSS VSS
D7 D6 D5 D4 D3 D2 D1 D0 D8 D9 D10 D11 D12 D13 D14 D15
A0 A1 A2 A3 A4 A5 A6 A12 A13 A14 A15 A10 A9 A8 A7 A11
/RD
/WR
+3.3V
R67
10K
JG3
1
2
R68
1K
R69
1K
+3.3V
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title PROGRAM and DATA SRAM MEMORY
Size A
Document Number DSP56F826EVM.DSN
Rev. 1.2
Date: Sunday, April 08, 2001
Designer: DSPD Design
Sheet 3 of 10

SRAM ENABLE JUMPER

OPTION	JG3
SRAM ENABLE	1-2
SRAM DISABLE	NC

Figure A-3. Program & Data SRAM Memory

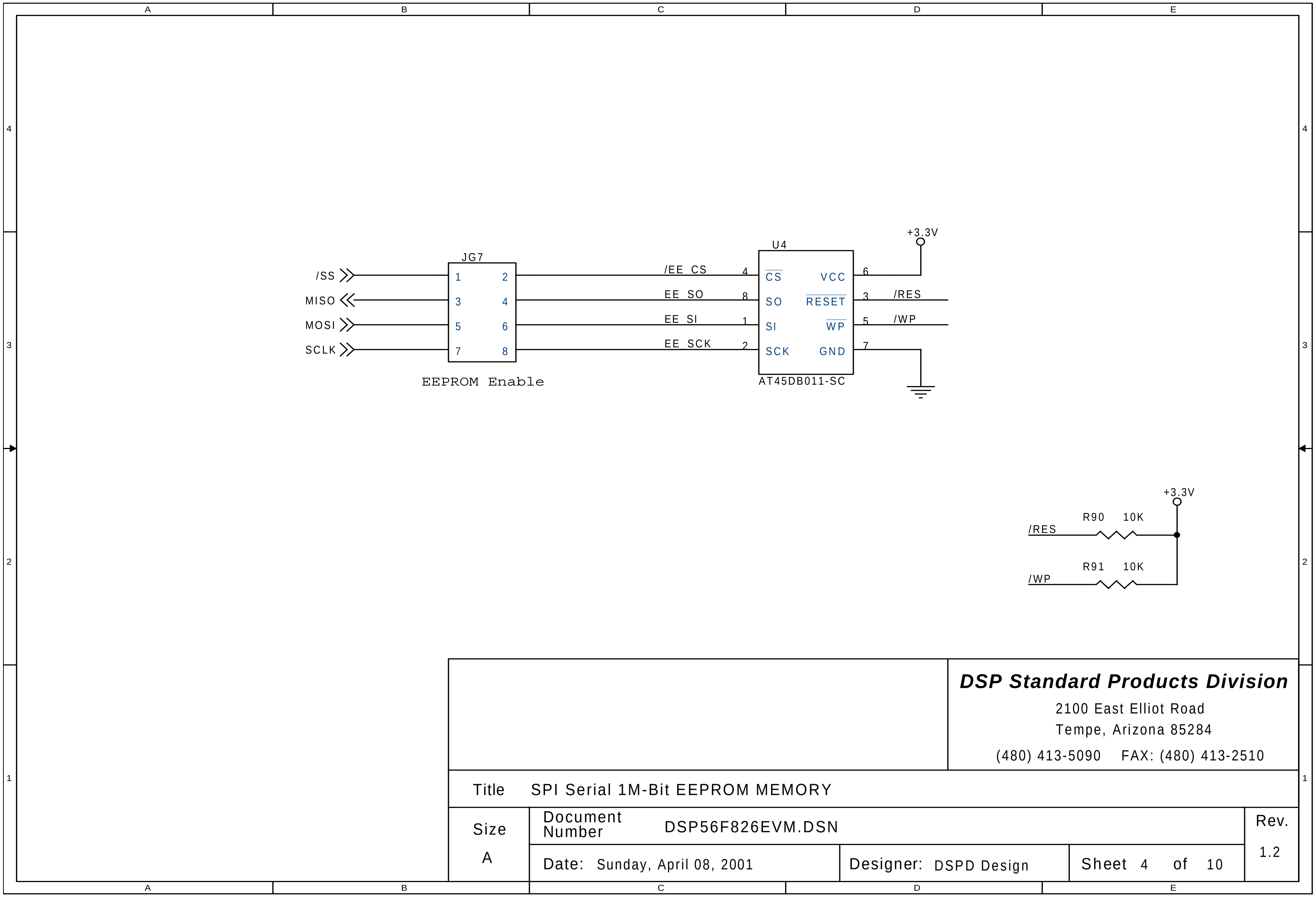

A
B
C
D
E
4
3
2
1
/SS
MISO
MOSI
SCLK
JG7
1
2
3
4
5
6
7
8
EEPROM Enable
/EE CS
EE SO
EE SI
EE SCK
U4
CS
SO
SI
SCK
VCC
RESET
WP
GND
AT45DB011-SC
+3.3V
/RES
/WP
R90 10K
R91 10K
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title SPI Serial 1M-Bit EEPROM MEMORY
Size
A
Document Number DSP56F826EVM.DSN
Rev.
1.2
Date: Sunday, April 08, 2001
Designer: DSPD Design
Sheet 4 of 10

Figure A-4. SPI Serial 1M-bit Serial EEPROM Memory

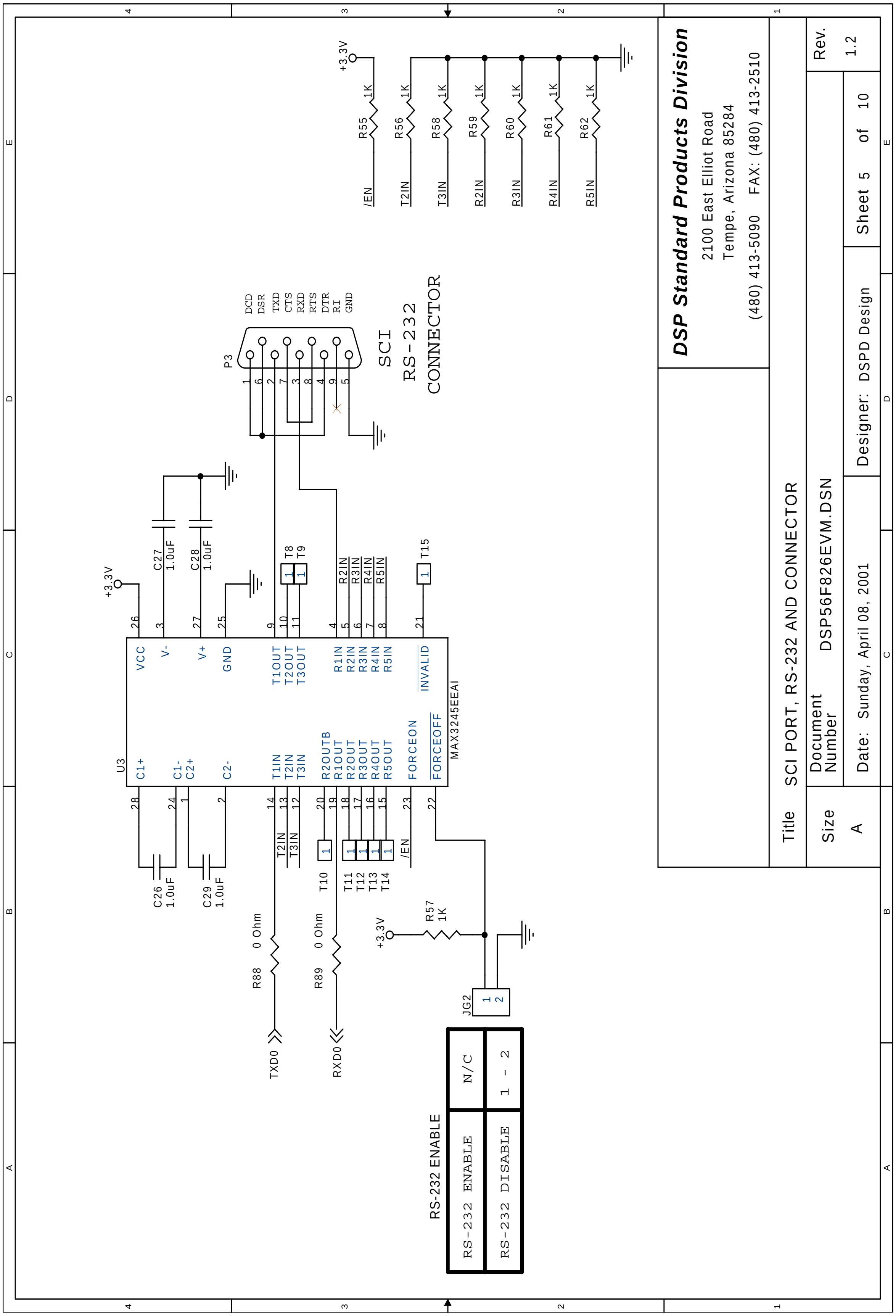
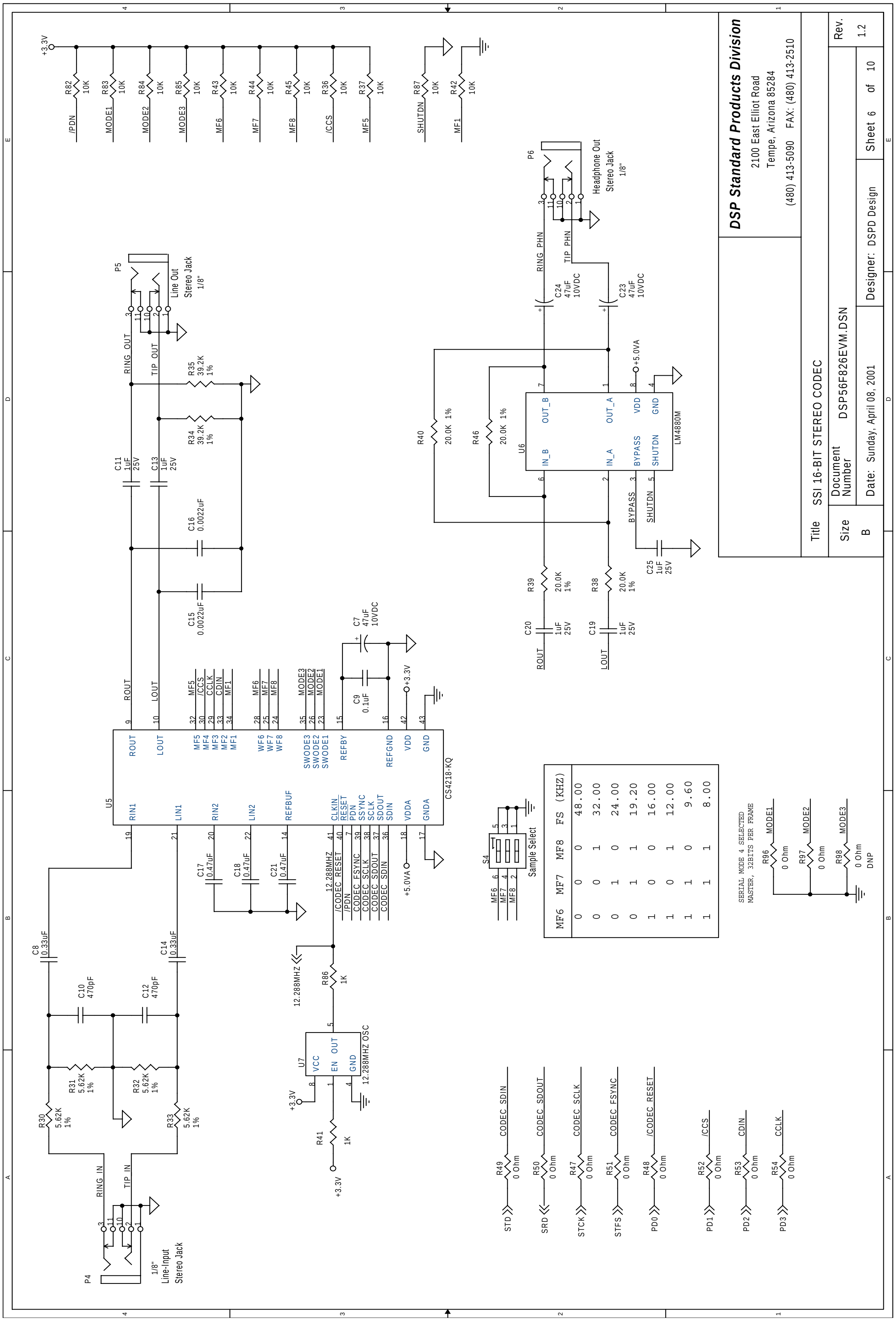
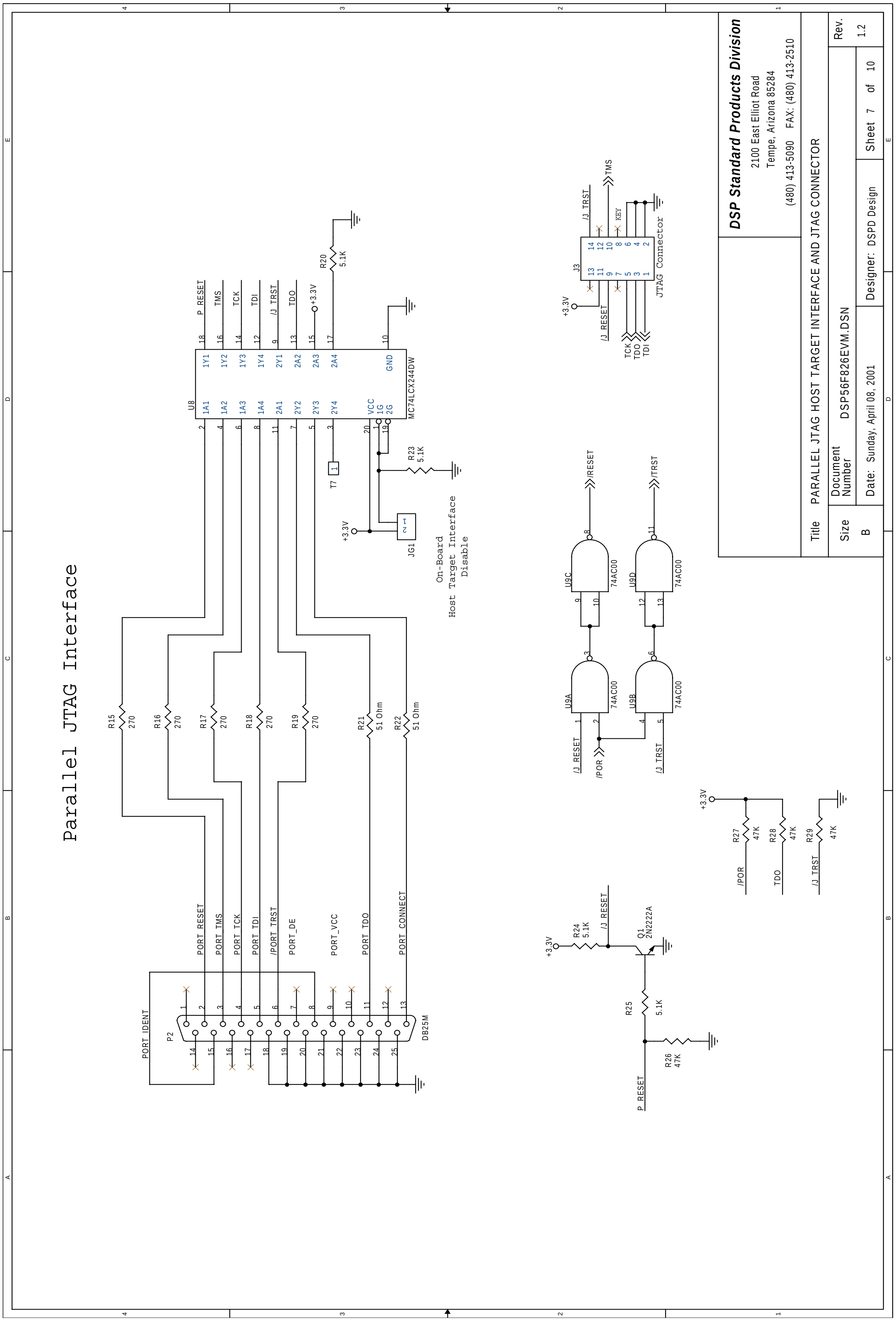

U3
MAX3245EEAI
C1+
C1-
C2+
C2-
T1IN
T2IN
T3IN
R2OUTB
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
FORCEON
FORCEOFF
VCC
V-
V+
GND
T1OUT
T2OUT
T3OUT
R1IN
R2IN
R3IN
R4IN
R5IN
INVALID
C26 1.0uF
C27 1.0uF
C28 1.0uF
C29 1.0uF
+3.3V
T8
T9
T10
T11
T12
T13
T14
T15
/EN
R88 0 Ohm
R89 0 Ohm
TXD0
RXD0
R57 1K
JG2
P3
DCD
DSR
TXD
CTS
RXD
RTS
DTR
RI
GND
SCI
RS-232
CONNECTOR
R55 1K
R56 1K
R58 1K
R59 1K
R60 1K
R61 1K
R62 1K
RS-232 ENABLE
RS-232 ENABLE
N/C
RS-232 DISABLE
1 - 2
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title SCI PORT, RS-232 AND CONNECTOR
Size A
Document Number DSP56F826EVM.DSN
Rev. 1.2
Date: Sunday, April 08, 2001
Sheet 5 of 10
Designer: DSPD Design

Figure A-5. SCI Port, RS-232 and Connector


DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title
SSI 16-BIT STEREO CODEC
Size
B
Document Number
DSP56F826EVM.DSN
Rev.
1.2
Date: Sunday, April 08, 2001
Sheet 6 of 10
Designer: DSPD Design
U5
CS4218-KQ
U6
LM4880M
U7
12.288MHZ OSC
P4
1/8" Line-Input Stereo Jack
P5
Line Out Stereo Jack 1/8"
P6
Headphone Out Stereo Jack 1/8"
S4
Sample Select
SERIAL MODE 4 SELECTED
MASTER, 32BITS PER FRAME
ROUT
LOUT
RIN1
LIN1
RIN2
LIN2
REFBUF
REFBY
REFGND
CLKIN
RESET
PDN
SSYNC
SCLK
SDOUT
SDIN
VDDA
GNDA
VDD
GND
MF5
MF4
MF3
MF2
MF1
WF6
WF7
WF8
SWODE3
SWODE2
SWODE1
IN_B
OUT_B
IN_A
OUT_A
BYPASS
SHUTDN
VCC
EN
OUT
+3.3V
+5.0VA
RING IN
TIP IN
RING OUT
TIP OUT
RING PHN
TIP PHN
12.288MHZ
/CODEC RESET
/PDN
CODEC FSYNC
CODEC SCLK
CODEC SDOUT
CODEC SDIN
/CCS
CDIN
CCLK
MODE1
MODE2
MODE3
MF6
MF7
MF8
STD
SRD
STCK
STFS
PD0
PD1
PD2
PD3
R82 10K
R83 10K
R84 10K
R85 10K
R43 10K
R44 10K
R45 10K
R36 10K
R37 10K
R87 10K
R42 10K
R35 39.2K 1%
R34 39.2K 1%
R40 20.0K 1%
R46 20.0K 1%
R39 20.0K 1%
R38 20.0K 1%
R30 5.62K 1%
R31 5.62K 1%
R32 5.62K 1%
R33 5.62K 1%
R86 1K
R41 1K
R49 0 Ohm
R50 0 Ohm
R47 0 Ohm
R51 0 Ohm
R48 0 Ohm
R52 0 Ohm
R53 0 Ohm
R54 0 Ohm
R96 0 Ohm
R97 0 Ohm
R98 0 Ohm DNP
C11 1uF 25V
C13 1uF 25V
C16 0.0022uF
C15 0.0022uF
C7 47uF 10VDC
C9 0.1uF
C8 0.33uF
C14 0.33uF
C10 470pF
C12 470pF
C17 0.47uF
C18 0.47uF
C21 0.47uF
C20 1uF 25V
C19 1uF 25V
C24 47uF 10VDC
C23 47uF 10VDC
C25 1uF 25V

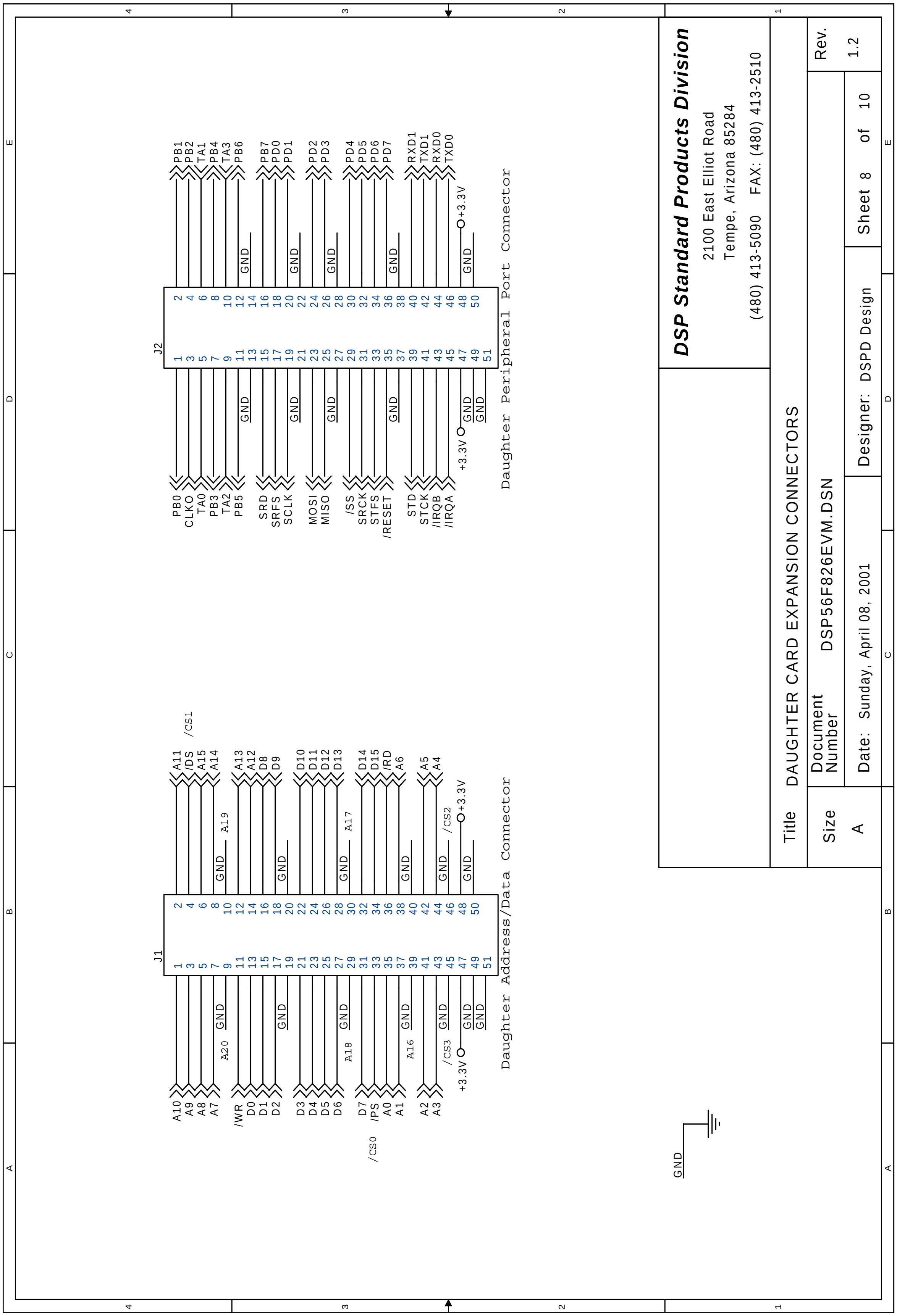
MF6	MF7	MF8	FS (KHZ)
0	0	0	48.00
0	0	1	32.00
0	1	0	24.00
0	1	1	19.20
1	0	0	16.00
1	0	1	12.00
1	1	0	9.60
1	1	1	8.00

Figure A-6. SSI 16-bit Stereo Codec



Parallel JTAG Interface
PORT_IDENT
P2
DB25M
PORT_RESET
PORT_TMS
PORT_TCK
PORT_TDI
/PORT_TRST
PORT_DE
PORT_VCC
PORT_TDO
PORT_CONNECT
R15 270
R16 270
R17 270
R18 270
R19 270
R21 51 Ohm
R22 51 Ohm
U8
MC74LCX244DW
1A1
1A2
1A3
1A4
2A1
2Y2
2Y3
2Y4
VCC
1G
2G
1Y1
1Y2
1Y3
1Y4
2Y1
2A2
2A3
2A4
GND
P_RESET
TMS
TCK
TDI
/J_TRST
TDO
+3.3V
R20 5.1K
T7
R23 5.1K
JG1
On-Board
Host Target Interface
Disable
U9A
U9B
U9C
U9D
74AC00
/J_RESET
/POR
/J_TRST
/RESET
/TRST
J3
JTAG Connector
KEY
/J_RESET
/J_TRST
TCK
TDO
TDI
TMS
R24 5.1K
Q1 2N2222A
R25 5.1K
R26 47K
P_RESET
R27 47K
R28 47K
R29 47K
/POR
TDO
/J_TRST
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090   FAX: (480) 413-2510
Title
PARALLEL JTAG HOST TARGET INTERFACE AND JTAG CONNECTOR
Size
B
Document Number
DSP56F826EVM.DSN
Rev.
1.2
Date: Sunday, April 08, 2001
Sheet 7 of 10
Designer: DSPD Design

Figure A-7. Parallel JTAG Host Target Interface and JTAG Connector


Daughter Address/Data Connector
J1
A10
A9
A8
A7
/WR
D0
D1
D2
D3
D4
D5
D6
D7
/PS
A0
A1
A2
A3
A20
A18
A16
/CS0
/CS3
+3.3V
GND
A11
/DS
A15
A14
/CS1
A13
A12
D8
D9
D10
D11
D12
D13
D14
D15
/RD
A6
A5
A4
A19
A17
/CS2
Daughter Peripheral Port Connector
J2
PB0
CLKO
TA0
PB3
TA2
PB5
SRD
SRFS
SCLK
MOSI
MISO
/SS
SRCK
STFS
/RESET
STD
STCK
/IRQB
/IRQA
PB1
PB2
TA1
PB4
TA3
PB6
PB7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
RXD1
TXD1
RXD0
TXD0
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title
DAUGHTER CARD EXPANSION CONNECTORS
Size
A
Document Number
DSP56F826EVM.DSN
Rev.
1.2
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Designer: DSPD Design

Figure A-8. Daughter Card Expansion Connectors

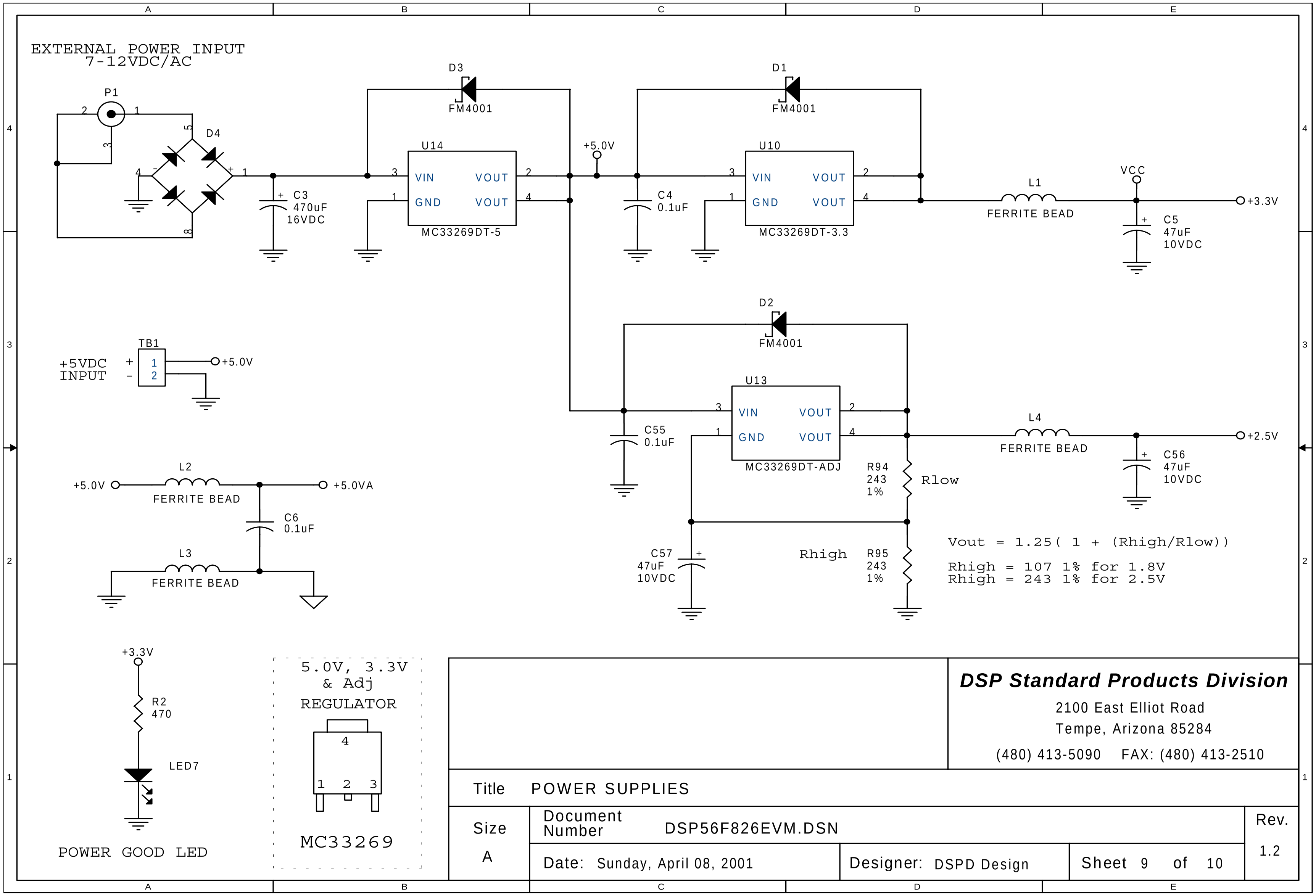
EXTERNAL POWER INPUT
7-12VDC/AC
P1
D4
C3
470uF
16VDC
D3
FM4001
U14
VIN
GND
VOUT
VOUT
MC33269DT-5
+5.0V
D1
FM4001
U10
MC33269DT-3.3
C4
0.1uF
L1
FERRITE BEAD
VCC
+3.3V
C5
47uF
10VDC
D2
FM4001
U13
MC33269DT-ADJ
C55
0.1uF
L4
FERRITE BEAD
+2.5V
C56
47uF
10VDC
R94
243
1%
Rlow
C57
47uF
10VDC
Rhigh
R95
243
1%
Vout = 1.25(1 + (Rhigh/Rlow))
Rhigh = 107 1% for 1.8V
Rhigh = 243 1% for 2.5V
+5VDC INPUT
TB1
+5.0V
L2
FERRITE BEAD
+5.0VA
C6
0.1uF
L3
FERRITE BEAD
+3.3V
R2
470
LED7
POWER GOOD LED
5.0V, 3.3V & Adj REGULATOR
MC33269
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title POWER SUPPLIES
Size A
Document Number DSP56F826EVM.DSN
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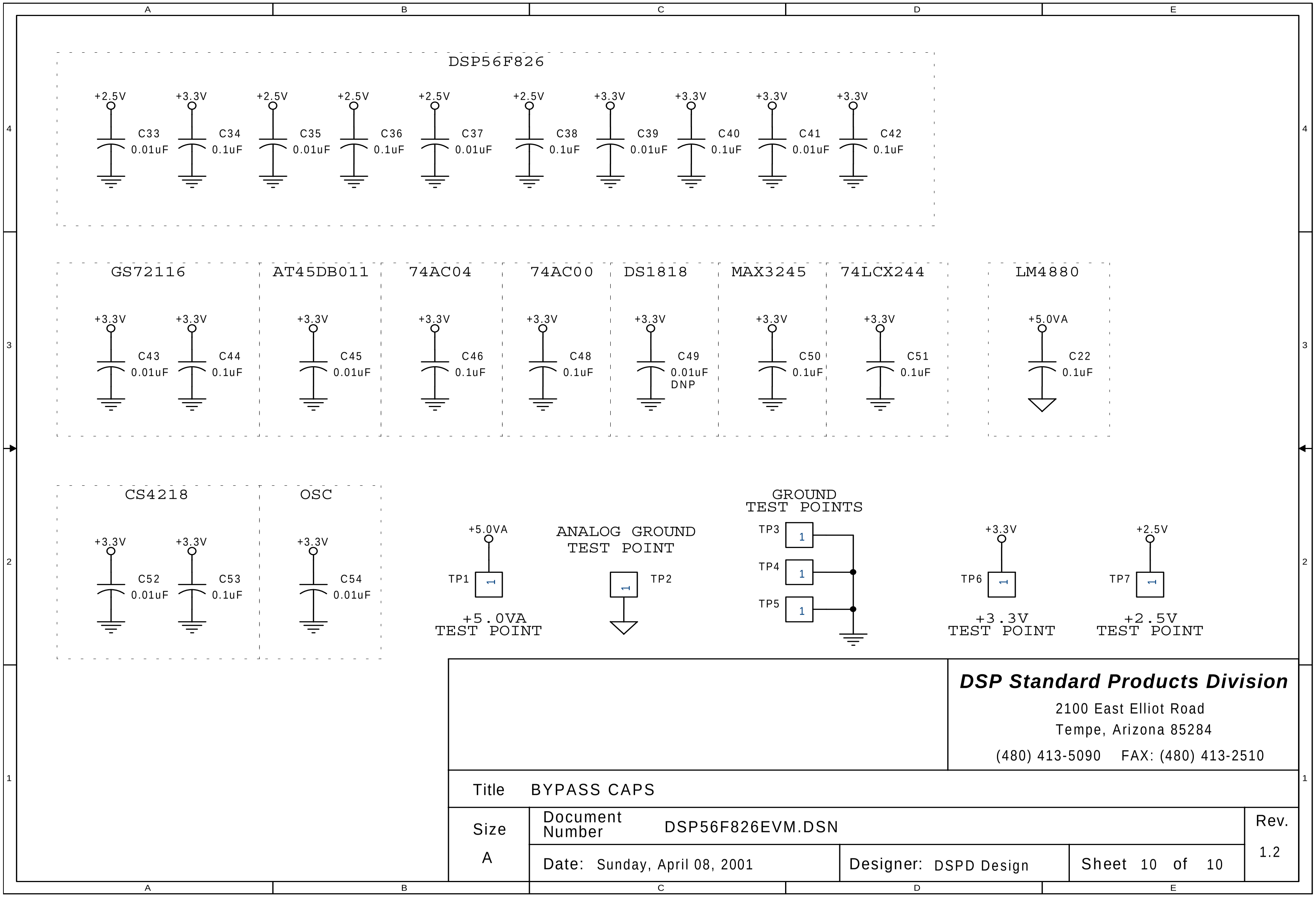
Figure A-9. Power Supplies


DSP56F826
+2.5V C33 0.01uF
+3.3V C34 0.1uF
+2.5V C35 0.01uF
+2.5V C36 0.1uF
+2.5V C37 0.01uF
+2.5V C38 0.1uF
+3.3V C39 0.01uF
+3.3V C40 0.1uF
+3.3V C41 0.01uF
+3.3V C42 0.1uF
GS72116
+3.3V C43 0.01uF
+3.3V C44 0.1uF
AT45DB011
+3.3V C45 0.01uF
74AC04
+3.3V C46 0.1uF
74AC00
+3.3V C48 0.1uF
DS1818
+3.3V C49 0.01uF DNP
MAX3245
+3.3V C50 0.1uF
74LCX244
+3.3V C51 0.1uF
LM4880
+5.0VA C22 0.1uF
CS4218
+3.3V C52 0.01uF
+3.3V C53 0.1uF
OSC
+3.3V C54 0.01uF
+5.0VA TP1 1
+5.0VA TEST POINT
ANALOG GROUND TEST POINT
TP2 1
GROUND TEST POINTS
TP3 1
TP4 1
TP5 1
+3.3V TP6 1
+3.3V TEST POINT
+2.5V TP7 1
+2.5V TEST POINT
DSP Standard Products Division
2100 East Elliot Road
Tempe, Arizona 85284
(480) 413-5090 FAX: (480) 413-2510
Title BYPASS CAPS
Size A
Document Number DSP56F826EVM.DSN
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A B C D E
1 2 3 4

Figure A-10. Bypass Caps

Appendix B
56F826EVM Bill of Material

Qty.	Description	Ref. Designators	Vendor Part #s
		Integrated Circuits	
1	DSP56F826BU80	U1	Freescale, DSP56F826BU80
1	GS72116	U2	GSI, GS72116TP-12
1	MAX3245	U3	Maxim, MAX3245EEAI
1	AT45DB011	U4	Atmel, AT45DB011-SC
1	CS4218	U5	Crystal Semiconductor, CS4218-KQ
1	LM4880	U6	National Semiconductor, LM4880M
1	12.288MHZ OSC	U7	Epson, SG-531P-12.288MC
1	74LCX244	U8	ON Semiconductor, MC74LCX244ADW
1	74AC00	U9	Fairchild, 74AC00SC
1	+3.3V Voltage Regulator	U10	ON Semiconductor, MC33269DT-3.3
1	74AC04	U11	ON Semiconductor, MC74AC04AD
1	+2.5V Voltage Regulator	U13	ON Semiconductor, MC33269DT-ADJ
1	+5.0V Voltage Regulator	U14	ON Semiconductor, MC33269DT-5
		Resistors	
1	10M Ω	R1	SMEC, RC73L2A10MOHMJT
1	470 Ω	R2	SMEC, RC73L2A470OHMJT
11	270 Ω	R3, R6, R9, R11, R13—R19	SMEC, RC73L2A270OHMJT
10	47K Ω	R4, R5, R7, R8, R10, R12, R26—R29	SMEC, RC73L2A47KOHMJT
4	5.1K Ω	R20, R23—R25	SMEC, RC73L2A5.1KOHMJT

Qty.	Description	Ref. Designators	Vendor Part #s
Resistors (Continued)			
2	51 Ω	R21, R22	SMEC, RC73L2A51OHMJT
4	5.62K Ω, 1%	R30—R33	SMEC, RC73L2A5.62KOHMFT
2	39.2K Ω, 1%	R34, R35	SMEC, RC73L2A39.2KOHMFT
19	10K Ω	R36, R37, R42—R45, R67, R70—R72, R82—R85, R87, R90—R93	SMEC, RC73L2A10KOHMJT
4	20.0K Ω, 1%	R38—R40, R46	SMEC, RC73L20.0KOHMFT
12	1K Ω	R41, R55—R62, R68, R69, R86	SMEC, RC73L2A1KOHMJT
12	0 Ω	R47—R54, R88, R89, R96, R97	SMEC, RC73JP2A
2	243 Ω, 1%	R94, R95	SMEC, RC73L243OHMFT
Inductors			
4	1.0mH FERRITE BEAD	L1, L2, L3, L4	Panasonic, EXC-ELSA35V
LEDs			
2	Red LED	LED1, LED4	Hewlett-Packard, HSMS-C650
2	Yellow LED	LED2, LED5	Hewlett-Packard, HSMY-C650
3	Green LED	LED3, LED6, LED7	Hewlett-Packard, HSMG-C650
Diodes			
2	S2B-FM401	D1, D2, D3	Vishay, DL4001DICT
1	1A Bridge Rectifier	D4	General Semiconductor, DF02S
Capacitors			
1	470µF, 16V DC	C3	ELMA, RV-16V471MH10R
19	0.1µF	C4, C6, C9, C22, C30—C32, C34, C36, C38, C40, C42, C44, C46, C48, C50, C51, C53, C55	SMEC, MCCE104K2NR-T1
6	47µF, 16V DC	C5, C7, C23, C24, C56, C57	ELMA, RV2-16V470M-R
2	0.33µF	C8, C14	SMEC, MCCE334K3NR-T1
2	470pF	C10, C12	SMEC, MCCE471J2NO-T1
9	1.0µF, 25V DC	C11, C13, C19, C20, C25—C29	SMEC, MCCE105K3NR-T1

Qty.	Description	Ref. Designators	Vendor Part #s
2	0.0022µF	C15, C16	SMEC, MCCE222K2NR-T1
3	0.47µF	C17, C18, C21	SMEC, MCCE474K3NR-T1
9	0.01µF	C33, C35, C37, C39, C41, C43, C45, C52, C54	SMEC, MCCE103K2NR-T1
		Jumpers	
4	1 × 2 Bergstick	JG1, JG2, JG3, JG6	SAMTEC, TSW-102-07-S-S
2	3 × 1 Bergstick	JG4, JG5	SAMTEC, TSW-103-07-S-S
1	4 × 2 Bergstick	JG7	SAMTEC, TSW-104-07-S-D
		Test Points	
7	1 × 1 Bergstick	TP1—TP7	Samtec, TSW-101-07-S-S
		Crystals	
1	4.00MHz Crystal	Y1	CTS, ATS04ASM-T
		Connectors	
1	2.1mm coax Power Connector	P1	Switchcraft, RAPC-722
1	DB25M Connector	P2	AMPHENOL, 617-C025P-AJ121
1	DE9S Connector	P3	AMPHENOL, 617-C009S-AJ120
3	1/8” Stereo Jack	P4—P6	Switchcraft, 35RAPC4BHN2
2	51-Pin HD Connector	J1, J2	BERG, 91930-21151
1	7 x 2 Bergstick	J3	SAMTEC, TSW-107-07-S-D
1	2-Pin Terminal Block	TB1	On-Shore Technology, ED500/2DS
		Switches	
3	SPST Pushbutton	S1—S3	Panasonic, EVQ-PAD05R
1	3-Position DIP SW	S4	CTS, 209-3LPST
		Transistors	
1	2N2222A	Q1	ZETEX, FMMT2222ACT
		Miscellaneous	
8	Shunt	SH1–SH8	Samtec, SNT-100-BL-T
4	Rubber Feet	RF1–RF4	3M, SJ5018BLKC

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  WS Preface-ix

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