MOTOROLA

AAL-2 Switch Application Guide

C-WARE SOFTWARE TOOLSET, VERSION 2.2

CSTAA2-UG/D
Rev 01

CONTENTS

ABOUT THIS GUIDE

Guide Overview

This document describes the design and features of the C-Ware AAL-2 Switch application (application identifier **aal2Switch**).

This guide is intended for users of the C-Ware Software Toolset (CST) who want to build any application provided in the CST or who want to develop new C-Ware-based applications targeted to a C-Port network processor device.

This guide contains one chapter that covers the following major topics:

- Overview
- System Configuration
- Application Feature Overview
- Application Control and Data Flow
- Resource Utilization
- Supplied Application Files
- Design Issues

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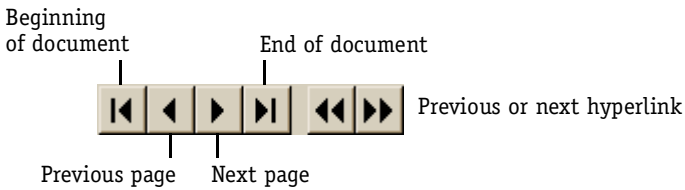

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Table 1 Navigating Within a PDF Document

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Guide Conventions

The following visual elements are used throughout this guide, where applicable:

This icon and text designates information of special note.

Warning: *This icon and text indicate a potentially dangerous procedure. Instructions contained in the warnings must be followed.*

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n History

Table 2 provides details about changes made for each revision of this guide.

Table 2 *Build System Conventions Guide* Revision History

REVISION DATE	CST REVISION	CDS REVISION	CHANGES
September 14, 2001	2.0	2.0	New document.

ıted Product umentation

Table 3 lists the documentation for the C-Ware library of reference applications.

Table 3 C-Ware Application Library Documentation Set

DOCUMENT NAME	PURPOSE	DOCUMENT ID
AAL-2 Switch Application Guide	Describes the key characteristics of the **aal2Switch** application.	CSTAA2-UG
AAL-5 Fabric Port SAR to Gigabit Ethernet Switch Application Guide	Describes the key characteristics of the **gbeOc12SarFp** applications.	CSTAA5F2G-UG
AAL-5 SAR Application Guide	Describes the key characteristics of the **oc3SarQ** application.	CSTAA5-UG
AAL-5 SAR to Gigabit Ethernet Switch Application Guide	Describes the key characteristics of the **gbeOc12Sar** and **gbeOc12SarQ** applications.	CSTAA52G-UG
ATM Cell Switch Application Guide	Describes the key characteristics of the **atmCellSwitchQ** application.	CSTAATMCS-UG
FibreChannel to Gigabit Ethernet IP Gateway Application Guide	Describes the key characteristics of the **gbeFc** application.	CSTAFC2G-UG
Frame Relay to ATM to 10/100 Ethernet Switch Router Application Guide	Describes the key characteristics of the **switchRouter** application.	CSTAFRAE-UG
Gigabit Ethernet Switch Application Guide	Describes the key characteristics of the **gbeSwitch** application.	CSTAGBE-UG
Multi-PHY Switch Application Guide	Describes the key characteristics of the **mphySwitch** application.	CSTAMPHYS-UG
Packet Over SONET Switch Application Guide	Describes the key characteristics of the **posOc48SwitchQ** application.	CSTAPOS-UG
Packet Over SONET to Ethernet Switch Application Guide	Describes the key characteristics of the **enetOc12Switch** application.	CSTAPOS2E-UG
Packet Over SONET to Gigabit Ethernet Switch Application Guide	Describes the key characteristics of the **posGbeSwitch** application.	CSTAPOS2G-UG
Voice Over IP to Voice Over ATM Media Gateway Application Guide	Describes the key characteristics of the **voIpToVoAtmSwitch** application.	CSTAVOIP-UG
Fabric Processor Configuration Component Guide	Describes the key characteristics of the **fabrics** application component.	CSTCFPC-UG
GMII Gigabit Ethernet Autonegotiation Component Guide	Describes the key characteristics of the **gmiiAutoNeg** application component.	CSTCGEAN-UG
ICMP Support Component Guide	Describes the key characteristics of the **ip** application component.	CSTCICMP-UG
MPC750 SBC Host Stack Support Component Guide	Describes the key characteristics of the **stackSupport** application component.	CSTCMHSS-UG
PHY Configuration Component Guide	Describes the key characteristics of the **phy** application component.	CSTCPHYC-UG

C-Ware Application Library Documentation Set (continued)

NT NAME	PURPOSE	DOCUMENT ID
QMU Configuration and RC Support Component Guide	Describes the key characteristics of the **queueUtils** application component.	CSTCQRCS-UG
SONET Monitoring Component Guide	Describes the key characteristics of the **sonet** application component.	CSTCSMC-UG
TLU Configuration Component Guide	Describes the key characteristics of the **tableUtils** application component.	CSTCTLUC-UG

Chapter 1

AAL-2 SWITCH APPLICATION GUIDE

Overview

This document is a functional and design specification for the **aal2Switch** application in the C-Ware Software Toolset (CST).

This document goes into detail about the following topics:

- System Configuration
- Application Feature Overview
- Application Control and Data Flow
- Resource Utilization
- Supplied Application Files
- Design Issues

Prerequisite Reading

Readers of this document are assumed to have read or be familiar with the topics in the following documents in the CST:

- *C-Ware Software Toolset Getting Started Guide* - How to get started with the CST.
- *Build System Conventions* - Description of how the build system works.

System Configuration

This application runs on the following modules as a part of the C-Ware Development System (CDS):

- C-5 Switch Module

This application runs with the following CDS Physical Interface Modules (PIMs):

- Combo (4 x 10/100, 4 x OC-3c, 1 x Gigabit Ethernet (TBI))

tion Feature w

The **aal2Switch** application in the CST is a two-port, OC-3c ATM adaptation layer 2 switch.

Feature Overview and Standards Support

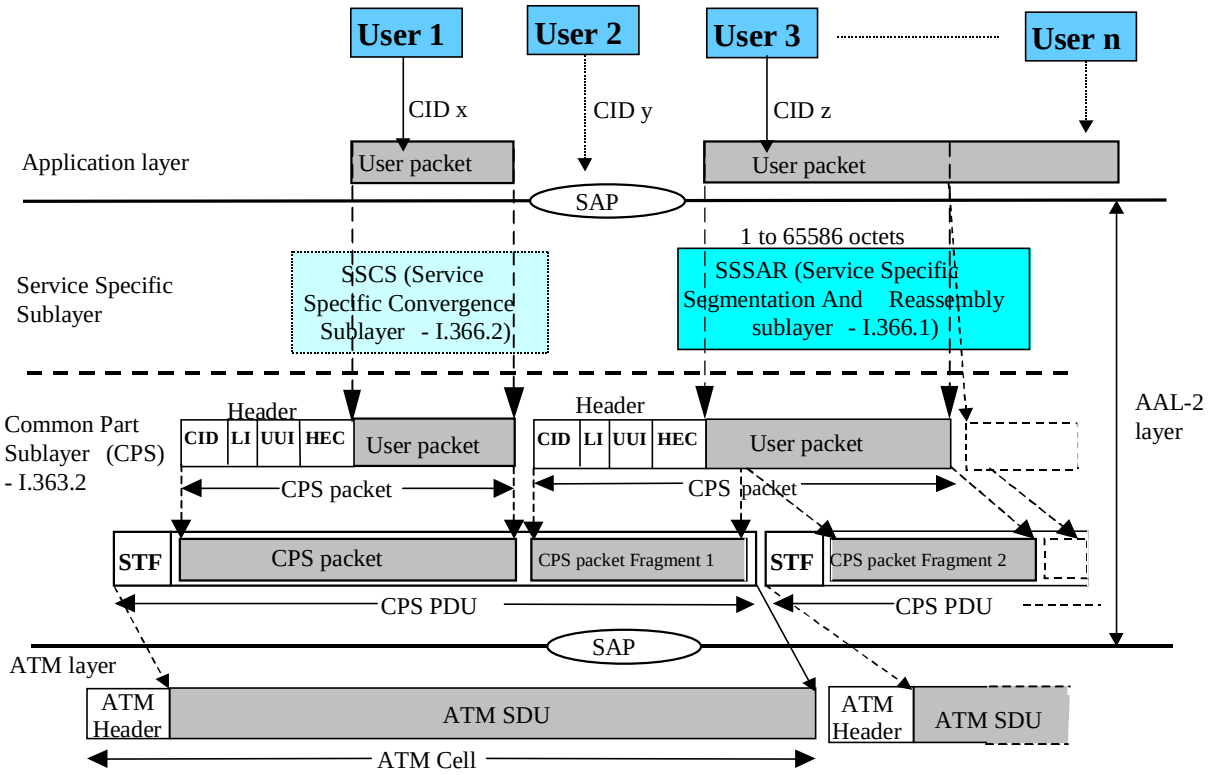
AAL-2 is an efficient transport mechanism for carrying low rate, real-time, variable bit rate traffic streams (for example, compressed/non-compressed voice streams) over an ATM connection. Typical applications that make use of AAL-2 are ATM Trunking and UMTS terrestrial radio access network (UTRAN).

Figure 1 on page 13 shows the protocol structure of ATM/AAL-2. AAL-2 Common Part Sublayer (CPS) provides multiplexing of different users on to a single ATM connection. The packets from these users are multiplexed into the payload of the ATM cell stream at the sending side and demultiplexed at the receiving side.

CPS packet has a header of three octets and a payload of variable length up to a maximum value of 64 octets (default maximum length is 45). The header consists of the following four fields:

- 8 bit Channel Identifier (CID), which identifies the AAL-2 channel (CPS user). AAL-2 channel is bi-directional (that is, same CID is used for both directions). The value "0" is not used and values "1" to "7" are reserved.
- 6 bit Length Indicator (LI), which indicates the length of the CPS packet payload. Default maximum length is 45 octets and can be set to 64.
- 5 bit User-to-User Indication (UUI), which is used to convey specific information transparently between the CPS users (that is, between SSCS entities or between Layer Management), and to distinguish between the SSCS entities and Layer Management users of the CPS. The UUI field provides for 32 codepoints, "0" ... "31". Codepoints 0...27 are available for SSCS entities, codepoints 30...31 are available to Layer Management, and codepoints 28...29 are reserved for future standardization.
- Header Error Control (HEC), which detects bit errors in the header by a 5 bit CRC.

Figure 1 ATM/AAL-2 Protocol structure



APacking/Multiplexing and Unpacking/Demultiplexing of CPS packets is done using the Start Field (STF). The STF consists of:

- 6 bit Offset Field (OSF), which points to the start of the first CPS packet (or to start of PAD field in the absence of any CPS packet start) in CPS PDU. The value 47 indicates there is no start (i.e. whole CPS PDU is part of a CPS packet). Values greater than 47 are not allowed.
- 1 bit Sequence Number (SN), which detects the lost ATM cell.
- Parity bit (P), which detect errors in the STF.

Figure 2 illustrates ATM Trunking, which is used in AAL-2 to provide Narrowband Services to support a broad range of applications involving interconnection of an IWF with narrowband and broadband facilities and interworking with various other telecommunications devices including PBXs, ATM network switches, and far-end IWFs.

Figure 2 ATM Trunking using AAL-2 for Narrowband Services

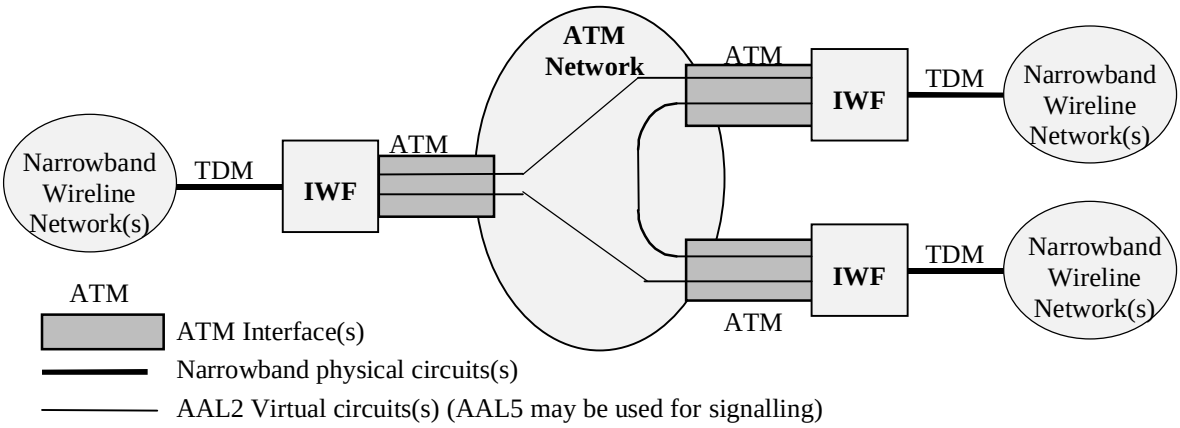
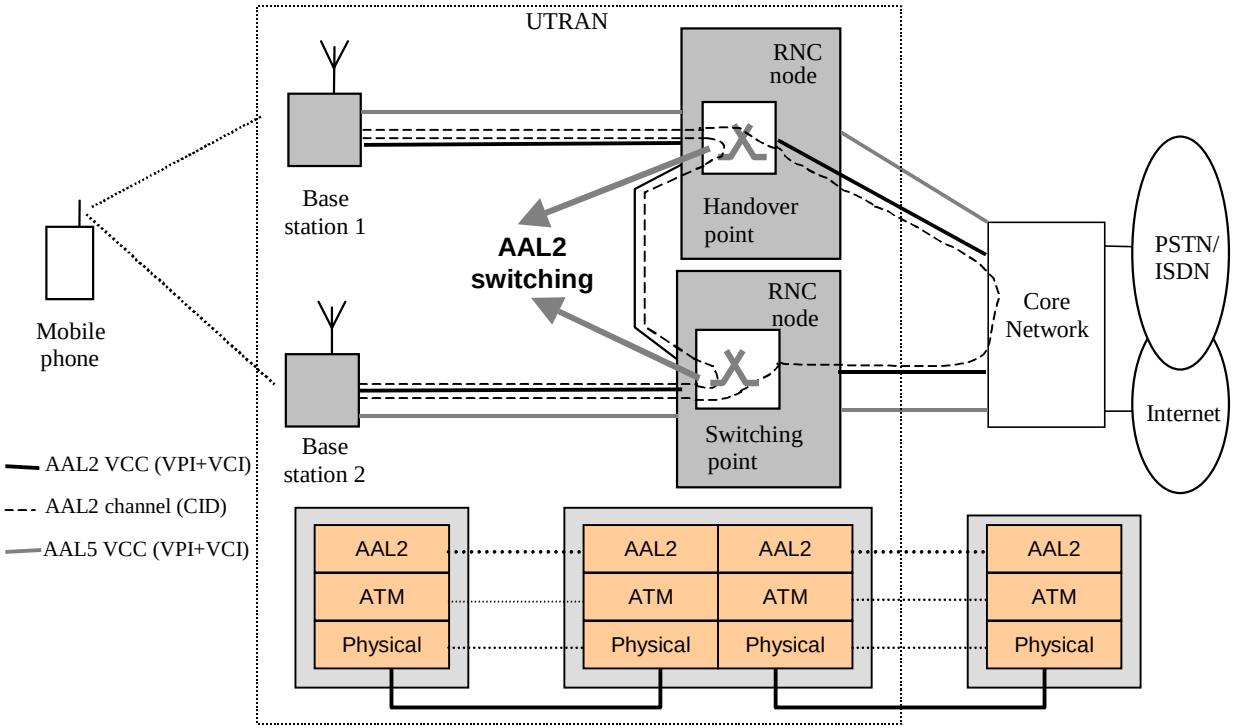


Figure 3 illustrates a simplified UMTS terrestrial access network (UTRAN) that uses both trunking and switching of AAL-2. Handover is done efficiently with AAL-2 switching.

Figure 3 AAL-2 for Narrowband Services in UTRAN



The **aal2Switch** application provides ATM and AAL-2 protocol functions with switching at both ATM layer and AAL-2 CPS. It also forwards OAM and AAL-5 PDUs from ATM ports to the Host (host processor) and vice-versa. Following are the features of the ATM/AAL-2 application:

- Two OC-3c ports
- ATM layer functions
- Cell Switching based on VPI and VCI

- ATM QOS — Subset of ATM Traffic Management 4.1 and includes CBR, rt-VBR.1, nrt-VBR.1 and UBR classes, traffic conformance (policing and shaping) and usage parameter control
- Up to 2048 VCs per port of which 1536 could be AAL-2 VCs
- AAL-2 CPS functions — Packing/multiplexing and Unpacking/de-multiplexing as per ITU I.363.2
- CU (Combined Use) Timer values from 2-10 ms (with 2 ms increments)
- 32K CIDs (16K CIDs per port and up to 250 CIDs per VC)
- AAL-2 CPS packet switching based on CID - 2.8 million pps (4 packets/cell and 1.4 million packets/port)
- Host interface for Control/Management plane functions (for AAL-5 and OAM Cells, Signaling/Control Messages)

These standards are applicable to the **aal2Switch** application:

- BICI 1.1ATM Forum — *B-ICI Specification Document (Version 1.1)*, September 1994.
- UNI 3.1 ATM Forum — *UNI Specification Document (Version 3.1)*, August 1993.
- I.362.2 ITU-T — *B-ISDN ATM Adaptation Layer Type 2 Specification*
- AF-TM-0121.000 ATM Forum — *Traffic Management Specification (Version 4.1)*, March 1999
- AF-VTOA-0113.000 ATM Forum — *ATM Trunking using AAL-2 for Narrowband Services*, February 1999
- 3G TS 25.4013GPP — *UTRAN Overall Description, v3.3.0*, June 2000, Technical Specification Group Radio Access Network
- RFC 2684 IETF — *ATM Adaptation Layer 5*, September 1999.

I.363.2 conformance

ATM/AAL-2 application supports following AAL-2 CPS features/functionality as specified in I.363.2:

- General Framework and Services
- Primitives to SSCS entities through CPS Packet descriptors
- Format and coding of AAL type 2 Common Part Sublayer (CPS):
  - Format and coding of the CPS-Packet — One to 45/64 bytes of payload and three bytes of header which consists of 1 byte Channel Identifier (CID), 6 bit Length Indicator (LI), 5 bit User-to-User Indication (UUI) and 5 bit Header Error Control (HEC)
  - Format and coding of the CPS-PDU — CPS-PDU payload of one or more (complete or partial) CPS-Packets and CPS-PDU start field (STF) which consists of 6 bit Offset Field (OSF), 1 bit (modulo 2) Sequence Number (SN) and 1 bit of Parity (P)
- AAL-2 Type 2 CPS Receiver functions which includes STF and HEC verification and unpacking of CPS packets
- AAL-2 Type 2 CPS Transmitter functions:
  - Multiplexing and packing of equal length CPS-Packets
  - Multiplexing and packing of different length CPS-Packets
  - Multiplexing and packing of maximum length CPS-Packets
  - Combined Use Timer (Timer_CU) of 2-10 ms (2 ms granularity)

AAL-2 CPS features/functionality that are not supported include:

- Layer Management and Control Plane (transparently passes the CPS packets received with CID values from 1 to 7, to host)
- Point-to-Mutlipoint

cation Components Used

The CST provides a number of application components that are used across applications. This application uses the following application components provided in the CST:

- **phy** (OC-3 bit micro-code)
- **queueUtils**
- **sonet**
- **qos**

See the documentation in the **apps/components/<componentName>/doc** *directory for the documentation on the software components that this application uses.*

lication Control and
ı Flow

Figure 4 shows AAL-2 data flow from one OC-3c port to the other OC-3c port.

Figure 4 AAL-2 Data Flow From OC-3c to OC-3c Port

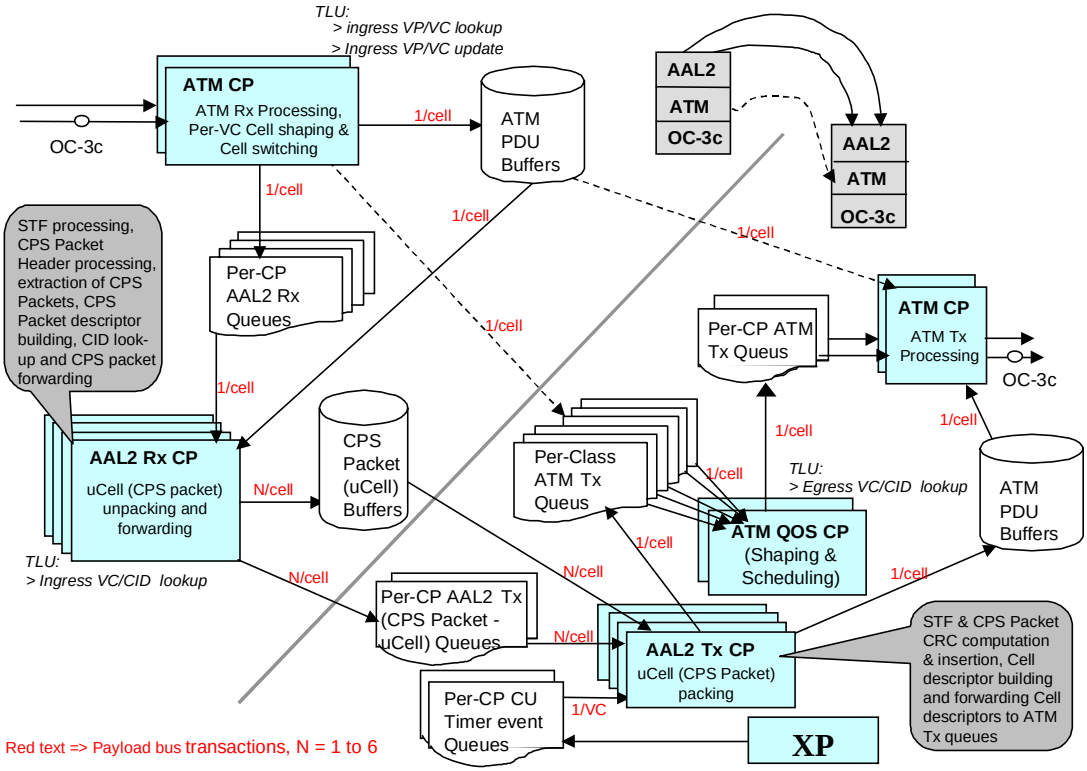
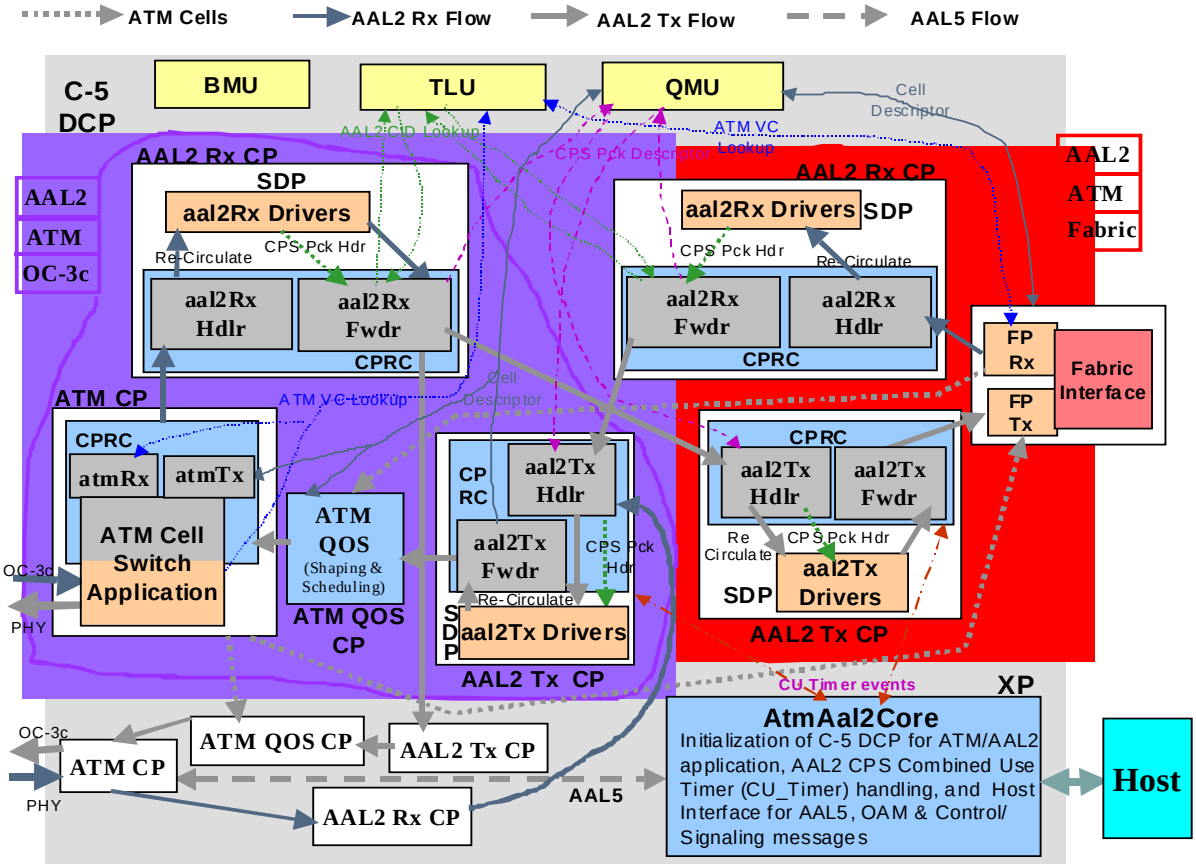


Figure 5 shows the data flow through the C-5 NP in more detail.

Figure 5 Architecture of aal2Switch Application



ɔurce Utilization

To support this application's features, the processors within the C-5 are performing a variety of tasks. The sections below enumerate what functionality is taking place and how the different processors are being used.

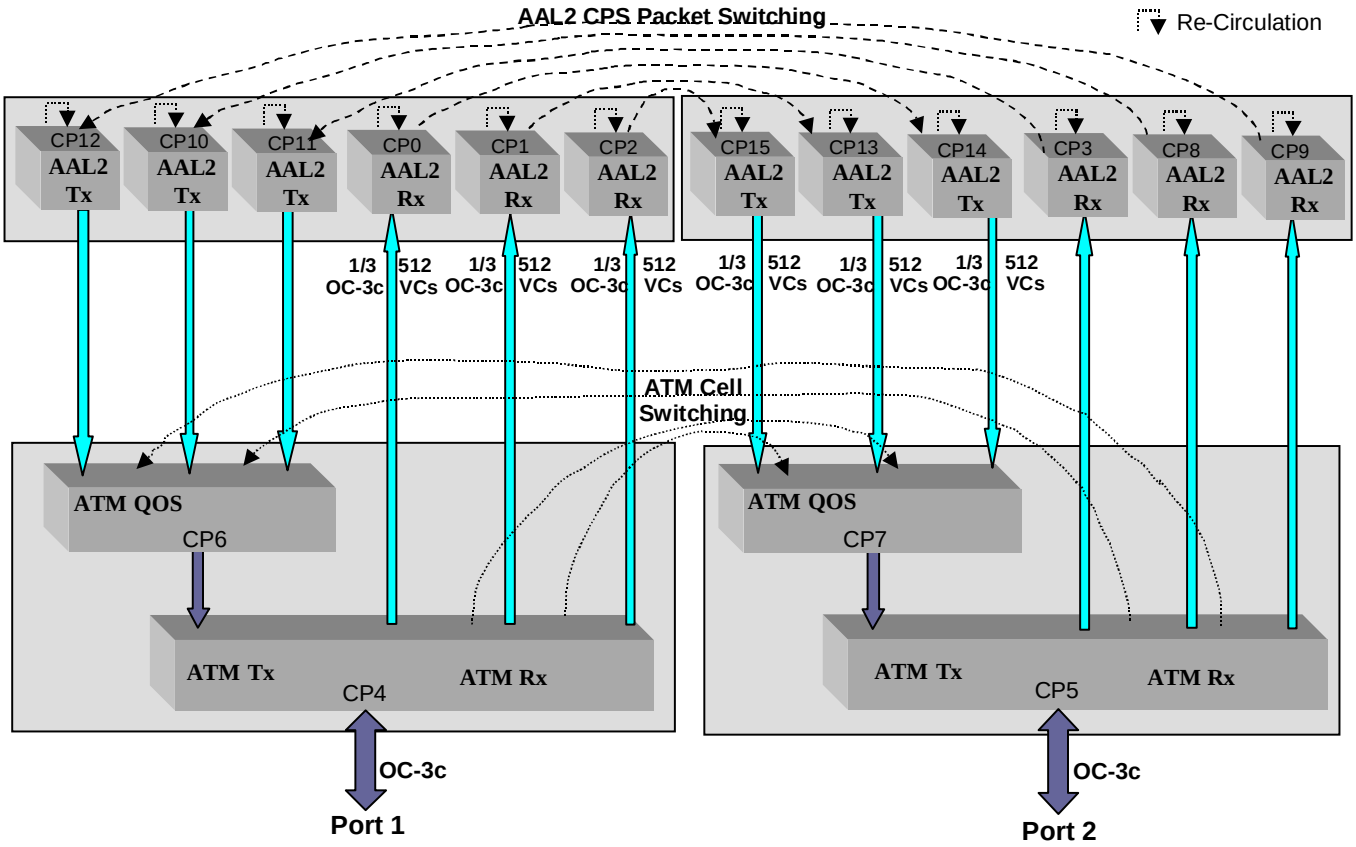
The **aal2Switch** application uses multiple CPs for ATM and AAL-2 processing. Figure 6 on page 22 shows the function partitioning of ATM/AAL-2 application. For each OC-3c port, one CP is used for ATM processing, one CP is used for ATM QOS, 3 CPs are used for AAL-2 Rx processing and 3 CPs are used for AAL-2 Tx processing.

In case of fabric, all ATM functions are not required, and the FP is used for transmitting cells to Fabric after inserting cell header, and extracting header and payload from the received cells and forwarding them based table lookup.

The **aal2Switch** application consists of three main components:

- ATM/AAL-2 Core
  - Initialization of C-5 NP for ATM/AAL-2 application
  - AAL-2 CPS Combined Use Timer (CU_Timer) handling
  - Host Interface for AAL-5, OAM and Control/Signaling messages
- ATM
  - ATM Receive Processing — HEC Verification, Cell Delineation and Cell Switching
  - ATM Transmit Processing — Cell Header and HEC generation, and Cell transmission
  - ATM QOS - CBR, rt-VBR.1, nrt-VBR.1 and UBR classes, traffic conformance (policing and shaping) and usage parameter control
- AAL-2
  - AAL-2 CPS Receive Processing — STF Checking, CPS Packet HEC verification, and CPS Packet Extraction and Switching
  - AAL-2 CPS Transmit Processing — CPS Packet Header and HEC generation, STF Generation and packing of CPS packets

Figure 6 Function Partitioning for the ATM/AAL-2 Application



XPRC The XP is used for initializing C-5 NP for ATM/AAL-2 application and includes initializing all the CPs, FP, TLU, QMU and BMU, and setting up Switching tables. It also handles Timer_CU for AAL-2 packing and provides host interface for AAL-5 and OAM Cells and Control/Signaling messages.

Initialization of C-5 NP for ATM/AAL-2 Application includes:

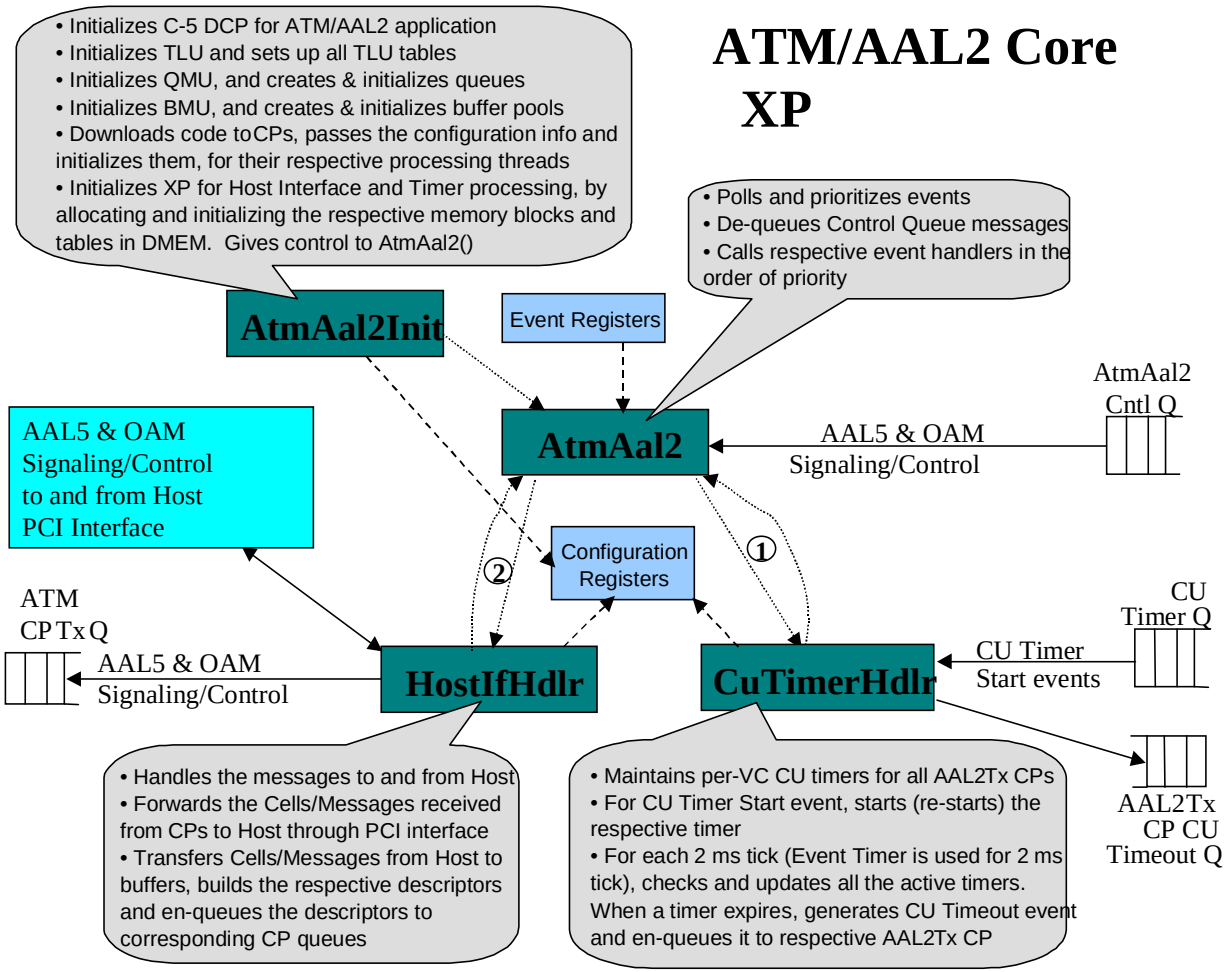
- Initialization of system services
- Queue Creation and Configuration
  - 2 for XP (AtmAal2 Cntl Q and CU Timer queue)
  - 1 for each ATM CP (ATM SDU queue)
  - 1 for each AAL-2 Rx CP (AAL2 Rx queue)
  - 2 for each AAL-2 Tx CP (AAL2 Tx queue and CU Timeout queue)
  - 196 for each ATM QOS CP
- Buffer Pool Creation and Configuration
  - 1 pool of 4096 buffers (each of size 64 bytes) for each ATM CP
  - 1 pool of 2048 buffers (each of size 64 bytes) for each AAL-2 Rx CP
  - 1 pool of 2048 buffers (each of size 64 bytes) for each AAL-2 Tx CP
  - 1 pool of 128 buffers (each of size 64 bytes) for XP
- Tables Setup
  - ATM Switching Tables (1 per ATM port/CP) for 2048 VPI and VCI combinations — Hash, Trie and Key Tables. Each Key entry is initialized with 28 bit VPI and VCI key, QOS and Traffic parameters, queue Id, and VC index of egress port. In case of AAL-2 VCs, queue Id is the Id of respective AAL-2 Rx queue and VC index corresponds to Ingress port.
  - CPS Packet Switching Tables (1 per VC and 512 per AAL-2 Rx CP) — Each table is initialized for 255 entries (one for each CID value 1 to 255). Each entry is initialized with queue Id of egress AAL-2 Tx CP, egress CID and VC index of egress port.

  - For AAL-2 VCs, VC indices from 0 to 1535 are used and ATM Switching Tables are setup such that each AAL-2 Rx CP handles 512 VCs in contiguous range (0 to 511, 512 to 1023, and 1024 to 1535).

- CP configuration and initialization
  - SDP configuration of ATM CPs for OC-3c interface
  - SDP configuration of AAL-2 Rx and Tx CPs for re-circulation
  - Package loading for CPs — CP0-CP3 for ATM and QOS processing, CP4-CP9 for AAL-2 Rx processing, and CP10-CP15 for AAL-2 Tx processing
  - Initialization descriptor building with respective configuration parameters (Buffer Pool Ids, Table Ids, etc.) for CPs
  - Passing initialization descriptors to CPs and enabling them
- Initialization for Host Interface and Timer Handling
  - Initialization for 2 ms timer tick
  - Allocation and initialization of data structures

Figure 7 shows the details of the ATM/AAL-2 Core.

Figure 7 ATM/AAL-2 Core - XP Architecture



CP Different Channel Processors (CPs) are used for processing at each protocol layer. ATM CP handles the ATM layer functions and cell switching for OC-3c line.

Existing ATM Cell Switch Application will be used for ATM layer functions and will be enhanced for ATM/AAL-2 application. The received cells are either directly switched to egress port (forwarded to destination ATM QOS CP or FP) or forwarded to AAL-2 Rx CP in case of AAL-2, based on VPI and VCI table lookup. AAL-5 and OAM cells are passed to XP, which in turn are passed to host. At the egress side, ATM CP receives the cells from ATM QOS CP and transmits them to OC-3c line.

ATM TM CP handles the traffic management functions at egress. It receives cells from ingress ATM CP or FP (cell switching), AAL-2 Tx CPs and XP (AAL-5 and OAM). It shapes the cells for their traffic conformance, schedules them as per traffic classes and passes them to egress ATM CP for transmission.

The AAL-2 Rx CP handles the receive CPS processing for AAL-2 PDUs (STF checking, CPS Packet HEC validation and unpacking) and extracts CPS packets. It forwards the CPS packets to destination AAL-2 Tx CP based on CID.

The AAL-2 Tx CP handles the transmit CPS processing (STF and CPS packet HEC computation and insertion) and packs the CPS packets into ATM cells. The cells are then forwarded to ATM QOS CP.

AAL-2 CPS Combined Use Timer (CU Timer) Handling

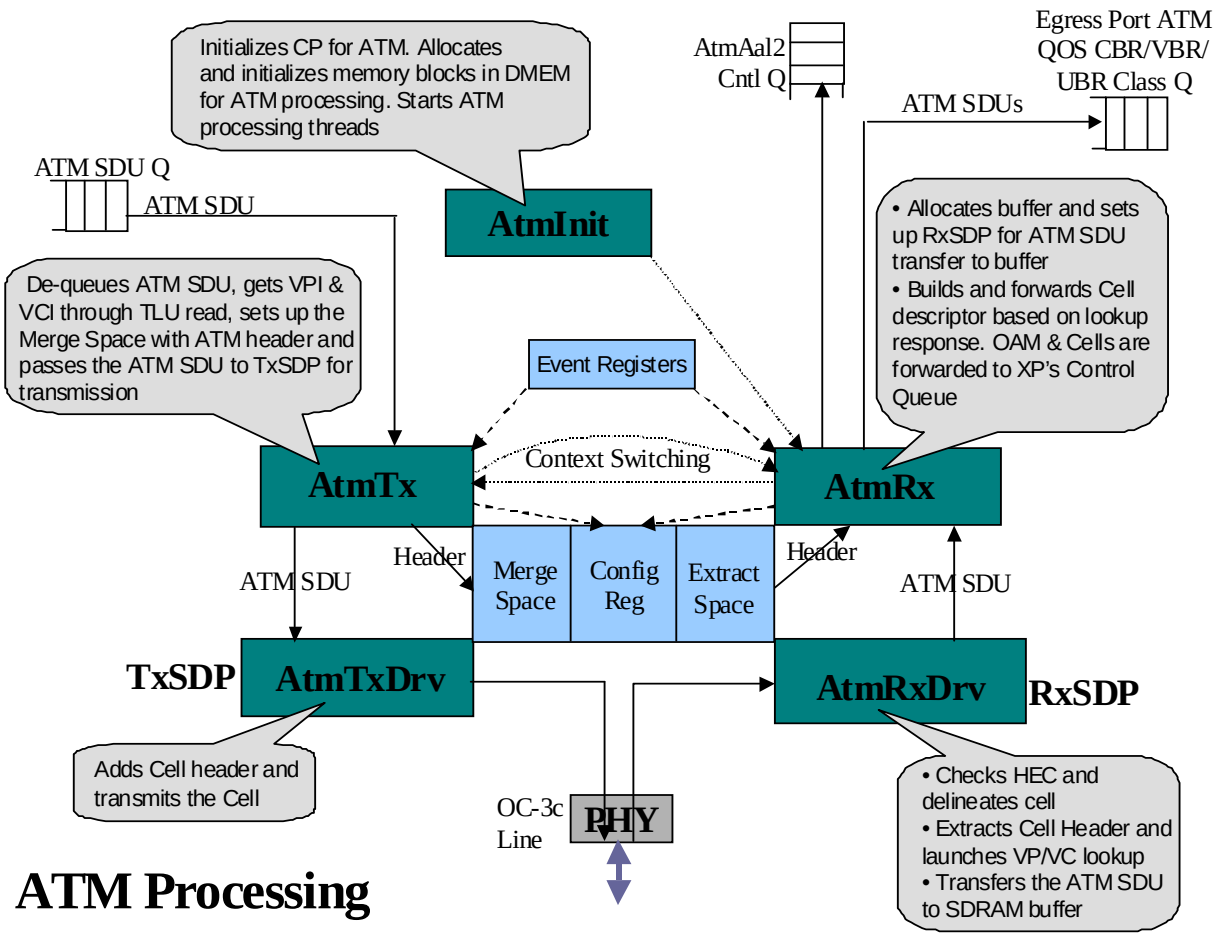
There are per VC timers for each AAL-2 Tx CP and they get started (re-started) on Timer Start events from AAL-2 Tx CPs. Each timer is updated every 2 ms and it is put into expired list when it expires. For each expired timer, a Timeout event is built with associated VC information and en-queued to the respective AAL-2 Tx queues. CU Timer Handling includes:

- Generation of 2 ms tick
- Updating timers for each 2 ms tick
- Starting (re-starting) timer for Timer Start event
- Generating timeout event on timer expiry

A 2 ms tick is generated using Countdown timer. Timers are updated one at a time after processing AtmAal2 Cntl queue and expired list (timer update processing continues when waiting for de-queue operation of AtmAal2 Cntl queue or en-queue operation of expired list).

Existing ATM Cell Switch application is modified/enhanced for ATM/AAL-2 application. Figure 8 below shows the ATM processing.

Figure 8 ATM Processing



ATM RX Processing

ATM Receive Processing is same as ATM Cell Switch application (see the *ATM Cell Switch Application Guide* document) except for table lookup. In existing ATM Cell Switch application, the lookup is based on simple VC index, which is computed using 4 bits of CP Id, 6 bits of VPI and 6 bits of VCI. In case of ATM/AAL-2 application, the lookup is based on exact match of received VPI and VCI. XP creates ATM Switching table for each port (ATM CP) which consists of hash, trie and VPI/VCI key tables, and passes the Table Ids to the ATM CPs.

ATM TX Processing

ATM Transmit Processing is same as ATM Cell Switch application (see the *ATM Cell Switch Application Guide* document) .

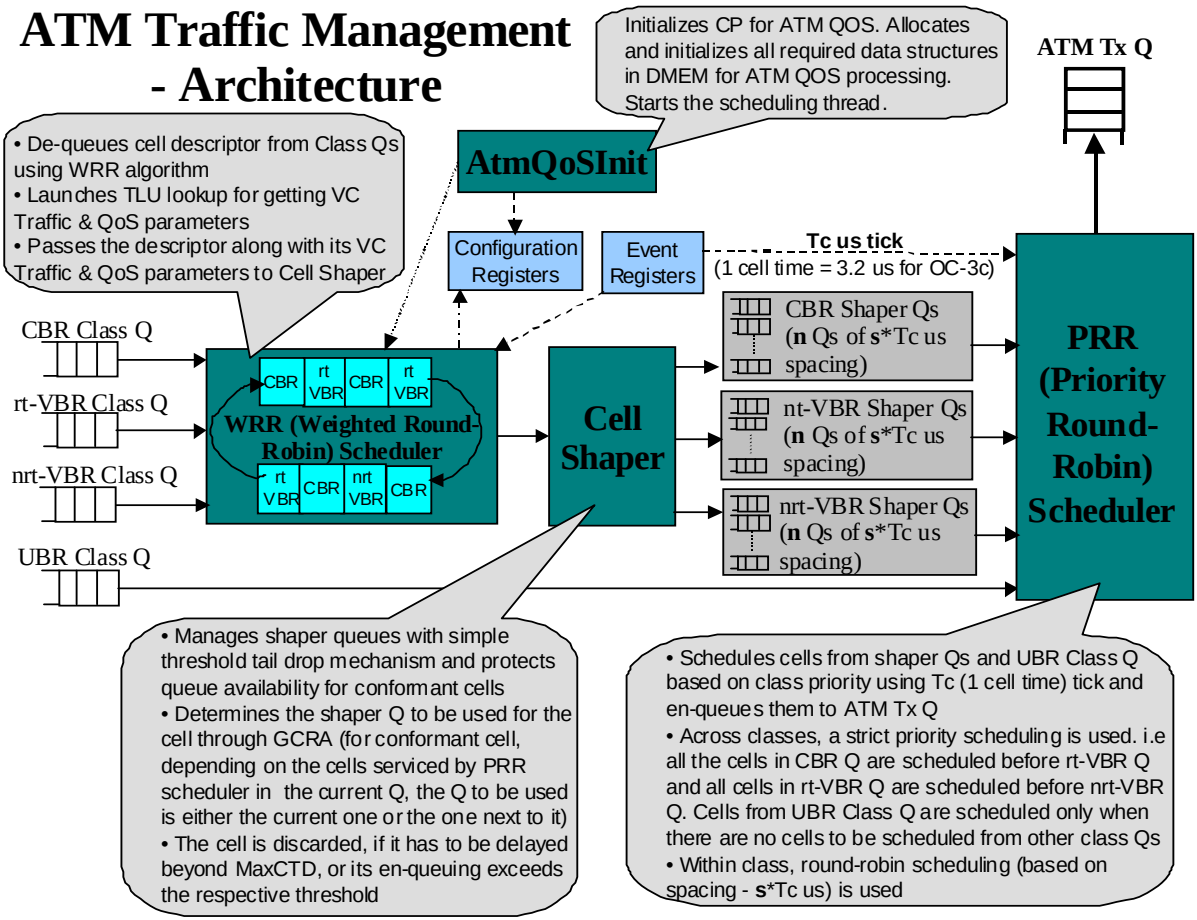
ATM QoS Processing

ATM QOS implementation for ATM/AAL-2 application includes sub-set of requirements/functionality specified in ATM Forum's *Traffic Management Specification - Version 4.1*. The features implemented are expected to address most of the real scenario QOS requirements of the products built for ATM/AAL-2 application. The requirements/functionality addressed are:

- ATM Service classes — CBR, rt-VBR.1, nrt-VBR.1 and UBR
- QoS Parameters — MaxCTD
- Traffic Parameters
  - PCR and CDVT for CBR
  - PCR, CDVT, SCR and MBS for rt-VBR and nrt-VBR
- Traffic Conformance — Policing and Shaping
  - CBR - GCRA(1/PCR, CDTV)
  - rt-VBR and nrt-VBR - GCRA(1/SCR, BT+CDTV), where BT = (MBS - 1) * (1/SCR - 1/PCR)
- Usage Parameter Control
  - PCR Enforcement
  - Cell Discarding

Figure 9 shows the Traffic Management architecture for ATM QOS.

Figure 9 ATM QoS



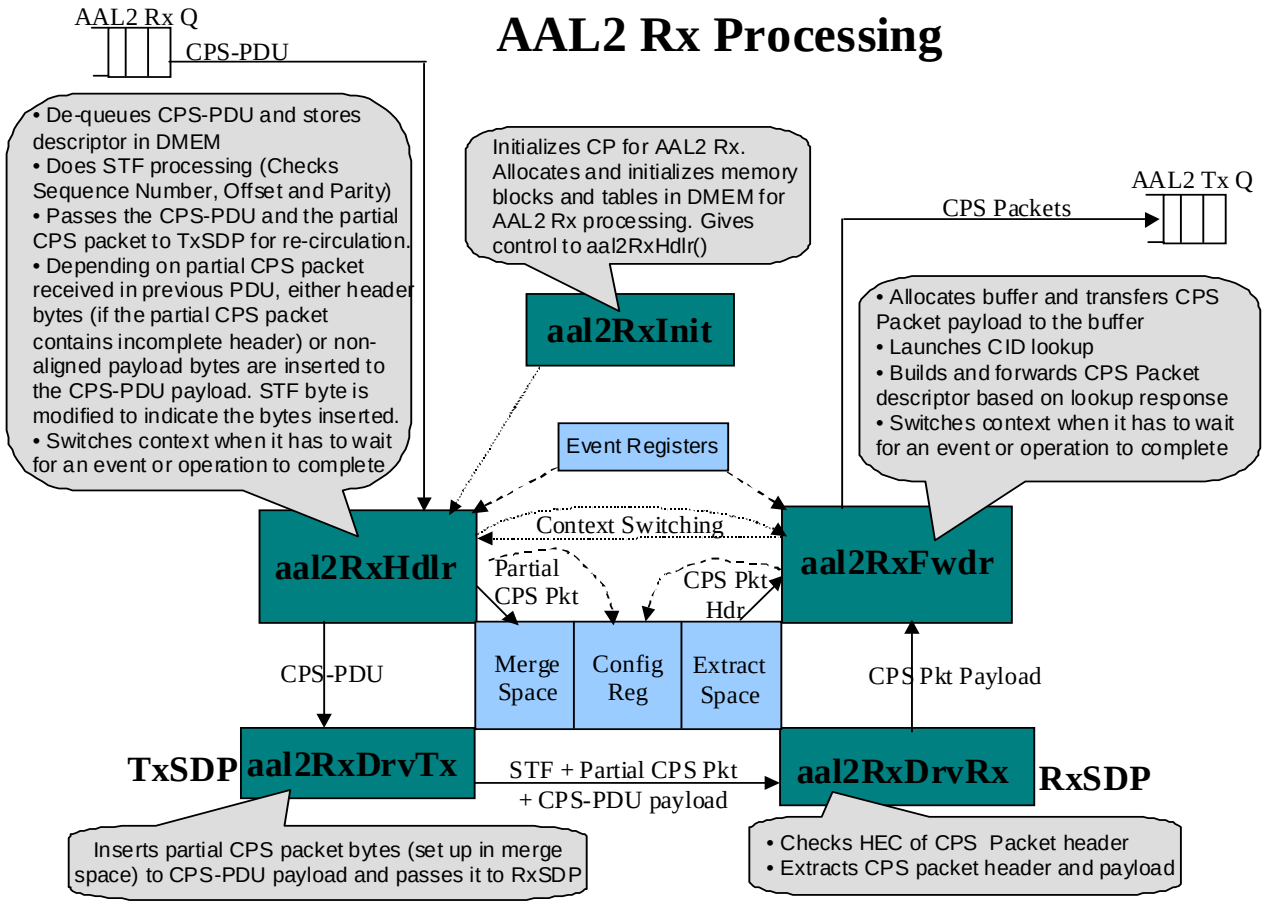
AAL-2 CPS Rx Processing

AAL-2 CPS Receive processing involves:

- Unpacking of CPS packets from CPS PDUs forwarded from ATM CP
- Forwarding CPS packets to egress AAL-2 Tx CPs based on CID lookup

Figure 10 below shows the AAL-2 receive processing and CPS packet forwarding.

Figure 10 AAL-2 Rx Processing



AAL-2 Rx CP handles unpacking of CPS packets for up to 512 VCs through a table maintained in DMEM. The CPS PDUs are de-queued from AAL-2 Rx Q and are re-circulated through SDP for extracting CPS packets.

AAL-2 Rx CP does pipeline processing by using both Data Scopes. At handler side (aal2RxHdlr and aal2RxDrvTx), up to two CPS PDUs (if they belong to different VCs) could be processed for re-circulation at any time.

At forwarder side (aal2RxFwdr and aal2RxDrvRx), up to four CPS packets could be unpacked and forwarded to AAL-2 Tx queues at any time. A forwarding table of size 4 is maintained at the forwarder side to store the information about the CPS packets that are being unpacked and forwarded.

If a CPS PDU belongs to a VC for which a previously de-queued CPS PDU is getting unpacked, the re-circulation is held till the unpacking is complete. The re-circulation is also held when there are four outstanding CPS packets to be forwarded (waiting for lookup response).

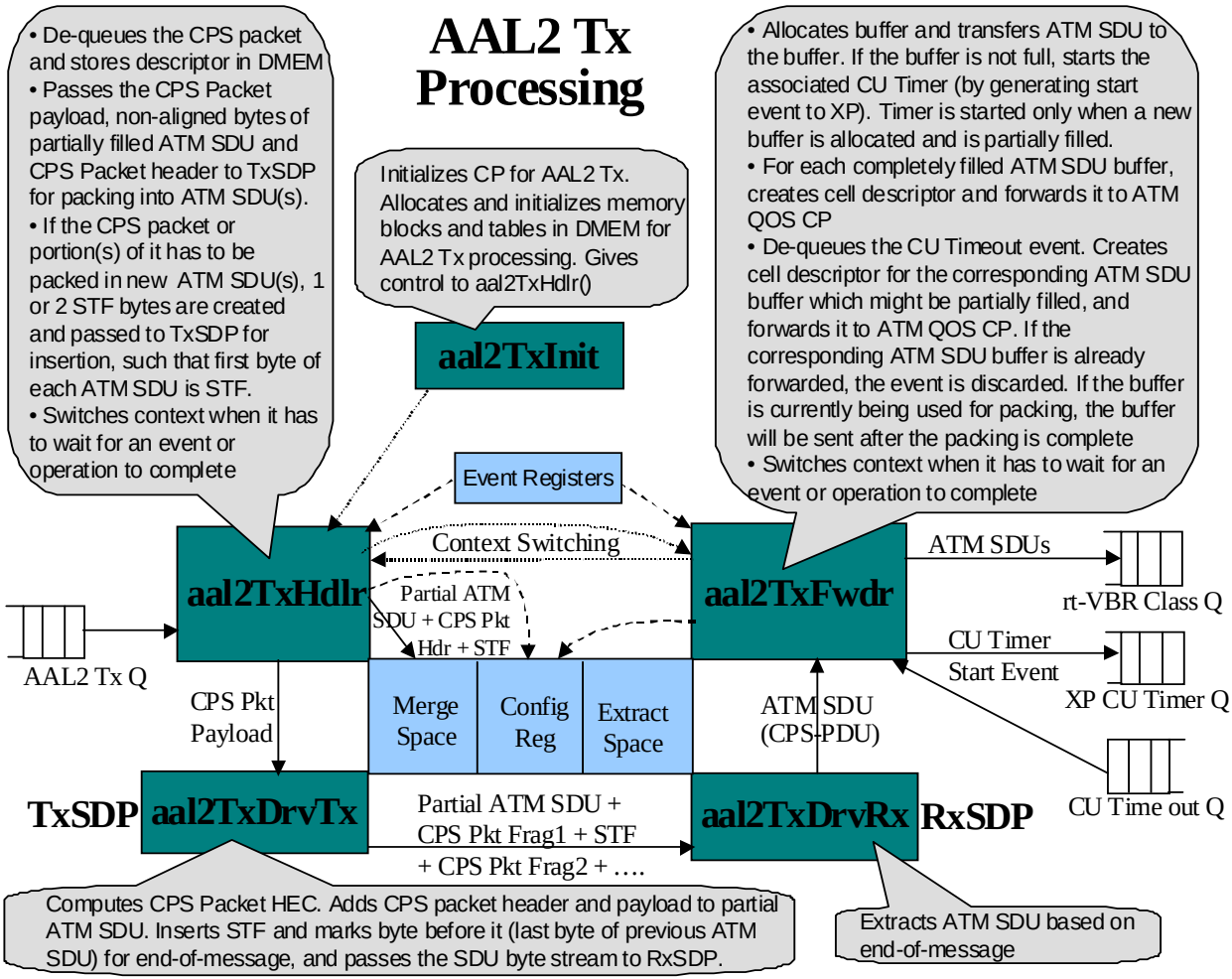
AAL-2 CPS Tx Processing

AAL-2 CPS Transmit processing involves:

- Packing of CPS packets into ATM SDUs
- Forwarding ATM SDUs to ATM QOS CP of egress OC-3c port

Figure 11 shows the AAL-2 transmit processing.

Figure 11 AAL2 Tx Processing



AAL-2 Tx CP handles packing of CPS packets for up to 512 VCs through a table maintained in DMEM. The CPS packets are de-queued from AAL-2 Tx queue and are re-circulated through SDP for packing into ATM SDUs.

AAL-2 Tx CP does pipeline processing by using both Data Scopes. Up to two CPS packets (if they belong to different VCs) could be processed for packing at any time. If a CPS packet belongs to a VC for which a previously de-queued CPS packet is getting packed, the re-circulation is held till the packing is complete.

Host Host Interface Handler gets called when there are AAL-5 and OAM cells and Signaling/Control messages to be passed between CPs and Host. Cells/Messages from CPs are passed host through PCI interface.

For cells/messages from host, corresponding descriptors are built and are enqueued to the respective CP queues after transferring the cells/messages to buffers.

d Application Files

Below is a list of the files that are a part of this application and a brief description of their contents.

XPRC

FILE NAME	LOCATION	DESCRIPTION
xpMain.h	_/chip/np/xprc/inc	Contains timer related definitions
xpMainInit.h	_/chip/np/xprc/inc	Contains definitions which specify the buffer and queue assignment to each of the processors.
aal2XpIf.h	_/chip/npxprc/inc	Contains the queue related definitions(Base queue for CP's , QOS queueu for variious class of traffic.
xpMain.c	_/chip/np/xprc/src	Main Program and entry point to the application
xpMainInit.c	_/chip/np/xprc/src	Main Initialization program and entry point to application
atmVccTableSetupXp.c	_/chip/np/xprc/src	Contains function to populate table used by ATM CP's.
aal2TableCreateXp.c	_/chip/np/xprc/src	Contains functions to create Lookup table used by AAL-2 CP's
aal2SwitchTablesXp.c	_/chip/np/xprc/src	Contains function which populates AAL-2 Switch table.

CPRC

FILE NAME	LOCATION	DESCRIPTION
aal2Init.h	_/chip/np/cprc/inc	Contains definitions used by AAL-2 Rx and Tx.
aal2Rx.h	_/chip/np/cprc/inc	Contains macros and definitions used by AAL-2 Rx
aal2RxIf.h	_/chip/np/cprc/inc	Contains protoype for AAL-2 Rx inititalisation function.
aal2Tx.h	_/chip/np/cprc/inc	Contains macros and definitions used by AAL-2 Tx.
aal2TxIf.h	_/chip/np/cprc/inc	Contains prototype for AAL-2 Tx initialization function.
atmIf.h	_/chip/np/cprc/inc	Contains declarations for alll he functions and global variables being used by ATM.
errorHandlling.h	_/chip/np/cprc/inc	Contains functions which return the status of an operation on queue's and buffer's.
systemServicesLocal.h	_/chip/np/cprc/inc	Contains some additional PDU services functions which enable writing to DMEM location from RxSDP and writing from DMEM to TxSDP.
aal2CpMain.c	_/chip/np/cprc/src	Contains AAL-2 main program
aal2RxCp.c	_/chip/np/cprc/src	Contains the master receive thread for AAL-2
aal2TxCp.c	_/chip/np/cprc/src	Contains the master transmit thread for AAL-2
atmInit.c	_/chip/np/cprc/src	Contains the atm initialization function.
atmOc3CpMain.c	_/chip/np/cprc/src	Contains the ATM main program.
atmOc3RxCp.c	_/chip/np/cprc/src	Contains the master receive thread for ATM.
atmOc3TxCp.c	_/chip/np/cprc/src	Contains the master transmit thread for ATM.
atmStats.c	_/chip/np/cprc/src	Contains the global variable for ATM statistics.
aal2Init.h	_/chip/np/cprc/inc	Contains definitions used by AAL-2 Rx and Tx.

SDP

FILE NAME	LOCATION	DESCRIPTION
aal2RxRxByte.c	_/chip/np/sdp/src	Contains the RxByte microcode for AAL-2 Rx CP.
aal2RxTxByte.c	_/chip/np/sdp/src	Contains the TxByte microcode for AAL-2 Rx CP.
aal2TxRxByte.c	_/chip/np/sdp/src	Contains the RxByte microcode for AAL-2 Tx CP.
aal2TxTxByte.c	_/chip/np/sdp/src	Contains the TxByte microcode for AAL-2 Tx CP.
atmRxByte.c	_/chip/np/sdp/src	Contains the ATM Rx microcode.
atmTxByte.c	_/chip/np/sdp/src	Contains the ATM Tx microcode.
atmRxSync.c	_/chip/np/sdp/src	Contains ATM RxSync microcode.

FDP

There are no files for the FDP in this application.

Host

There is no host application for this application.

Binaries

FILE NAME	LOCATION	DESCRIPTION
aal2Switch.dsc	_/run/	Package descriptor file for this application.
aal2Switch.pkg	_/run/bin/<VARIANT>/	Package file for this application.
aal2SwitchXp.dcp	_/run/bin/<VARIANT>/	XPRC main ELF file for this application.
aal2SwitchXp.map	_/run/bin/<VARIANT>/	XPRC main memory map for this application.
aal2SwitchXpInit.dcp	_/run/bin/<VARIANT>/	XPRC main Initialization ELF file for this application.
aal2SwitchXpInit.map	_/run/bin/<VARIANT>/	XPRC main Initalization memory map for this application.
aal2Cp.dcp	_/run/bin/<VARIANT>/	CPRC ELF file for AAL-2 portion of this application.
aal2Cp.map	_/run/bin/<VARIANT>/	CPRC memory map for AAL-2 portion of this application.
atmCp.dcp	_/run/bin/<VARIANT>/	CPRC ELF file for ATM portion of this application.
atmCp.map	_/run/bin/<VARIANT>/	CPRC memory map for the ATM portion of this application.
aal2RxUcode.sdp	_/run/bin/<VARIANT>/	SDP image for AAL-2 Rx side of this application.
aal2TxUcode.sdp	_/run/bin/<VARIANT>/	SDP image for the AAL-2 Tx side of htis application.
atmUcode.sdp	_/run/bin/<VARIANT>/	SDP image for ATM side of this application.

Simulation Files

FILE NAME	LOCATION	DESCRIPTION
config_1	_/run/	Software simulator configuration file used for this application.
sim.in	_/run/	Software simulator file used for this application.
acceptAal2Switch-cxe .expected	_/run/	Compare file C-5e/C-3e simulation.
acceptAal2Switch-c5 .expected	_/run/	Compare file for C-5 simulation.

Design Issues

This section describes some of the design issues that relate to the **aal2Switch** application.

ATM Traffic Management

Traffic Management Parameters

Per VC Traffic Management parameters that TLU Tables contain are:

- Increment (I) - "1/PCR" for CBR, and "1/SCR" for rt-VBR and nrt-VBR
- Limit (L) - "CDVT" for CBR, and "CDVT + (MBS-1)(1/SCR-1/PCR)" for rt-VBR and nrt-VBR
- Maximum Cell Transfer Delay (maxCTD)
- Theoretical Arrival Time (TAT)

Host processor will derive the values for parameters 'I' and 'L' from the respective traffic parameters during VC set-up time and will update the TLU table for I, L and maxCTD.

The granularity for the parameters I, L and maxCTD depends on size (s) and number (n) of CBR/rt-VBR and nrt-VBR shaper queues (the total number of all the queues is limited by available QMU queues). The shaper queues for CBR and rt-VBR classes are logically processed as one set (they are physically separate to protect CBR traffic from rt-VBR traffic bursts). This implementation will use 192 QMU queues, which are arranged as follows:

- 64 queues of size 64 for CBR and rt-VBR classes
- PCR/SCR granularity of 64 cells/sec (24kbps)
- maxCTD of 64*64*Tc (64*64*3.2 = 13.1 ms for OC-3c)
- 64 queues of size 4096 for nrt-VBR class

- PCR/SCR granularity of 4096 cells/sec
- maxCTD of 64*4096*Tc (64*4096*3.2 = 839 ms)

Queue Management

Since the queue lengths are limited, their availability needs to be protected for conforming cells of each of the classes - CBR,rt-VBR and nrt-VBR. Hence, the usage of queues needs to be controlled for each class as well as shaping of non-conforming cells (shaping should not affect conforming cells), through proper management mechanisms. For queue management, a simple threshold with trail drop mechanism is used.

- Queue Management for CBR and rt-VBR queues
  - CBR and rt-VBR queues are logically managed as one set (they are physically separate to protect VBR traffic from rt-VBR traffic bursts)
  - Queues size for each logical queues — 64
  - Queues thresholds for non-conforming cells and rt-VBR class
- Queue Management for nrt-VBR queues
  - Queue size for each queue — 4096
  - Queue threshold for non-conforming cells

Performance

ATM/AAL-2 Core

For CU timer and host interface processing, XP does three QMU operations/cell (1/port for dequeuing Timer Start event, 0.3/port for enqueuing Timeout event and 0.2/port for cell descriptors assuming 10% as AAL-5 and OAM Cells and Control/Signaling messages), 0.4 BMU operations (0.2/port for cell payloads). Hence there will a total of 3.4 payload bus transactions/cell. There will be one TLU operation/cell for statistics read and update.

ATM Processing

For ATM Rx processing there will be:

- One QMU operation/cell (for en-queuing cell descriptor).
- One BMU operation/cell (for transferring cell payload to SDRAM)

Hence, there is a total of two payload bus transactions/cell.

There will be one TLU operation/cell (28 bit VPI-VCI hash lookup).

For ATM Tx processing, there will be:

- One QMU operation/cell (for de-queuing cell descriptor)
- One BMU operation/cell (for getting cell payload from SDRAM).

Hence, there is a total of two payload bus transactions/cell.

There will be a total of one TLU operation/cell (for getting VPI and VCI), two QMU operations and two BMU operations. The TLU operation and four payload bus transactions should complete within 545 cycles.

For ATM QOS processing, there will be three QMU operations/cell (that is, 1.5 for en-queuing and 1.5 for de-queuing cell descriptor) and hence three payload bus transactions/cell. There will be four TLU operations/cell (that is, three for getting QOS and Traffic parameters and one for update). Three QMU operations, four TLU operations and three payload bus transactions should complete within 545 cycles.

AAL-2 Receive Processing

Since each AAL-2 Rx CP handles 1/3 of OC-3c traffic, the maximum time a CPS PDU can wait in AAL-2 Rx Q before it gets de-queued for processing is 1635 clock cycles (that is, 3 * 545 where 545 is the mean cycles between 2 cells).

At Handler side, there will be one QMU operation/cell (for de-queuing cell descriptor), two BMU operations/cell (that is, one for cell payload and one for partial CPS packet payload) and hence a total of three payload bus transactions/cell.

At Forwarder side, there will be four QMU operations/cell (for en-queuing packet descriptors), four BMU operations/cell (for transferring packet payloads to SDRAM) and hence a total of eight payload bus transactions/cell. There will be an average of four TLU operations/cell (average of four CID lookups with peak of 12). Five QMU operations, six BMU operations, four TLU operations and 11 payload bus transactions should complete within 1635 cycles.

AAL-2 Transmit Processing

Each AAL-2 Tx CP handles 1/3 of OC-3c traffic. Hence the maximum time a CPS packet can wait in AAL-2 Tx Q before it gets de-queued for processing is 408 (that is, 3 * 545/4, assuming an average of four packets/cell) clock cycles.

At Handler side, there will be one QMU operation/packet (for de-queuing packet descriptor), two BMU operations/packet (that is, one for packet payload and one for partial cell payload) and hence a total of three payload bus transactions per packet.

At Forwarder side, there will be one BMU operation/packet (for transferring packet to ATM SDU in SDRAM), 2.3 QMU operations/cell (that is, one for cell descriptor, one for Timer Start event, and 0.3 for Timeout event) and hence a total of 1.6 (1 + 2.3/4) payload bus transactions per packet. 1.6 QMU operations, three BMU operations, 0.2 TLU operation, and 4.6 payload bus transactions should complete within 408 cycles.