Protect Your Cloud Onboarding with the Latest LPC54S0xx Microcontroller

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MICR Systems & Applications Engineering

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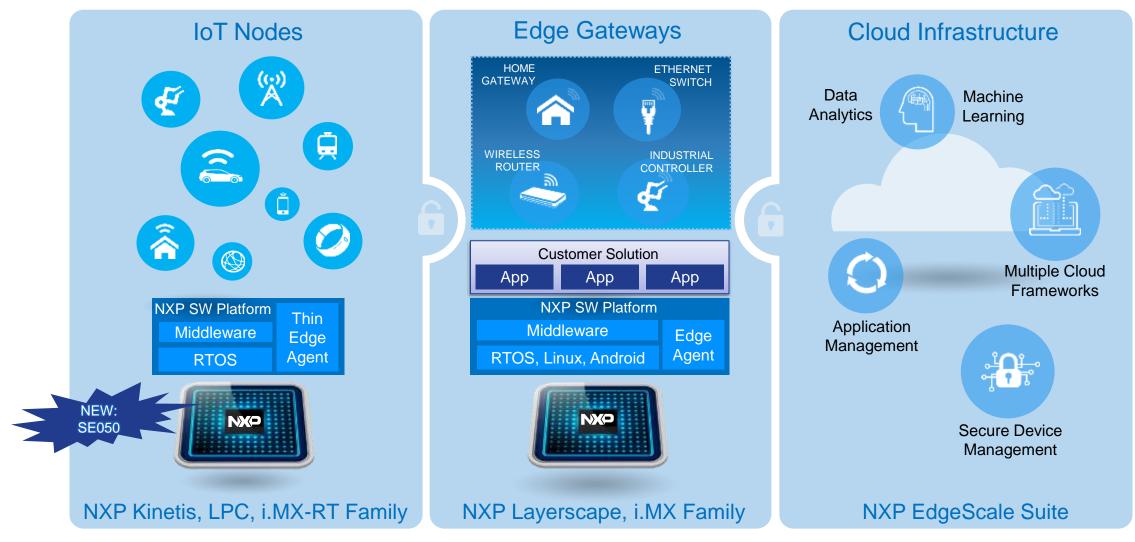


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Agenda

- Relevance of IoT Security
- IoT Security: Threats, Principles and Lifetime
- AWS at a Glance
- LPC54S0xx: Protecting Cloud
 On-boarding
- Q & A

NXP Solutions for Edge Computing









Consumer IoT Device Attack Trends

Attack method	Profitability	Comment	Trend
DDoS attacks	+	Still growing in size - simple	
Spam attacks		Not the easiest way to spam	+
Cryptocurrency mining		Depends on the coin price	•
Ransomware/locker	+	Might work on some devices	1
Blackmail/extortion	•	Does not scale well – depends	
Pranks/nuisance	••	Not done by cyber criminals	-
Information stealing	•	Done because it's simple	1
Click fraud	+	Often overlooked - profitable	
Premium services	+	Difficult to conduct	ŧ
Sniffing network traffic		Difficult with SSL/TLS	ŧ
Pivoting/attacking LAN	+	Infecting attached computers	1
Proxy	•	Not very lucrative, but useful	•

https://www.rsaconference.com/writable/presentations/file _upload/sem-m03d-profiting-from-hacked-iot-devicescoin-mining-ransomware-something-else.pdf

- Profitability motivates the IoT attacker
- DDoS attacks are enabled by dark web store fronts
- As the value of devices and the data they handle increases, Ransomware or device lock out attacks will rise
- IoT devices with weak cybersecurity allow attackers entry into protected networks



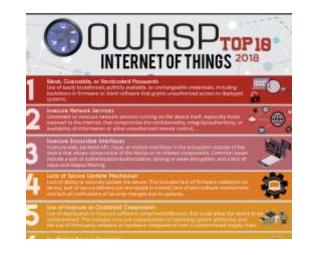
Legislation

Government is noticing/acting...



https://www.youtube.com/watch?v=YxC1kcZDMyc& feature=youtu.be

- Convergence on IoT security guidelines from many angles (foreign and domestic)
- OWASP (Open Web Application Security Project has a nice <u>list</u>

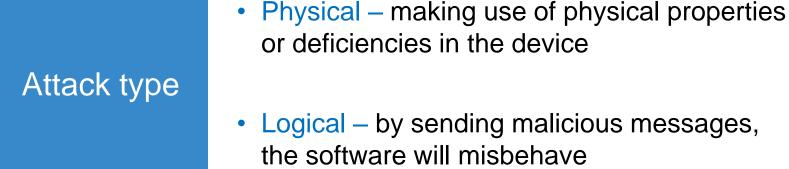








Attacks Occur in Many Forms: Different Types and Locations



Adversary's location

- Local adversary must be in the proximity of the device
- Remote adversary can be anywhere



IoT Security Threats and General Protection Principles

Threat Spectrum

3 Physical Logical Physical Logical If an attacker can get local If an attacker can get local All local interfaces: access to the device, make a access to the device, aim to Exploiting JTAG Power analysis cost/benefit trade-off and protect protect against local logical Light attacks - Serial Local against relevant local physical attacks. Reason: can be – USB Glitching • attacks over the lifetime of the automated and executed by — ... device laymen 1 Buffer overflow Aim to protect against remote attacks. Rowhammer Heartbleed Reason: scalable attacks can be automated and executed by Remote **Cache Timing** Flooding/DoS • laymen from anywhere in the world

Level of importance to ensure security against threats

High

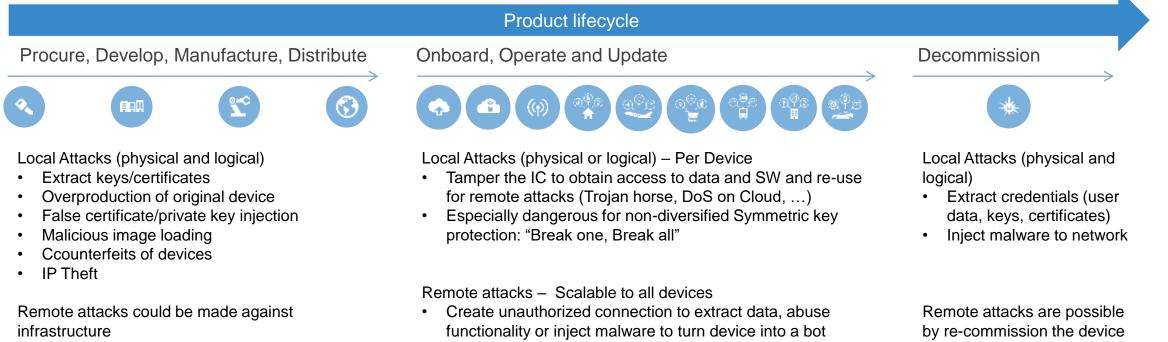
Higher

Highest

Solution Rationale Against Threats



A Connected/smart Device is Vulnerable Throughout its Lifecycle



Perform malicious software update to do the same

to attack the network or cloud



Derived Features for IoT Devices

Secure system lifecycle	System is able to securely go through its different life stages, including: Power-up / Boot phase, debug, OTA updates of FW and SW and decommissioning
Crypto & Key protection	A device must provide means for protected secure root key provisioning and storage of key and certificate credentials, and handle the security of derived keys.
Resource isolation (HW and SW)	Minimize the attack surface by isolating HW (like memory and processing) and SW resources used for platform security features from other parts of the IoT system
Run time integrity and attestation	The run-time integrity of a system is ensured and can be (remotely) validated – This validation is (remote) attestation







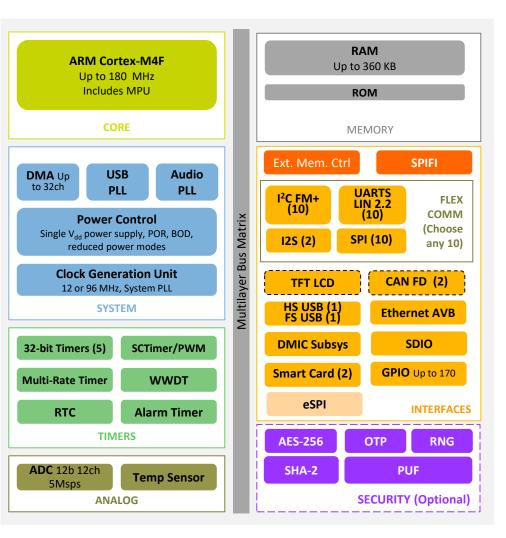
LPC54Sxx Block Diagram

High performance with high-end Graphical User Interface and security

- Cortex-M4F, 180MHz
 - Up to 360 KB RAM
 - 16KB EEPROM
 - XIP from QSPI via SPIFI
 - External Memory Ctrl (up to 32 bits)

Key Features

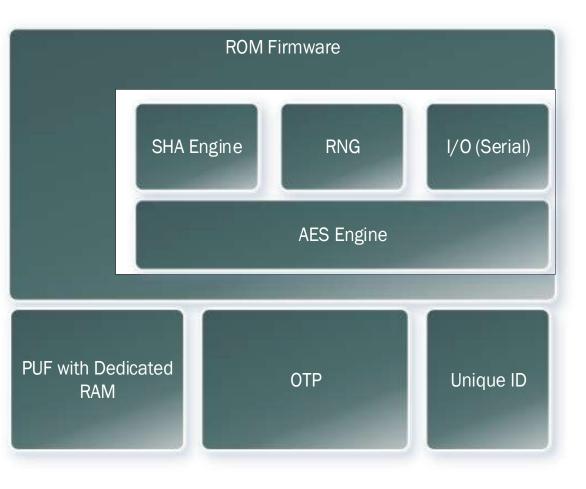
- Graphic LCD with resolutions up to 1024 x 768
- CAN-FD controller x2 (LPC54608)
- eSPI interface (slave and LPC bus device functionality)
- Digital mic subsystem supporting voice detection
- Hi-Speed and Full Speed USB
 - USB: 1x HS (H/D) w/on-chip HS PHY
 - XTAL-less FS USB Dev
- FlexComm: flexible serial connectivity
- Advanced Security Option:
 - AES-256, SHA-2, True RNG
 - PUF for key storage
 - HW diversified OTP Key Storage
 - Secure boot using 2048-bit RSA authentication and SHA-2 verification
 - Encrypted boot using AES-GCM mode





LPC54Sxx Security Sub-system

- ROM supporting secure boot methods
 - Authentication, Encryption, combination options
- AES Engine
 - Supports 128, 192 or 256 bit keys
 - Encryption modes: Electronic Codebook (ECB), Cipher Block Chaining (CBC), Cipher Feedback (CFB), Output Feedback (OFB), Counter (CTR), Galois Counter Mode (GCM)
- SHA Engine
 - Support SHA1 (160 bit) and SHA2 (256 bit)
- Physically Unclonable Function (PUF)
 - Device unique root key (256 bit strength)
 - Can store key sizes 64 bit to 4096 bit
 - Index 0 Keys routed to AES engine via direct HW bus
- 128-bit UUID per device
 - RFC4122 compliant
- Random Number Generator (RNG)
 - FIPS 140-1 compliant
- HW diversified OTP key
 - Key stored in OTP is scrambled using device unique ID







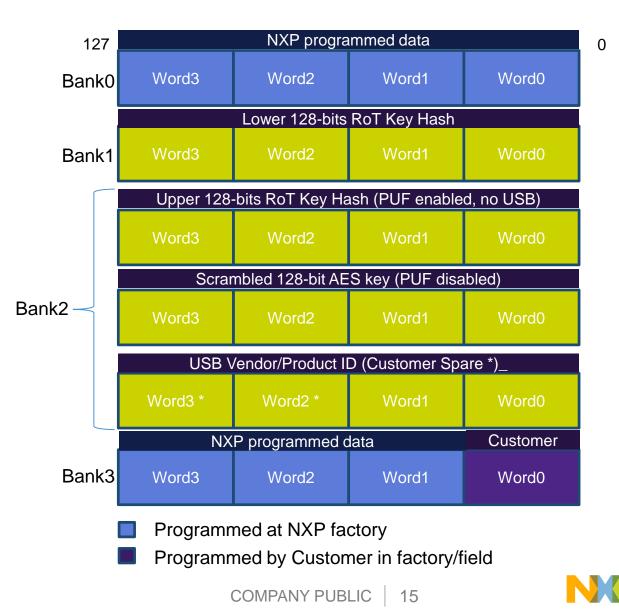


NP

OTP Layout – LPC54S0xx

OTP provides tamper proof storage for key material and boot control

- OTP is organized as four 128-bit banks
- Each 32-bit word can be read/write lockable
- Bank 1 (either):
 - Lower 128 bits of RoT key hash
 - Customer data (encrypt only)
- Bank 2 (either):
 - Upper 128 bits of RoT key hash
 - Scrambled 128-bit AES key (PUF disabled)
 - USB vendor/product IDs
 - Customer data (encrypt only, PUF enabled)
- Bank 3 word 0 of controls secure boot behavior along with key revocation list







SRAM PUF Technology

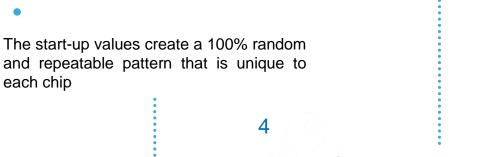
Process Variation

Naturally occurring variations in the attributes of transistors when chips are fabricated (length, width, thickness)

2

SRAM Start-up Values

Each time an SRAM block powers on the cells come up as either a 1 or a 0



Silicon Fingerprint

SRAM PUF Key (KPUF)

The silicon fingerprint is turned into a secret key that builds the foundation of a security subsystem

.

SRAM PUF Benefits

Device-unique, non-reproducible ٠ fingerprint

Leverages entropy of mfg. process

each chip

3

No key material ٠ programmed



SRAM PUF Advantages





SRAM PUF Technology

- Key generated by device entropy
- No traces of sensitive data

Other Solutions

- Key programmed externally
- Permanent physical alteration
- Key visible in structure

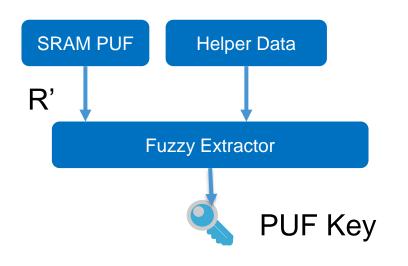


Key Provisioning Based on SRAM PUF

1. Enrollment Mode



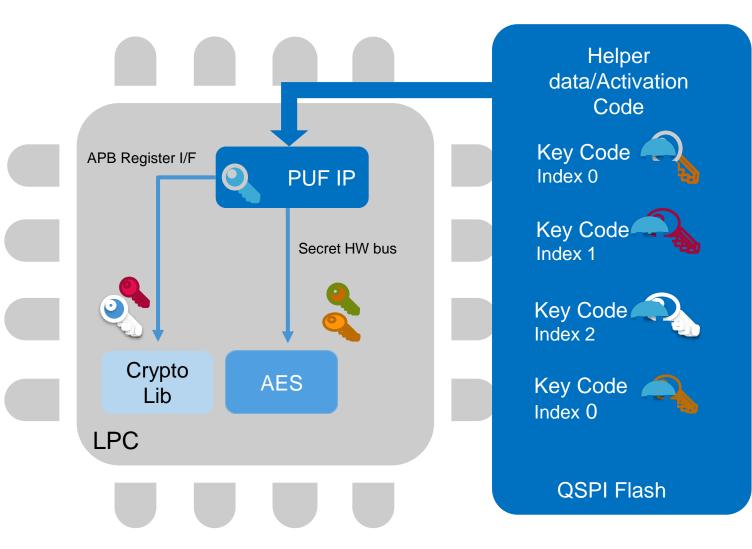
2. Key Reconstruction Mode



- SRAM PUF response (R) is a noisy fingerprint of the chip
- PUF IP implements the Fuzzy Extractor or Helper Data Algorithm
 - Error correction
 - Privacy Amplification
- Two operation modes:
 - Enrollment mode
 - Key Reconstruction Mode



PUF Key Store



LPC PUF Features

- 256 bit strength Root key
- Supports wrapping of keys
 - 64 to 4096 bits keys
 - Generation of Intrinsic keys (random key)
 - Index 0 accessible through HW secret bus
 - Other indexes through register I/F

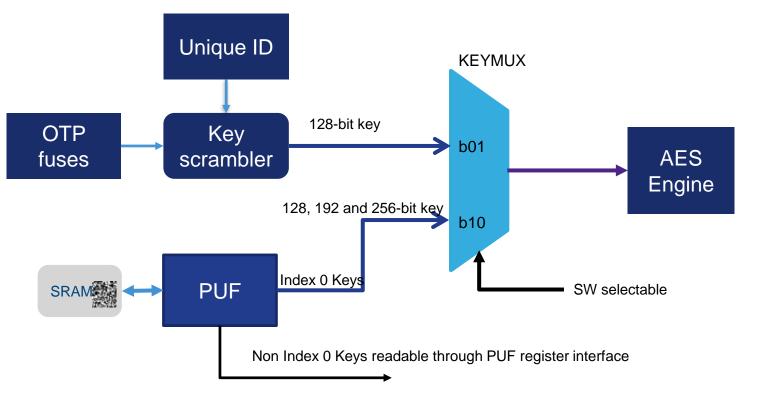






Key Management – HW AES Key Paths

- Critical keys feed directly to AES engine via HW bus
- No access to secret keys (Index 0) via SW readable registers
 - Except during provisioning
- PUF derives unique root key (KPUF) per device from SRAM fingerprint
 - Eliminates complexity of generating unique keys per device during provisioning
 - Protects credentials on a per device basis







COMPANY PUBLIC 23

LPC54Sxx Secure Boot ROM Features

- Support following secure boot mode
 - Authentication only image: Public Key signed image
 - Encrypted image: Symmetric key encrypted image with and MAC authentication
 - Enhanced secure image: Symmetric key encrypted image with Public Key authentication
- Support Public Keys & Image Revocation
- Support redundant boot image on external SPI flash



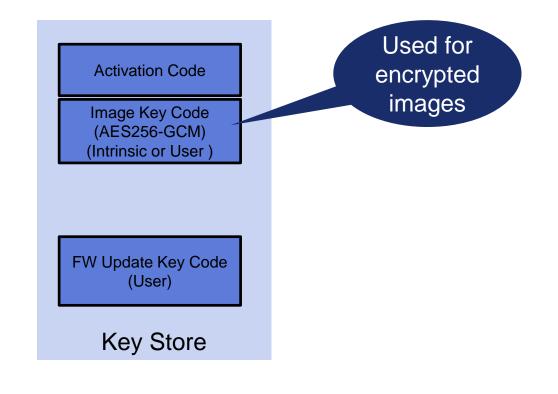
Secure Boot ROM – Option Details

- Secure Boot
 - Authentication only images:
 - RSA signature verification with public key (2048-bit modulus and 32-bit exponent)
 - Image key certificate support with revocation capability
 - Uses OTP to authenticate public key
 - SHA256 digest of public key should be stored in OTP
- Encrypted Boot
 - Uses AES-GCM mode to decrypt and authenticate image
 - 256-bit key using PUF
 - OR
 - HW diversified 128-bit key using OTP
- Enhanced images support based on security policy



Key Store Details

- Activation code
 - ~1KB of data generated during PUF enrollment
 - Helper data (~Error Correction Code) to reconstruct root key
 - Generated during provisioning
- Key codes
 - User keys
 - Pre-shared keys
 - Provisioned during manufacturing
 - Intrinsic keys
 - Random keys









Key Management Table Authentication Only, No Encryption (See Slide 47)

Key Key Storage Description Owner **Key Generation** Key Use Name Use a certificate authority OEM Root of Generated by the image -OR-RSA 2048 Private key used for Used to sign the image key creation tool (python script). Trust -ORcertificate which is part of creating signatures of the image key Trusted OEM machine must Private Use of key material can be certificate image data have OpenSSL and should password protected in this tool Key CA have a strong RNG and be "Air Gapped" Used to validate the image Part of the boot image Root of Associated RSA 2048 public key for Tool can generate HEX output certificate which is holds the authenticating boot code. This key is of the hash of the public key to Image Public key. Not a trust OEM Hash stored on chip OTP for Public inserted into the image certificate be stored in OTP which is secret key, checked for which becomes part of the boot data checked during booting integrity by Root of Trust integrity check Key Hash. Generated by the image Trusted OEM machine must RSA 2048 Private key used for Image creation tool (python script). have OpenSSL and should OEM Private creating signatures of application Use of key material can be have a strong RNG and be Key binaries "Air Gapped" password protected in this tool Associated RSA 2048 public key for Image authenticating boot image. This key is Generated by the image Used to validate the boot Public OEM Part of the boot image inserted into the certificate which creation tool (python script) image upon every reset Key becomes part of the boot data



Key Management Table

Signed and Encrypted (Enhanced with PUF); See slide 49 for Fuse settings and previous slide

Same keys as detailed in previous slide, but also, the below

Key Name	Description	Owner	Key Generation	Key Use	Key Storage
PUF Boot Encryption Key (Image Key)	AES256bit symmetric key which is used to encrypt application code and data.	OEM	Tool generates AES key LPC Chip Set PUF KEY encrypts this key	Decrypt the signed image (GCM)	Built during manufacturing time. The plain text key is given to PUF and encrypted for in system storage in external flash.
K _{PUF} Hardware unique key	AES256 bit symmetric key which is used to protect the PUF Boot Encryption Key.	LPC Chip	Generated by the chip itself (PUF SRAM Fingerprint based)	Used to create other keys that go in the key store (like the PUF Boot encryption key)	Intrinsic to PUF
Activation Code	Not a Key, but data needed to support the PUF	LPC Chip (external Flash)	Generated during the enrollment phase of PUF	Not a key, but helper data needed to support PUF	External Flash (see slide 64)



Multiple options for establishing unique identity for the Chip

protections

ounterfeit

 1) RFC4122 compliant Unique ID
 2) OTP Key diversified by chip Unique ID

crip Unique ID can be used to create encrypted private key material 3) PUF generated key can operate in a similar capacity

Keys are protected by dedicated interface to HW AES engine Chip specific unique and protected keys along with secure boot flow protect OEM installed cloud credentials

Cloud credentials become part of the secure boot image that is protected for integrity and confidentiality

During manufacturing cloud credentials are encrypted with chip specific unique & protected keys Secure boot functions provide the foundation for establishing trust in the device functions ROM provides an immutable

ROM provides an immutable secure boot flow to support recovery from system run away scenarios

Arm MPU for memory partitioning for logical security TLS Stacks (Arm Mbed TLS) use hardware managed keys Option for AES engine to use OTP or PUF generated keys Hardware acceleration for AES and SHA-2

(SHA-256)

Based on device policies, data stored in system is protected by hardware managed keys

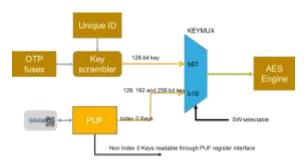
> Option for AES engine to use OTP or PUF generated keys

Confidentiality

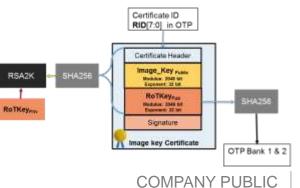
Data

Hardware acceleration for AES and SHA-2 (SHA-256 New firmware applied to the system must pass the secure boot flow ROM support for up to 8 revocations

Key Management



Secure Boot



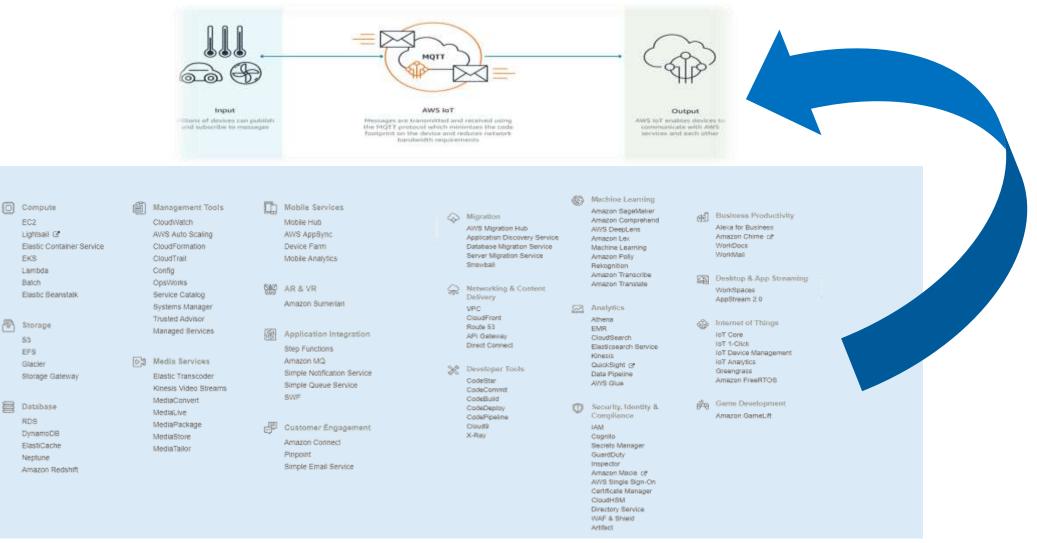
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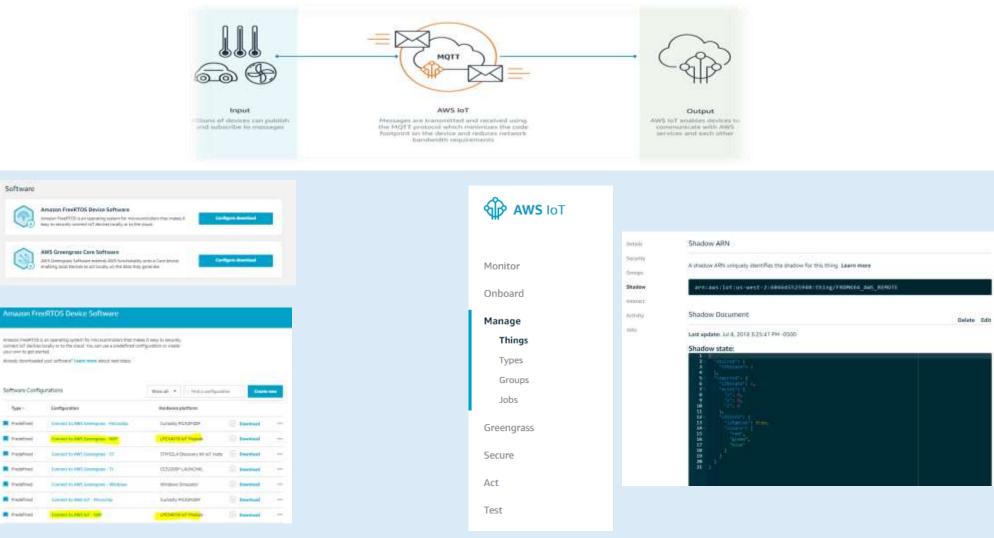


Amazon Web Services and AWS IoT

All AWS Services



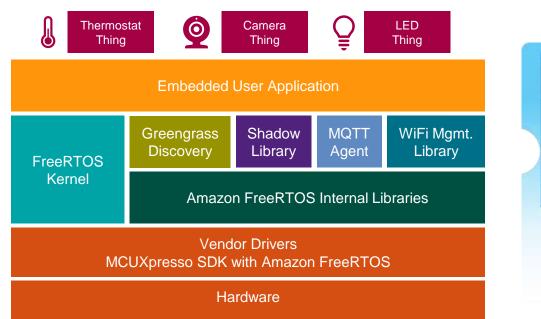
AWS IoT Device and Cloud Views





Amazon FreeRTOS at the Device

The FreeRTOS kernel is now an AWS open source project, and these pages are being updated accordingly. AWS are pleased to announce immediate availability of aws the MIT licensed Amazon FreeRTOS operating system, built on the FreeRTOS kernel v10.







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AWS IoT: What Can Go Wrong?



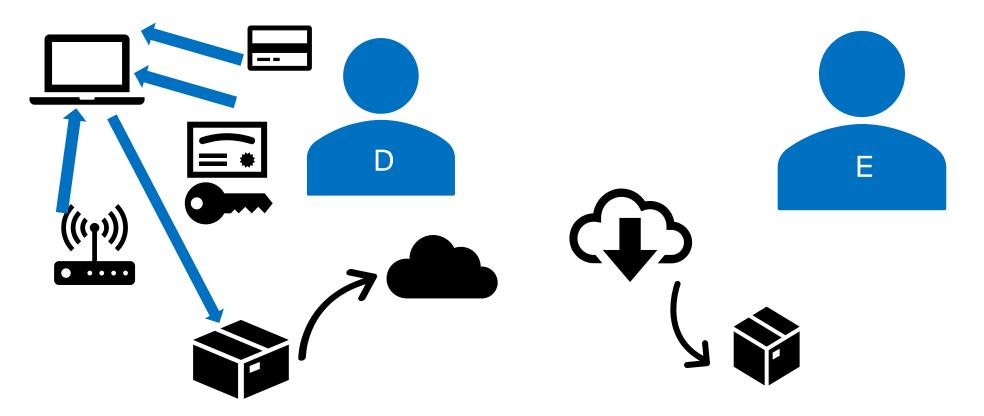


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Actual Events, Names and Faces Have Been Changed...

- Developer D from one Company is working jointly with Developer E from a different Company on benchmarking performance for a new processor and memory architecture
- They decide together to use an Amazon FreeRTOS example as a "typical IoT application"
- Developer D sets up an AWS account and gets the "MCUXpresso SDK Remote Control" application working and enables Show-Run-Time stats for Amazon FreeRTOS
- Excited about the results and working towards a deadline Developer D shares his work with Developer E.





Developer D: Uses personal credit card to create AWS account, creates device credentials for App, sets default policies for the device and the Smart phone App that controls it, uses home WiFi Credentials to get the app working then post the package for Developer E Developer E: Now has access to Developer D's Wifi SSID and password. With the device credentials Developer E can make a counterfeit device and use it to push large amounts of data to Developer D's AWS account leading to data fees charged to personal Credit Card of Developer D



Amazon FreeRTOS Examples are Part of MCXpresso SDK

1. IE

Name ✓ ■ ≡ aws_examples ✓ ≡ aws_greengrass_discovery_enet \checkmark aws_greengrass_discovery_wifi \checkmark aws_remote_control_enet \checkmark aws_remote_control_wifi \checkmark aws shadow enet aws shadow wifi

Great Examples!

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1 12 MARGINAL REPORT OF ALT OF ALT OF ALT OF A DECK AND LOCATED AND A DECK AN

Prepare the Android application

Red Property and Charles and Co.

The Android application requires Cognito service to authorize to AWS IoT in order to access device shadows. Use Amazon Cognito to create a new identity pool:

1. In the Amazon Cognito Console https://console.aws.amazon.com/cognito/ select "Manage Federated Identities" and "Create new identity pool".

plain text in a header file

2. Name your pool and ensure "Enable access to unauthenticated identities" is checked. This allows the sample application to assume the unauthenticated role associated with this identity pool. Note: to keep this example simple it makes use of unauthenticated users in the identity pool. This can be used for getting started and prototypes but unauthenticated users should typically only be given read-only permissions in production applications. More information on Cognito identity pools including the Cognito developer guide can be found here: http://aws.amazon.com/cognito/.

> Unauthenticated entities are allowed

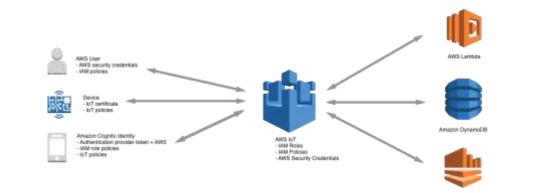






AWS Security Goals Statement

https://docs.aws.amazon.com/iot/latest/developerguide/iot-security-identity.html



Security and Identity AWS IoT Authentication

1. No.

 You are responsible for managing device credentials (X.509 certificates, AWS credentials) on your devices and policies in AWS IoT. You are responsible for assigning unique identities to each device and managing the permissions for a device or group of devices.

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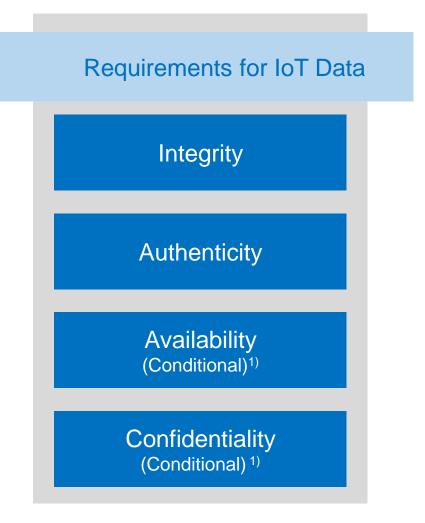


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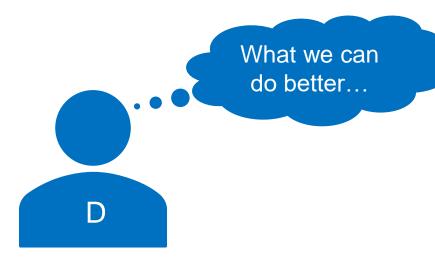


Other Application Specific Needs

- WiFi Credentials
- Passwords
- Personal Identifiable Information (Privacy)
- Payment Information
- Sensor Integrity/ Application Integrity







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credentials

10 ODDINAUTORIESISSI CAESCONAUTORIA CONTRACTOR CONTRACT and the set of the 28 *N4hU+jCZs2iM5a00NhVnH+C3aesF0H+pcP50to1C75ib467hUdgxc+09Mv3WoE/1\n* 21 "QSECAWEAAaNgHF4wHwYOVR0j88gwFoAUuzuriY8HrshdIaehT9z4NwR/+P0wHQYD\n" 22 "VR8088YEFC8XqTanQ1Ubpqv42m1fUzG5tFmcHVwGA1UdEwE8/wQCMAAwDgY0VR8P\n" 23 *AQH/BAQQAgeAVA86CSq6STb3DQEBCwJAA41BAQQN3M71Nr67n1nCMwc16nK6MFS31/n* 24 *S8jIVoLjc5rLWHE6MSTOt9w4vsz5Qo98jA8j3b1HvDMbsyRAvXNRKZIIgEKNhXPL7\n* 25 "rGPR1KOU8LLC8q1QtMaEyga2v79eeitAF98zz5LYE7zrLZGK95ZEq8+E9Q/Z1cn2\n" 26 */1HM2dl1nY2P0tDzaXj12w6f5nq2CDv8+U3+ygMknQdsfEEp3/wK/8ME71AyHF0h\n* 27 *NdHUrJK+Yy896sPH17gjOWi+DOw2eN9Dpg6mJh5seGL3eGRTr+PGRTmYmRPj1NHP\n* 28 *D8664PUbpooCeneuW61wPvn3rHHMgrHTnX6vEETz58pjn/41pR+DTyyPRZqV\n* 29 "-----END CERTIFICATE-----\n"; 30 310/* 12 * PEM-encoded client private key. 33 * > 🗟 aws_default_root_certificates.h 34 * Must include the PEM header and fouter: 35 * "-----BEGIN RSA PRIVATE KEY-----" 36 " "...bose64 data..." > aws_dev_mode_key_provisioning.h 37 * "----- END RSA PRIVATE REV-----"; 38 =/ 39 static const char clientcredentialCLIENT_PRIVATE_KEY_PEM[] = aws_greengrass_discovery_demo.h 40 "----- BEGIN RSA PRIVATE KEY----- \n" #1 "MITEpAIBAAKCAQEAsRfhufKtYTRID8Kge1v8QPZILCCqA60o2t9aV0xtJV6QKp3u\n" 42 *46-w6+14007779753w666w7sSw61w23enRahu7ALXK28w6+51Hoougxytn330Am0\n* > B aws greengrass lib private h

Protect device private keys with encryption/software

Prepare the Android application

· @ amazon-freerlos

bufferpool

> es config_files

e devmode key provisioning

> aws_bufferpool.h.

> aws_crypto.h

aws_demo.h

· aws clientcredential keys/l

> B aws_clientcredential.h

aws_doubly_linked_list.h

> aws_ggd_config_defaults.h

> aws_greengrass_discovery.h

En crypto

> in drivers

v include

FreeRTOS

The Android application requires Cognito service to authorize to AWS IoT in order to access device shadows. Use Amazon Cognito to create a new identity pool:

1. In the Amazon Cognito Console https://console.aws.amazon.com/cognito/ select "Manage Federated Identities" and "Create new identity pool".

2. Name your pool and ensure "Enable access to unauthenticated identities" is checked. This allows the sample application to assume the unauthenticated role associated with this identity pool.

Note: to keep this example simple it makes use of unauthenticated users in the identity pool. This can be used for getting started and prototypes but unauthenticated users should typically only be given read-only permissions in production applications. More information on Cognito identity pools including the Cognito developer guide can be found here: http://aws.amazon.com/cognito/.

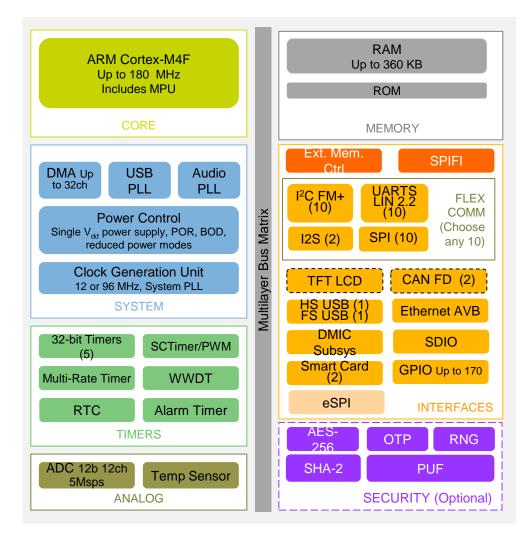
Set real AWS policies







LPC540xx/LPC54Sxx Block Diagram



High performance with high-end Graphical User Interface and security

- Cortex-M4F, 180MHz
 - Up to 360 KB RAM
 - 16KB EEPROM
 - XIP from QSPI via SPIFI
 - External Memory Ctrl (up to 32 bits)

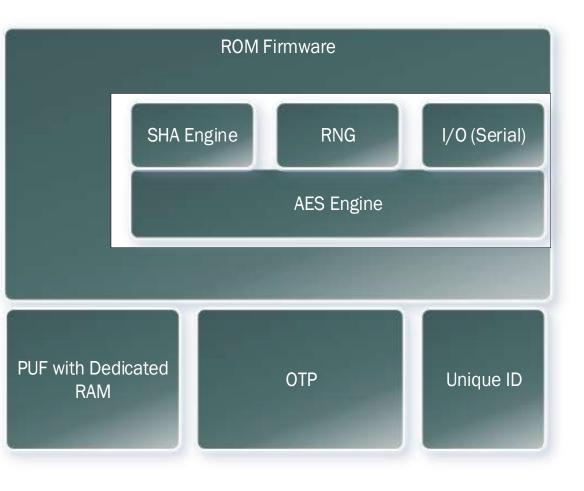
Key Features

- Graphic LCD with resolutions up to 1024 x 768
- CAN-FD controller x2 (LPC54608)
- eSPI interface (slave and LPC bus device functionality)
- Digital mic subsystem supporting voice detection
- · Hi-Speed and Full Speed USB
- USB: 1x HS (H/D) w/on-chip HS PHY
- XTAL-less FS USB Dev
- FlexComm: flexible serial connectivity
- Advanced Security Option:
 - AES-256, SHA-2, True RNG
 - PUF for key storage
 - HW diversified OTP Key Storage
 - Secure boot using 2048-bit RSA authentication and SHA-2 verification
 - Encrypted boot using AES-GCM mode



LPC54Sxx Security Sub-system

- ROM supporting secure boot methods
 - Authentication, Encryption, combination options
- AES Engine
 - Supports 128, 192 or 256 bit keys
 - Encryption modes: Electronic Codebook (ECB), Cipher Block Chaining (CBC), Cipher Feedback (CFB), Output Feedback (OFB), Counter (CTR), Galois Counter Mode (GCM)
- SHA Engine
 - Support SHA1 (160 bit) and SHA2 (256 bit)
- Physically Unclonable Function (PUF)
 - Device unique root key (256 bit strength)
 - Can store key sizes 64 bit to 4096 bit
 - Index 0 Keys routed to AES engine via direct HW bus
- 128-bit UUID per device
 - RFC4122 compliant
- Random Number Generator (RNG)
 - FIPS 140-1 compliant
- HW diversified OTP key
 - Key stored in OTP is scrambled using device unique ID



SRAM PUF Technology

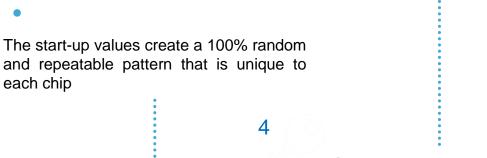
Process Variation

Naturally occurring variations in the attributes of transistors when chips are fabricated (length, width, thickness)

2

SRAM Start-up Values

Each time an SRAM block powers on the cells come up as either a 1 or a 0



Silicon Fingerprint

SRAM PUF Key (KPUF)

The silicon fingerprint is turned into a secret key that builds the foundation of a security subsystem

.

SRAM PUF Benefits

Device-unique, non-reproducible ٠ fingerprint

Leverages entropy of mfg. process

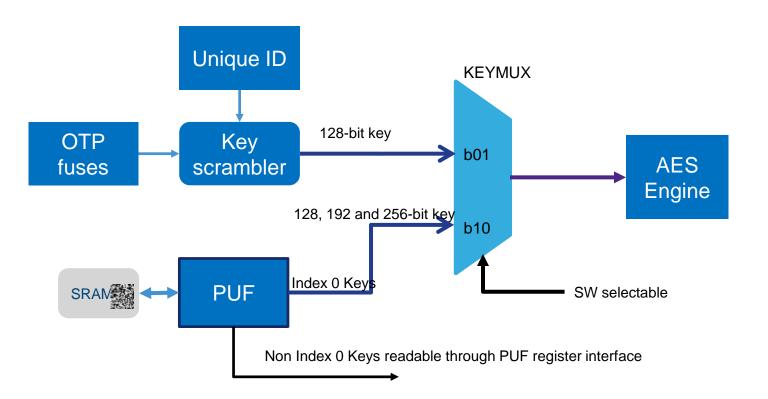
each chip

3

No key material ٠ programmed

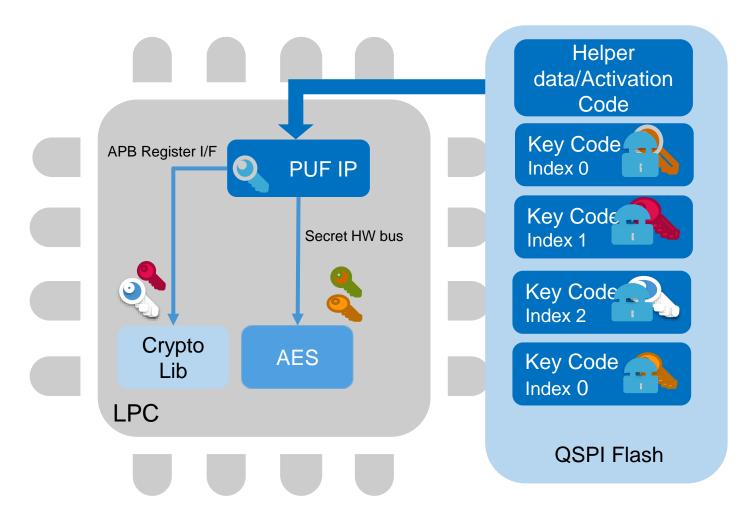
Key Management – HW AES Key Paths

- Critical keys feed directly to AES engine via HW bus
- No access to secret keys (Index 0) via SW readable registers
 - Except during provisioning
- PUF derives unique root key (K_{PUF}) per device from SRAM fingerprint
 - -Eliminates complexity of generating unique keys per device during provisioning
 - Protects credentials on a per device basis





PUF Key Store



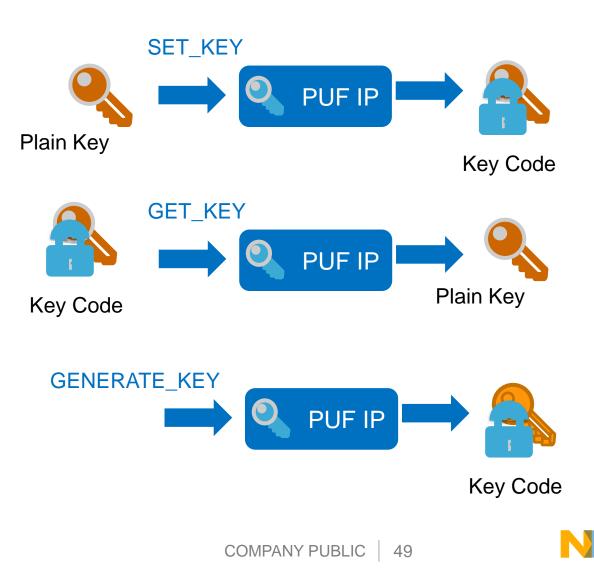
LPC PUF Features

- 256 bit strength Root key
- Supports wrapping of keys
 - 64 to 4096 bits keys
 - Generation of Intrinsic keys (random key)
 - Index 0 accessible through HW secret bus
 - Other indexes through register I/F

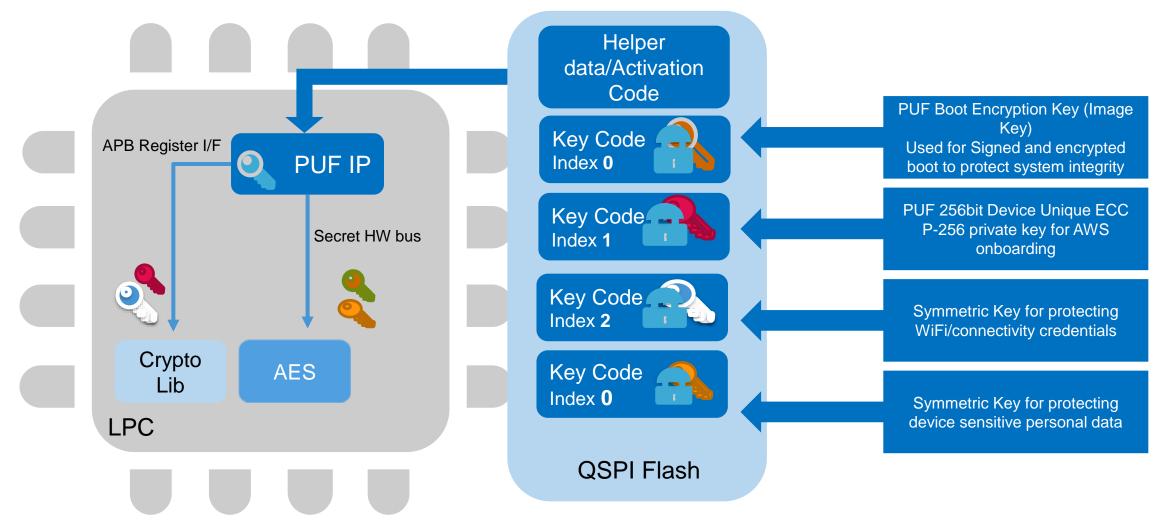


PUF Key Store – Key Generation

- Keys generated externally can be stored through PUF using SET_KEY operation
- PUF controller provides generation of device unique cryptographic strength keys (64 to 4096 bits) using GENERATE_KEY operation
 - If key index parameter is set to 0 then key is not known to anybody.
 - Any other key index are accessible through register interface using GET_KEY operation.



PUF Key Store for Updated Amazon FreeRTOS Example



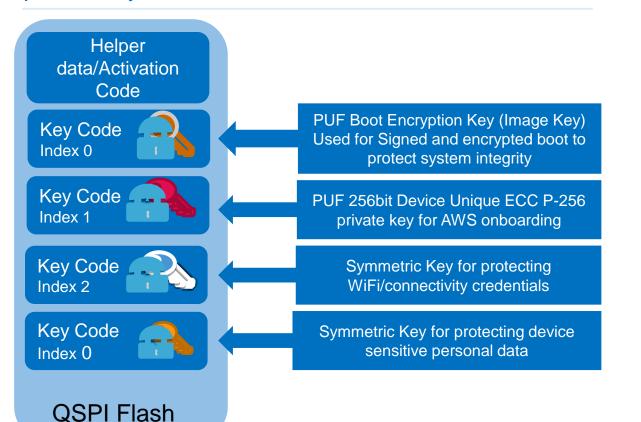


PUF Key Store for Updated Amazon FreeRTOS Example



Ex: PUF Key Store for Amazon FreeRTOS and Onboarding

Key storage protected by the "PUF protected" private key

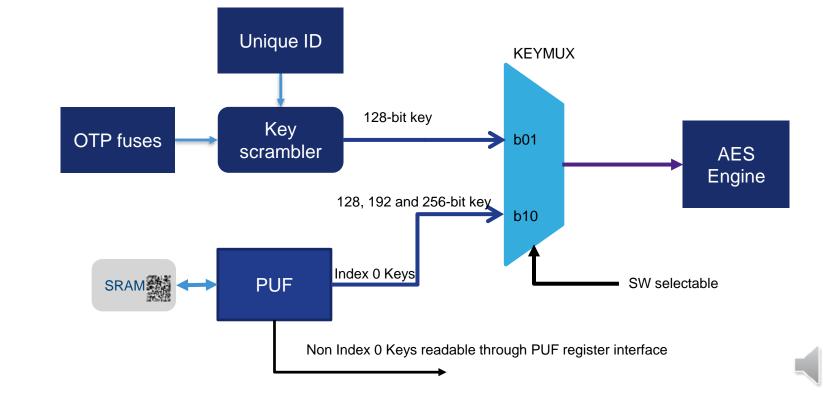


Benefits of this to onboard securely to AWS cloud

- + Protect device private key needed for AWS onboarding with a device unique symmetric key
- Integrity is protected with the secure boot with image encryption based on PUF (physically unclonable function)
- + PUF encrypted WiFi credentials to minimize risk of WiFi access code theft

Key Management – HW AES Key Paths

- Critical keys feed directly to AES engine via HW bus
- No access to secret keys (Index 0) via SW readable registers
 - Except during provisioning of installed key
 - For PUF generated key, no access



- per device during provisioning
- Protects credentials on a per device basis

PUF derives unique root

key (K_{PUF}) per device

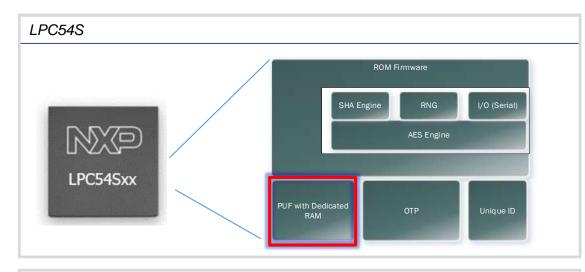
from SRAM fingerprint

-Eliminates complexity of

generating unique keys

Secure Onboarding with LPC54Sxx

Key Store for Amazon FreeRTOS and onboarding



NXP products used

LPC54Sxx IoT Microcontroller

Security use-cases features enabled

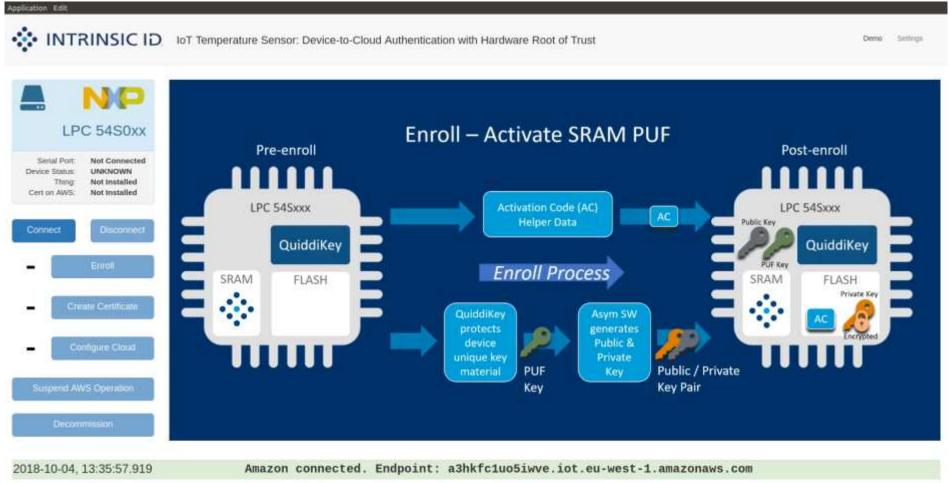
- Enable Amazon FreeRTOS and secure onboarding to the AWS cloud, by having the key encrypted with a PUF-protected encryption
- Securely store multiple private keys to protect system data (WiFi Credentials)
- Secure boot of the device using a PUF encrypted key

Security features of products used

- PUF Physically unclonable function with dedicated RAM
- HW accelerated encryption (AES, SHA) secure bus to PUF key
- ROM supporting secure boot methods



Demonstration Video





SECURE CONNECTIONS FOR A SMARTER WORLD

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