NXP'S DIFFERENTIATING GPIO EXPANDERS ADDRESS SYSTEM CHALLENGES IN EMERGING APPLICATIONS

MAY 21, 2020

SECURE CONNECTIONS FOR A SMARTER WORLD

TODAY'S AGENDA

- System benefits of General Purpose I/O (GPIO) Expanders
- Market trends and design challenges
- Recent developments
- What's next?
- Q&A

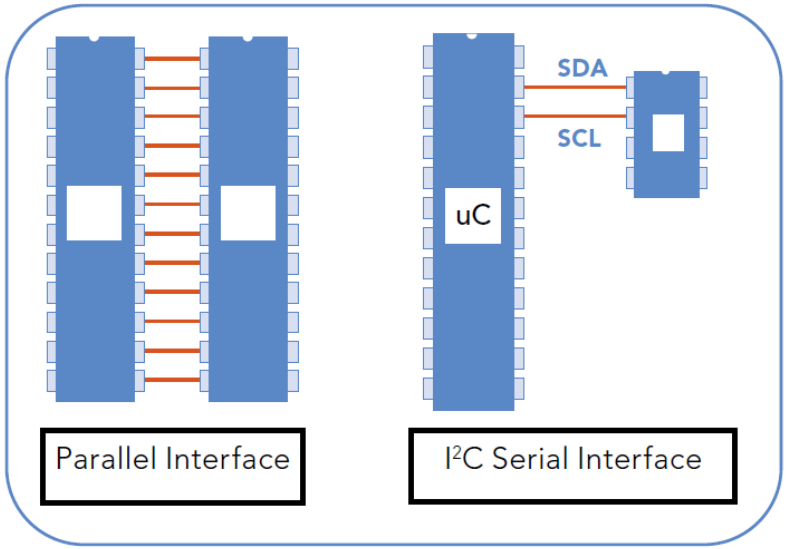
Featured Speakers:

Steve Blozis
International Product Marketing Manager

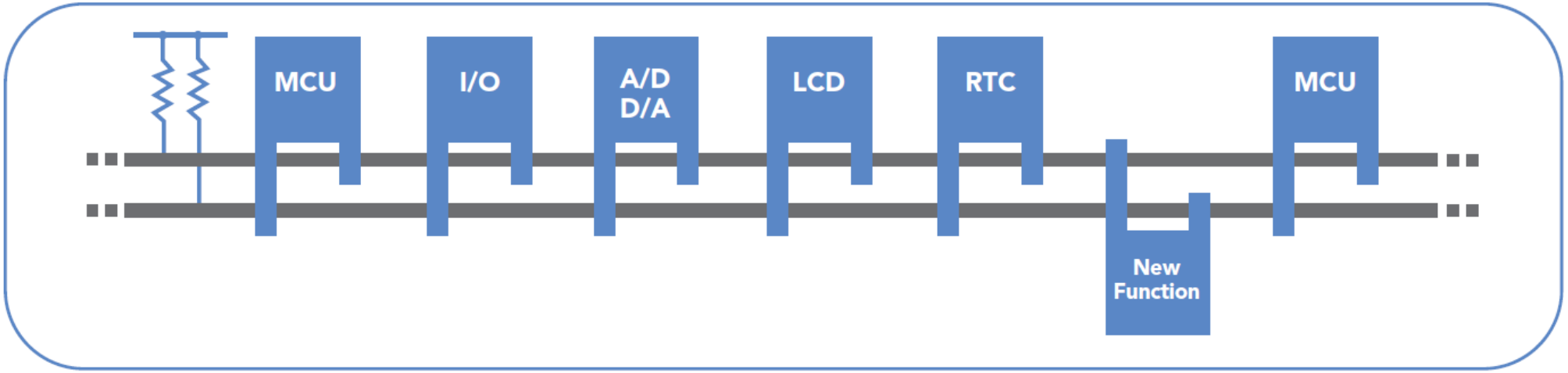
Emmanuel Nana
Technical Marketing Manager

SYSTEM BENEFITS OF GENERAL PURPOSE I/O (GPIO) EXPANDERS

A LITTLE BACKGROUND…



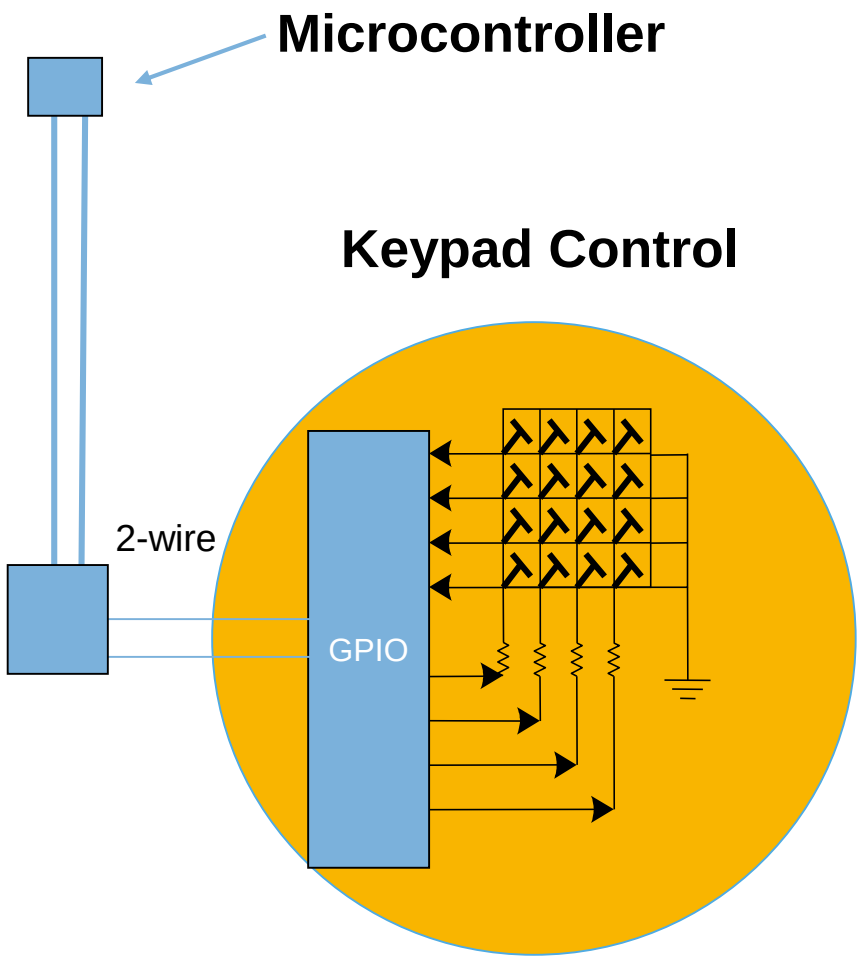
- I²C-bus invented by NXP (Philips) 30+ years ago
- Simple two-wire format
- Shrinks device footprint by reducing number of pins
- Fewer traces reduces design complexity and lowers system cost



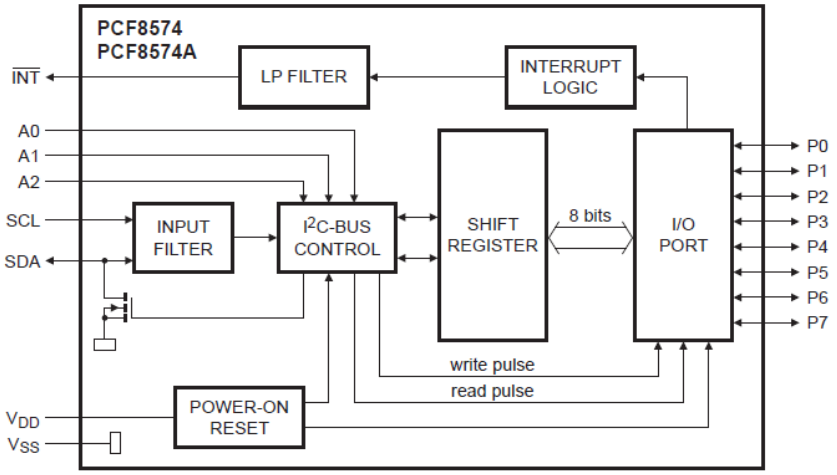
MARKET TRENDS AND DESIGN CHALLENGES

THE INCREASING NEED FOR GENERAL PURPOSE IO EXPANDERS

- IO Expansion via I^2C-bus
- Simplify Routing on PCB
- Power Management
- Voltage Level Translation



HOW DO I²C GPIO EXPANDERS WORK?



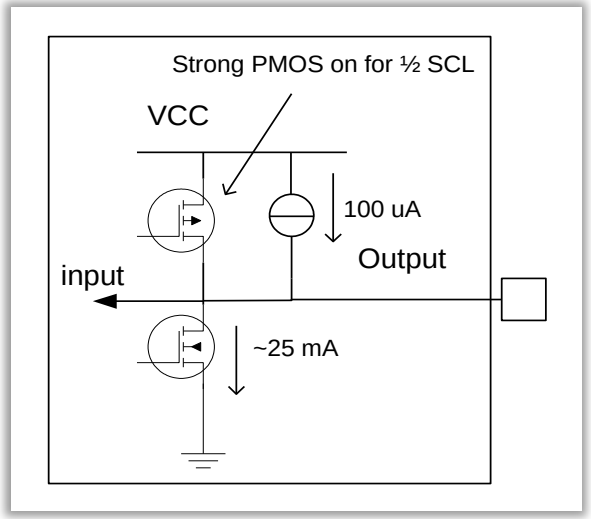
- To write to the outputs

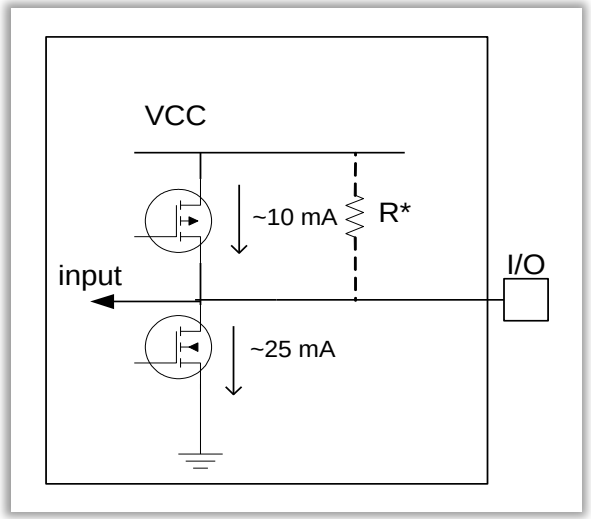
S	Address	$\overline{W}$	A	OUTPUT DATA	A	P

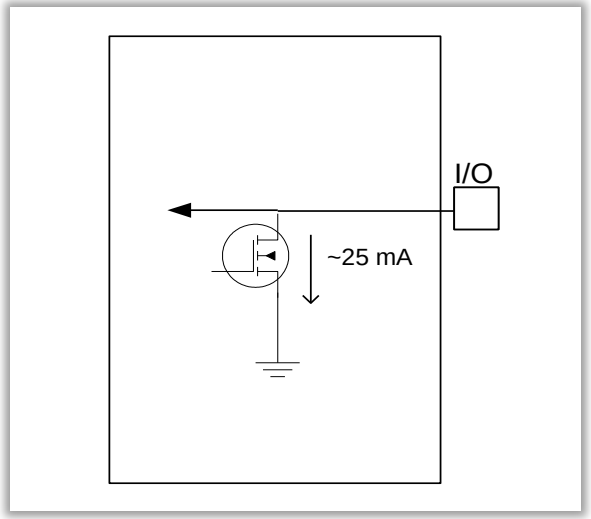
- To read input values

S	Address	R	A	INPUT DATA	$\overline{A}$	P

Quasi Output | **Totem-Pole Output** | **Open-Drain Output**







GPIO PORTFOLIO COVERAGE… THERE'S MANY OPTIONS

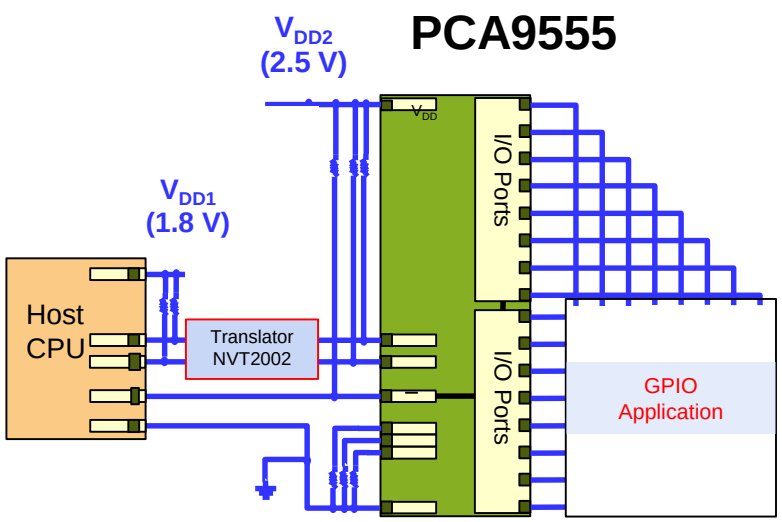
- **Over 50 unique functional devices**
  - Interfaces
  - Output structures
  - Bit widths
  - Hardware and digital features
  - I^2C-bus speeds
  - Supply voltage rails and translation

- **Wide array of industry standard and custom packages**

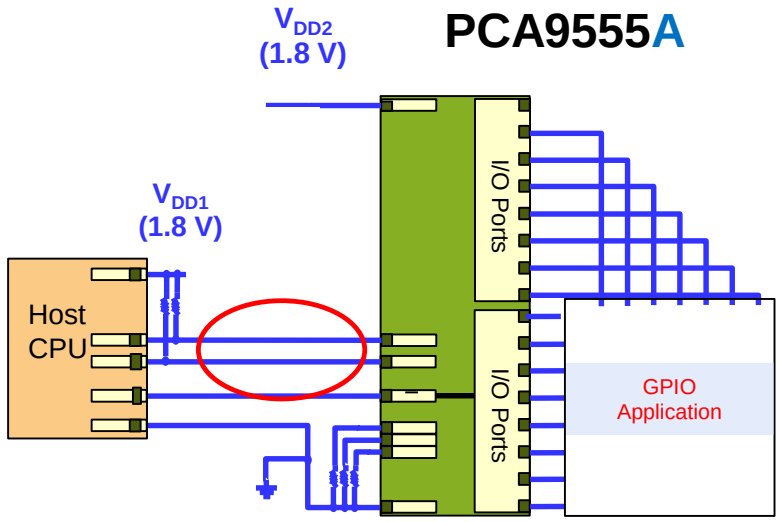
RECENT DEVELOPMENTS

RECENT PRODUCT DEVELOPMENT FOCUS AREAS

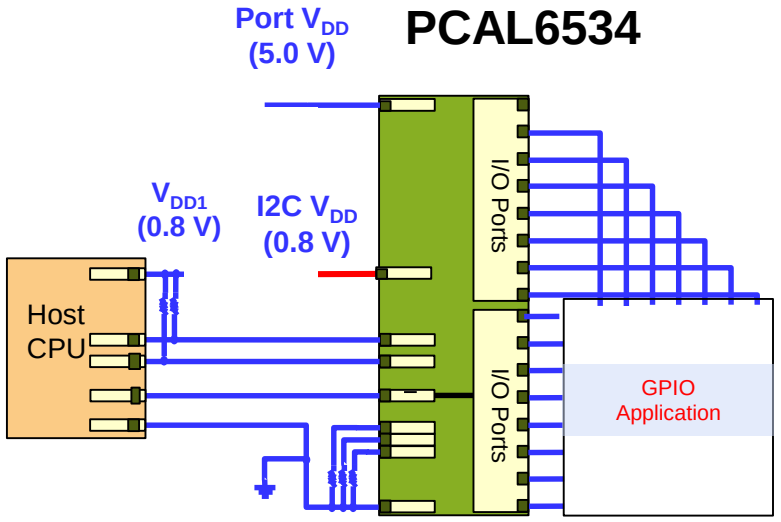
- Voltage translation
- Multiple supplies
- Agile IO
- More bit width options



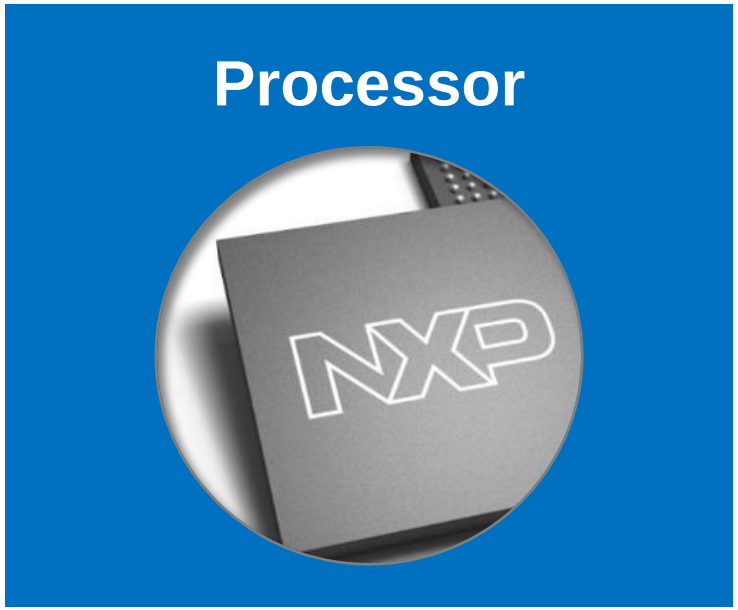
Single Supply



Lower-Voltage Single Supply

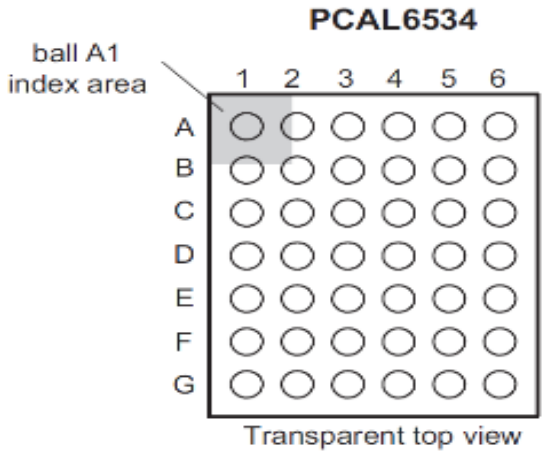


Dual Supply



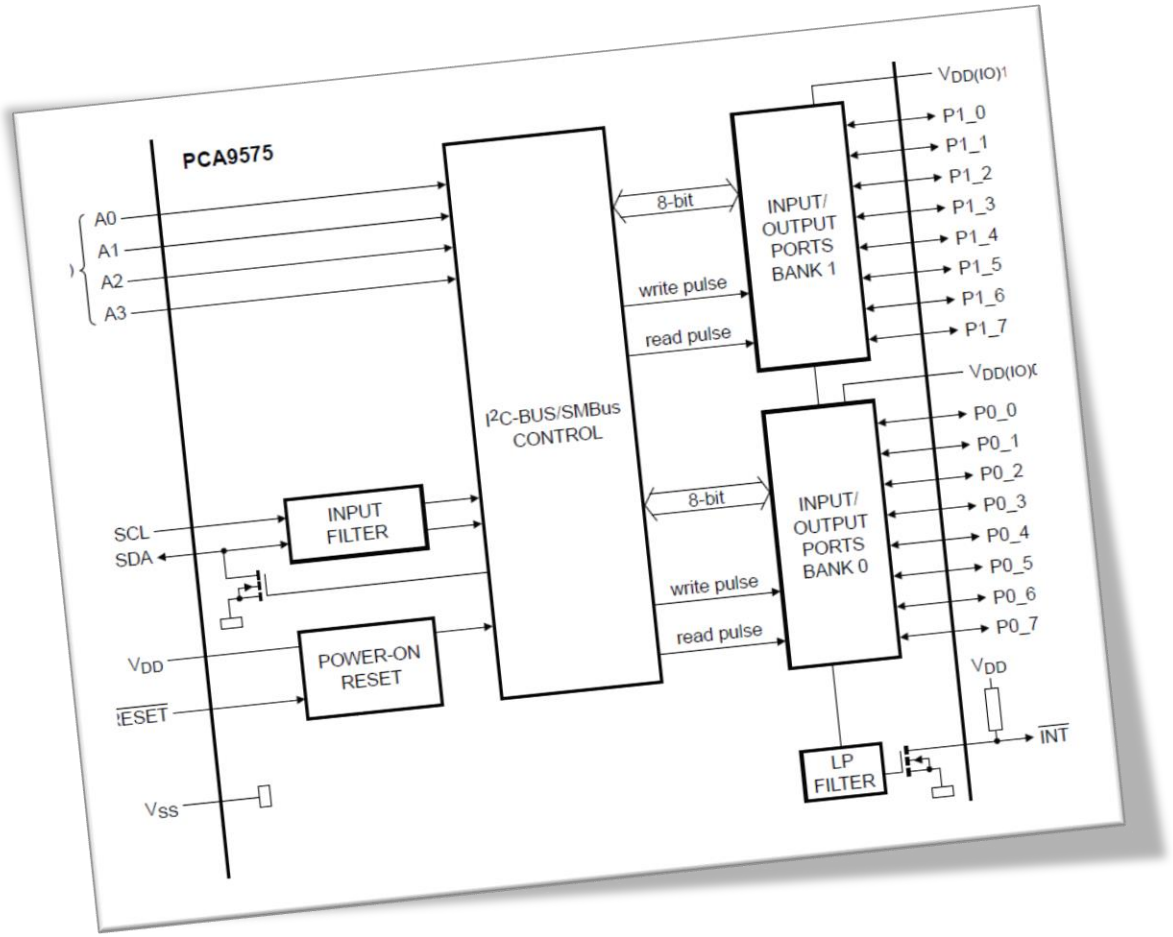
Geometry	I/O Voltages
40 nm	5 V
28 nm	3 V
14 nm	1.8 V
10 nm	1.2 V
7 nm	1.0 V
5 nm	<1.0 V

- Voltage level translating
- V_{DD} (I^2C): 0.8 V to 3.6 V or 1.65 V to 5.5 V
- V_{DD} (P-port): 1.65 V to 5.5 V
- ‘Agile IO’ features
- Lowest cost per bit
- Offerings:
  - PCA6408A & PCA6416A: Non Agile I/O 8-bit & 16-bit
  - PCAL6408A & PCAL6416A: Agile I/O 8-bit & 16-bit
  - PCAL6524 & PCAL6534: Agile I/O Plus 24-bit & 34-bit



MULTIPLE SUPPLIES AND LOW VOLTAGE GPIO EXPANDER

- Independent supplies
  - Interface voltage range from 1.1 V to 3.6 V
  - I/O voltage range from 1.1 V to 3.6 V
- Separate V_{DD} for each 8-bit bank
- Offerings:
  - PCA9574: 8-bit
  - PCA9575: 16-bit



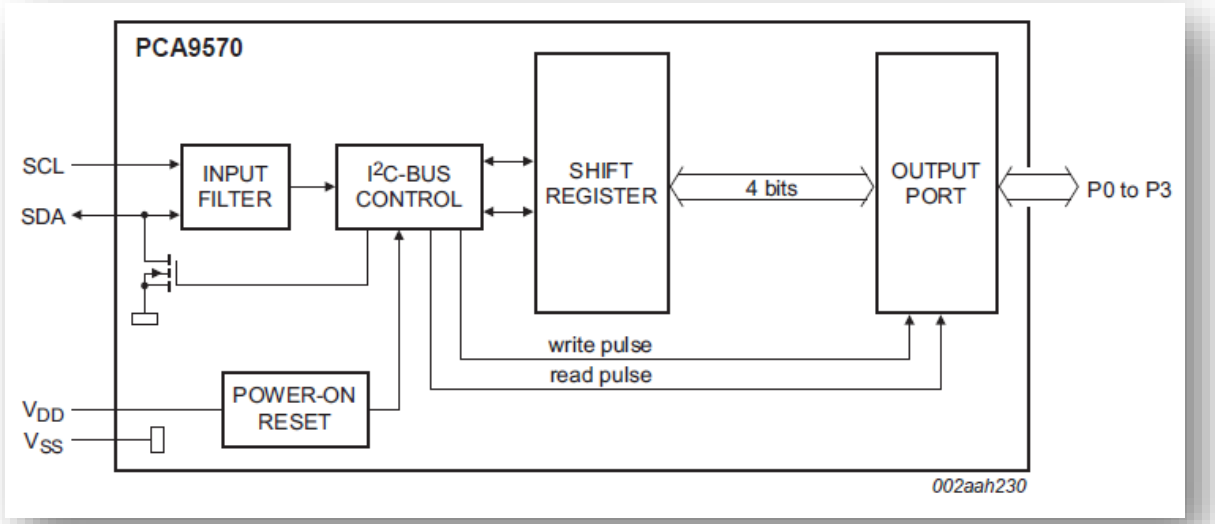
STANDARD PUSH PULL AND AGILE IO GPIO EXPANDER DIFFERENCES

Feature	PCA6408A PCA6416A	PCA9574 PCA9575	PCAL64xx PCAL65xx	Advantages
Bus-Hold Enable Command Byte		✔		User may enable bus-hold on the I/O's. The bus-hold feature provides a valid logic level when the I/O is not actively driven.
Pull-up / Pull-down Selector Command Byte		✔	✔	User may program a 100-kΩ pull-up or pull-down at the I/O's.
Interrupt Mask Command Byte		✔	✔	User may select which I/O changes would not generate an interrupt to reduce spurious interrupts by setting the corresponding bits in this register.
Interrupt Status Command Byte		✔	✔	User may read this register to identify the source of an interrupt directly without having to remember the previous state of the input
Open Drain Output Register			✔	Changes I/O from push pull to open drain per byte
Reset	Hardware	Hardware/ Software	Hardware	Reset device without having to cycle power

AGILE IO DEVICES ARE FEATURE-RICH AND PROVIDE FLEXIBILITY TO SYSTEM DESIGNERS

SMALL, LOW-COST, LOW VOLTAGE GPO EXPANDERS

- 4 mA push-pull outputs
- 1.1 V to 3.6 V operation
- 1 MHz I²C-bus interface
- Software Reset and power-on reset
- Available in tiny packages
- Offerings:
  - PCA9570: 4-bit
  - PCA9571: 8-bit



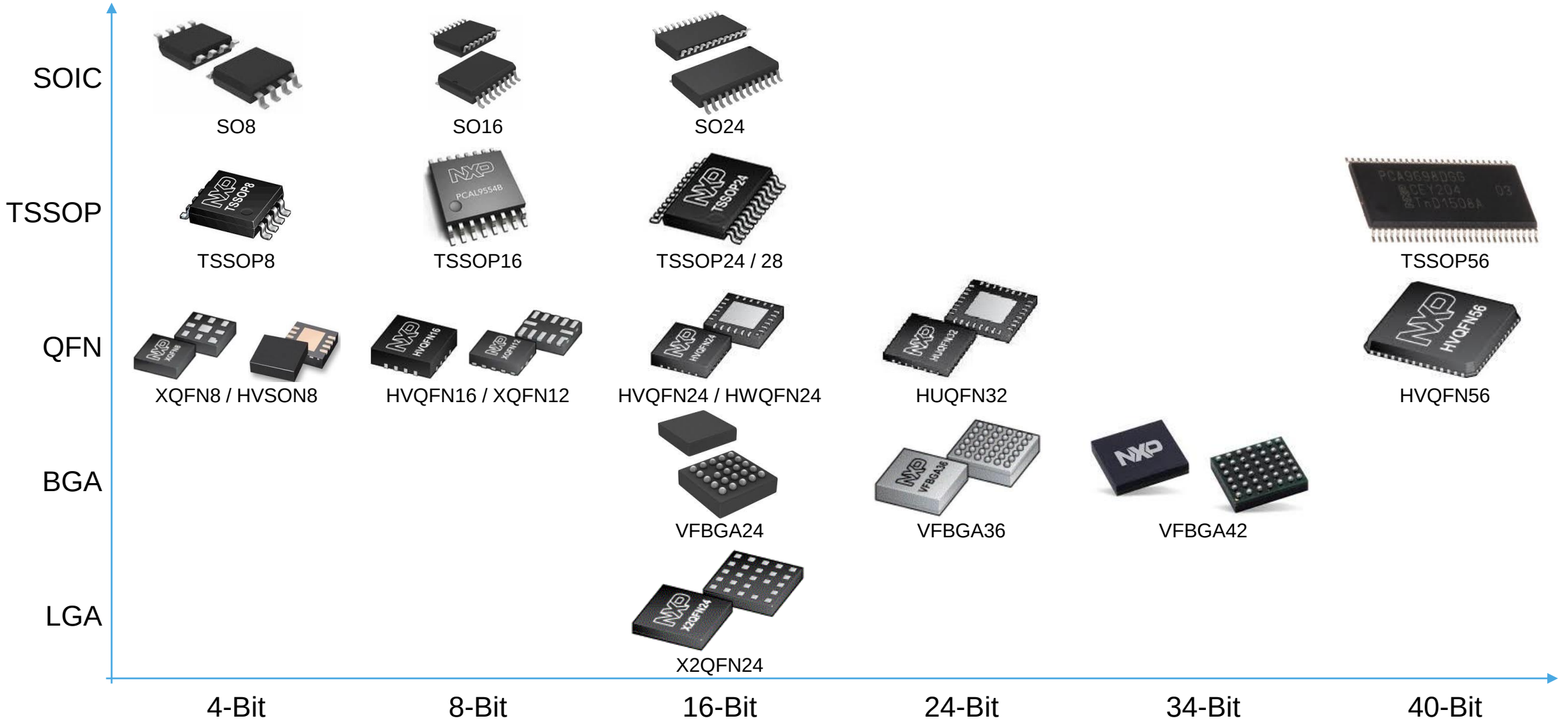
XQFN8

(1.6 x 1.6 x 0.5 with 0.5-mm pitch)

XQFN12

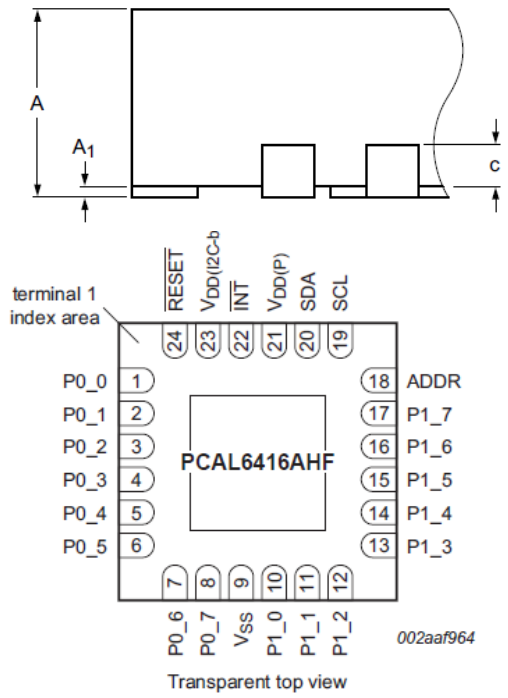
(1.7 x 2.0 x 0.5 with 0.4-mm pitch)

GPIO EXPANDERS PACKAGE COVERAGE



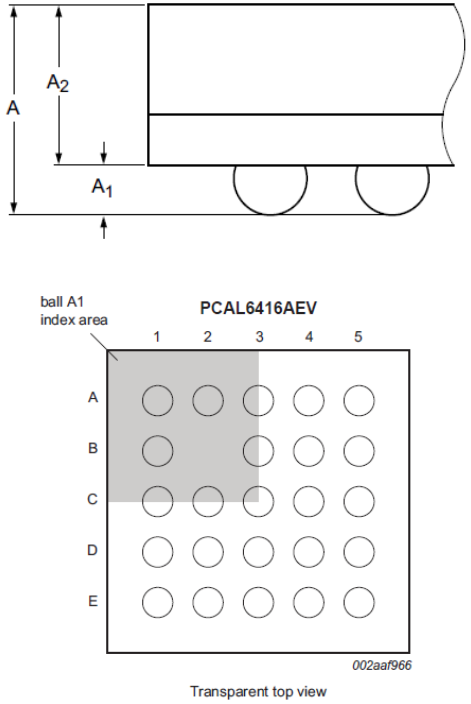
OFFERING SMALL AND LOW-PROFILE PACKAGES

QFN (Quad Flatpack No Leads) “Pads”



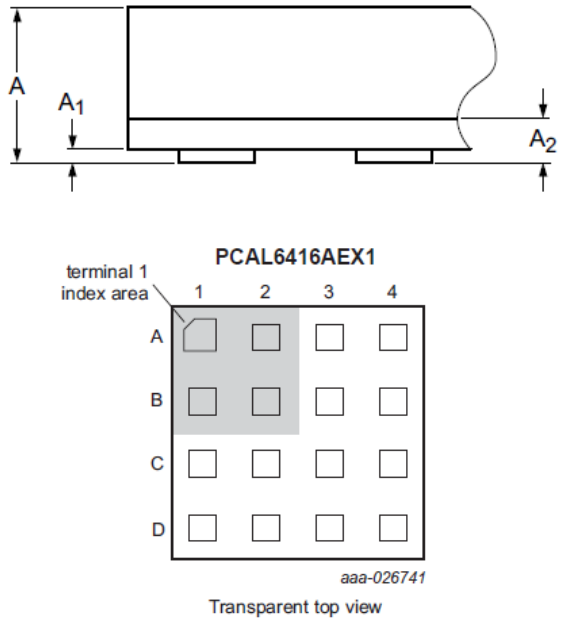
4 x 4 x 0.75 mm
0.5-mm pitch

BGA (Ball Grid Array) “Balls”



3 x 3 x 0.85 mm
0.5-mm pitch

LGA (Land Grid Array) “Pads”



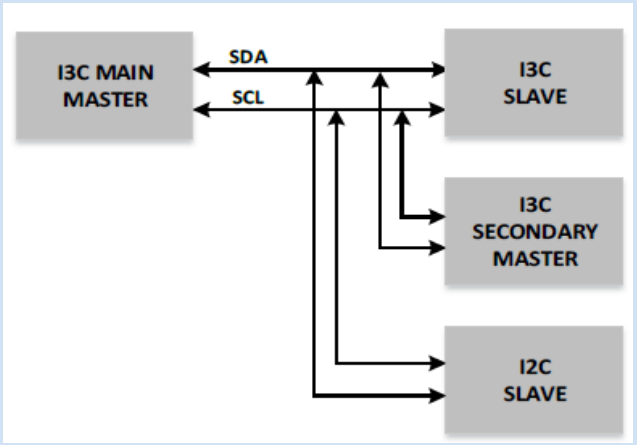
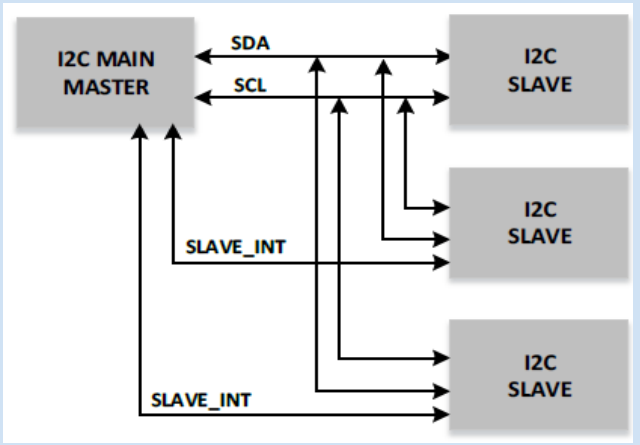
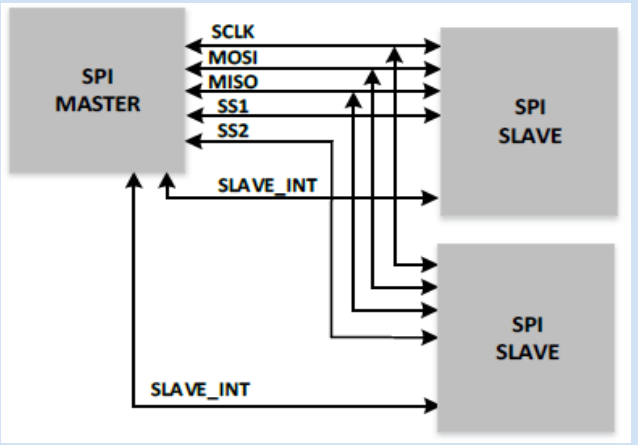
2 x 2 x 0.35 mm
0.4-mm pitch

WHAT'S NEXT?

INNOVATION NEVER STOPS

- **I3C** – higher speed and in-band interrupt – backward compatible to I^2C
- **Continued migration to lower voltage** – both to host and support chips (port)
- **GPIO default as output low** – vs having to configure at power up

I3C…THE NEXT BIG THING!

Parameter	MIPI I3C	I²C	SPI
Overview			
# of lines	2-wire	2-wire (plus separate wires for each required interrupt signal)	4-wire (plus separate wires for each required interrupt signal and additional selects). Not multi-master
Effective Real-Data Bitrate	30 Mbps max at 12.5 MHz (Typical:10.6 Mbps at 12 MHz SDR)	3 Mbps max at 3.4 MHz (Hs) 0.8 Mbps max at 1 MHz (Fm+) 0.35 Mbps max at 400 kHz (Fm)	Approx. 60 Mbps max at 60 MHz for conventional implementations (Typical: 10 Mbps at 10 MHz)

From MIPI I3C White paper: http://resources.mipi.org/MIPI I3C-sensor-whitepaper-from-mipi-alliance

NXP – AT THE FOREFRONT OF INNOVATION

- System benefits of General Purpose I/O (GPIO) Expanders
  - Serial interface reduces number of traces
  - GPIO Expanders allow systems designers to increase the IOs
- Market trends and design challenges
  - The increasing need for General Purpose I/O Expanders
- Recent developments
  - Lower I/O voltage
  - Multiple supplies
  - Agile I/O
- Future innovation
  - I3C: Higher speeds and in-band interrupt

ADDITIONAL RESOURCES

GPIO information: http://nxp.com/gpio

For questions, please contact: Stephen.Blozis@nxp.com

Q&A

THANK YOU