The MPC500 Family of 32-bit Embedded Controllers from Motorola

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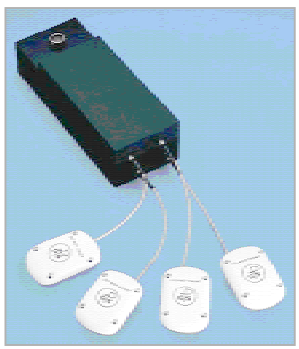
Application Examples

Robotics

- The Xerox® Palo Alto Research Center (PARC) Module Reconfigurable Robotics



Global Positioning System (GPS)

- An All-In-View, parallel tracking, 12-channel GPS receiver from Rokar and others

Powertrain Systems

- BMW's state-of-the-art Valvetronic Systems: the most advanced powertrain control technology in the world today (now on the road in the new 3-Series vehicles)

MPC500 Design Opportunities

A wide range of general-purpose embedded applications

Industrial

Robotics
Power meter
Handheld scope
Testing equipment
IV pump
Weight scale
Barcode printers

Telecom line test equipment
Traffic control system
Elevator control
Car wash
Medical equipment
Fuel cell
Power control

Currently 200+ registered design opportunities!

MPC500 Design Opportunities

A wide range of general-purpose embedded applications

Networking
Telecommunications
Test equipment
Cable TV

Avionics
Instruments
Fuel control
Altimeter
GPS

Control
Servo board
Motor controller
Room control system
Advanced motion control

Currently 200+ registered design opportunities!

MPC500 Family Features

- High-performance 32-bit RISC microcontrollers with floating point
- Embedded Flash (up to 1.0 MB)
- Highly integrated, intelligent peripherals
- Multiple Time Processor Units (TPU) with RISC core
- Dual A/D converters that support complex motor control
- Multiple CAN modules, which also support the industrial DeviceNet standard
- Available in automotive (-40° to +125° C) and industrial (-40° to +85° C) temperature ranges

MPC500 Family Features

- Industry standard JTAG interface and background debug module
- IEEE-ISTO Nexus 5001™ Standard Interface
- Chip-select system in SIU that can support external memory without need for external glue logic
- Suitable for applications using embedded Linux and other open source OS (MPC565)
- Production-ready devices with algorithms, drivers, and application software are available

Embedded Flash ~ A Core Competency

Why Embedded Flash?

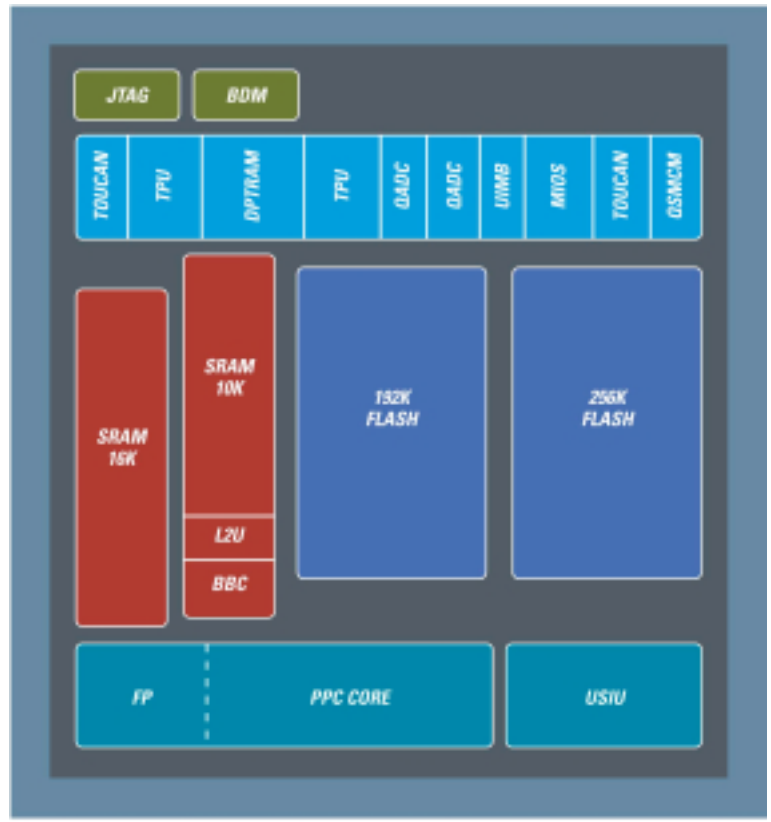
- **Integration, Performance, Reliability, Flexibility, and Security**
  - Allows user to reduce cycle times (development and production)
  - Enables field software updates
  - Saves money by reducing inventory/stocking levels
  - Enables self-calibration and adaptability of equipment
  - Helps protect application software
- **A Key Market Requirement**
  - Automotive, Computer Peripheral, Industrial Control, and Robotics

Embedded Flash ~ A Core Competency

- **Our Legacy**
  - 15 years experience with nonvolatile memory
  - First manufacturer in volume production with integrated nonvolatile memory (NVM)
  - First manufacturer with 32-bit Flash-based MCUs (MC68F333)
  - First manufacturer to offer 1.0 MB of embedded Flash
- **Our Strategy**
  - Flash is the main on-chip program memory
- **Embedded Flash Products**
  - MPC500 family: from 448 kB to 1.0 MB
  - Two memory blocks for easy in-application programming on the MPC565
  - Censorship: a security feature in Flash
  - Next-generation MPC5500 family with up to 6.0 MB

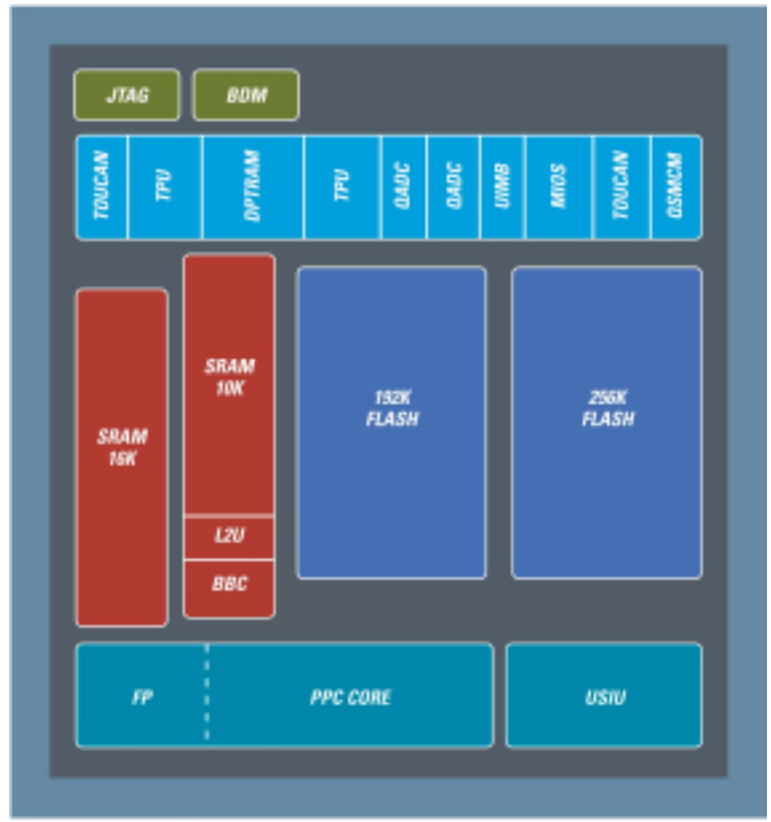
MPC555

- 40 MHz core compatible with the PowerPC™ instruction set architecture with floating point unit (FPU)
- 448 kB of qualified Flash memory
  - –One clock cycle access to page buffer
  - –Support for instruction and data storage, and censorship modes
  - –Endurance of 100 write/erase cycles
- 26 kB static RAM
- Dual Time Processor Units with 6 kB of emulation RAM
  - –32 TPU timing channels
  - –Standard TPU mask ROM functions or custom I/O routines that can be stored in emulation RAM
- 5V general-purpose I/O



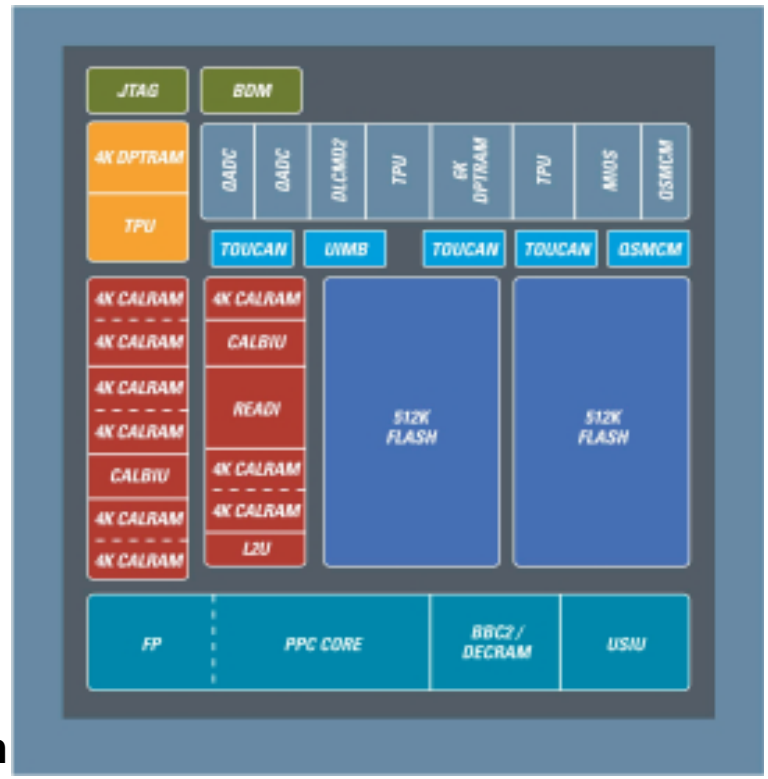
MPC555

- Dual Queued Analog to Digital Converter (QADC)
  - –32-channel internally multiplexed direct or up to 81 externally multiplexed with 10-bit resolution, with 5 µsec conversion time
  - –Flexible queuing system with up to 64 locations and automatic trigger modes
- System Interface Units (SIU)
- Full burst mode support for glueless external memories (SRAM and Flash)
- 32-bit data, 24-bit address bus with four chip-select regions, each with extensive timing options
- 64-bit timebase, real-time clock (RTC), watchdog and bus monitor protection circuits
- Other peripherals: MIOS, TouCAN, and QSMCM



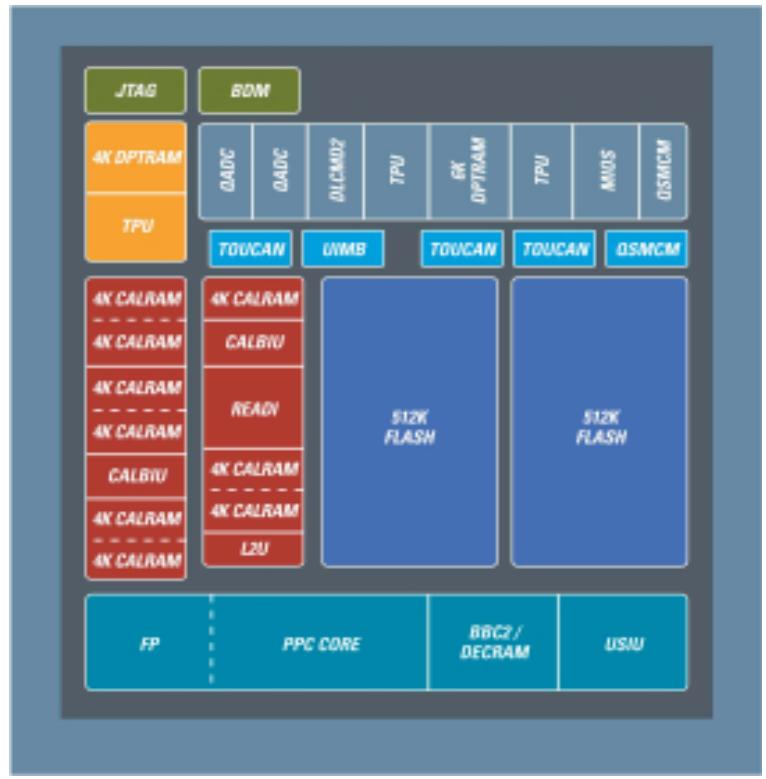
MPC565

- 40 or 56 MHz core compatible with the PowerPC instruction set architecture with FPU
- 1 MB of qualified Flash memory
  - One clock cycle access to page buffer
  - Support for instruction and data storage, and censorship modes
  - Endurance of 1000 write/erase cycles
- 36 kB static RAM
- Three Time Processor Units with 10 kB of emulation RAM
  - 48 timing channels
  - Standard mask ROM functions or custom I/O routines that can be stored in emulation RAM



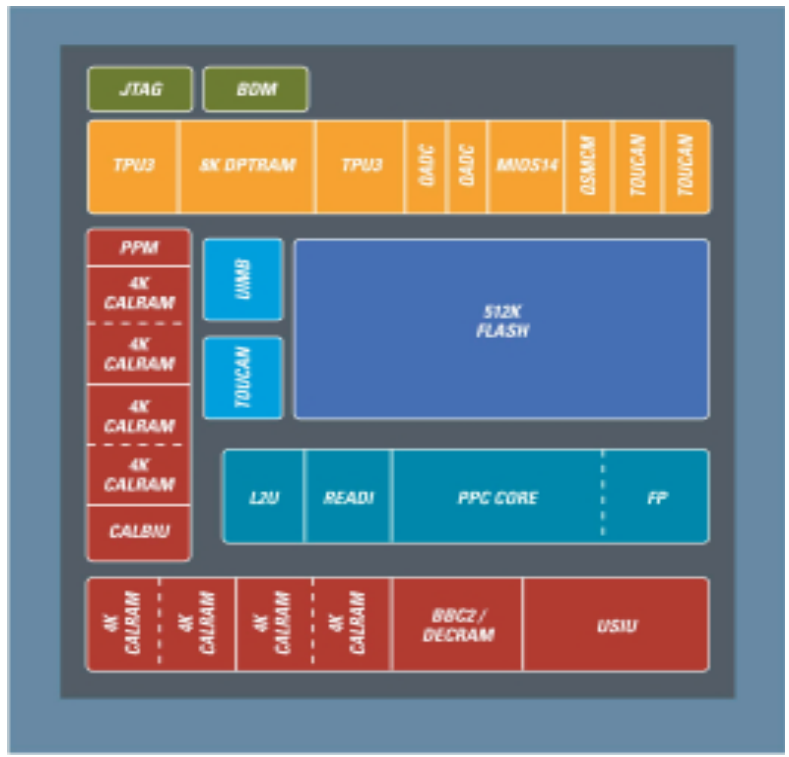
MPC565

- Dual Queued Analog to Digital Converter (QADC)
  - 40-channel internally multiplexed direct or up to 81 externally multiplexed with 10-bit resolution, with 5 µsec conversion time
  - Flexible queuing system with up to 64 locations and automatic trigger modes
- System Interface Units (SIU)
  - Full burst mode support for glueless external memories (SRAM and Flash)
  - 32-bit data, 24-bit address bus with four chip-select regions, each with extensive timing options
  - 64-bit timebase, RTC, watchdog and bus monitor protection circuits
- Other Peripherals: MIOS, three TouCAN (CAN version 2.0B), QSMCM, and one J1850 interface
- Full Class 3 Nexus debug and calibration port
- 5V general-purpose I/O



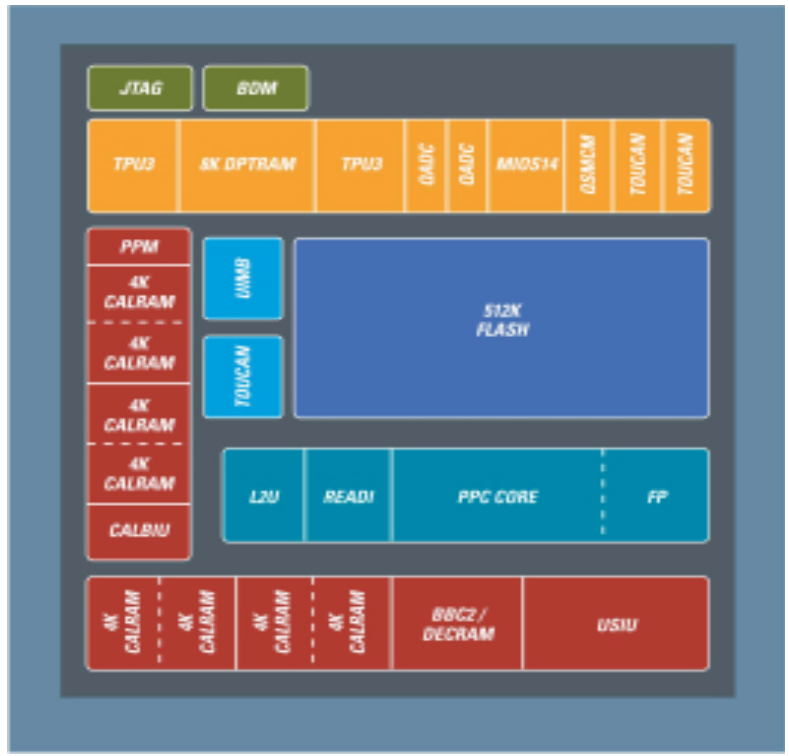
MPC563

- 40 or 56 MHz core compatible with the PowerPC instruction set architecture with FPU
- 512 kB of qualified Flash memory
  - One clock cycle access to page buffer
  - Support for instruction and data storage, and censorship modes
  - Endurance of 1000 write/erase cycles
- 32 kB static RAM
- Dual Time Processor Units with 8 kB of emulation RAM
  - 32 timing channels
  - Standard mask ROM functions or custom I/O routines that can be stored in emulation RAM



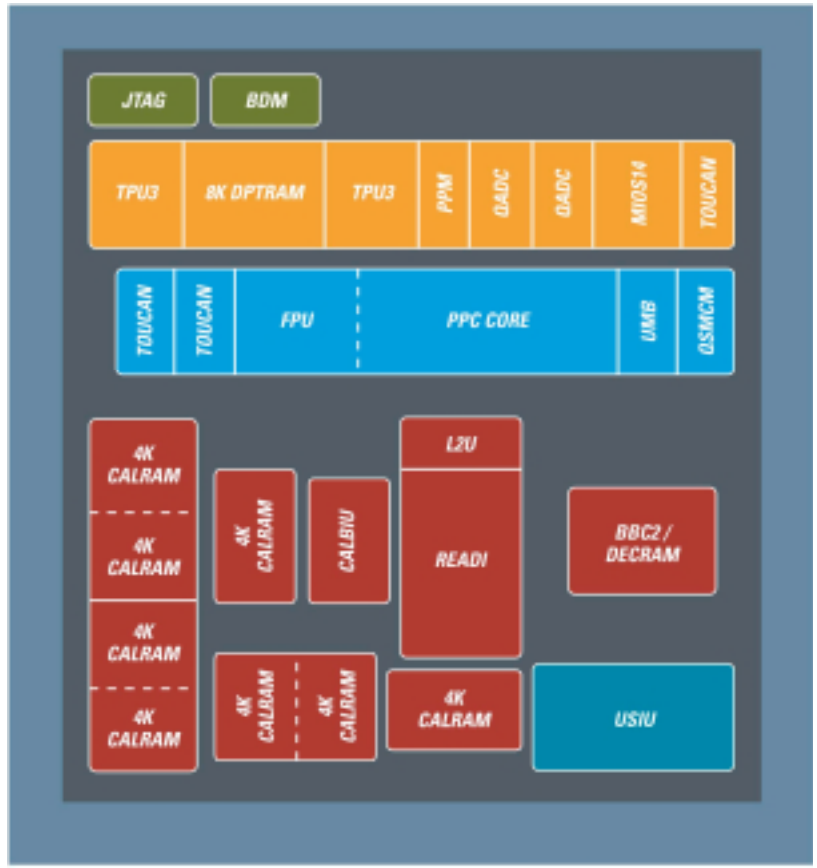
MPC563

- Dual Queued Analog to Digital Converter (QADC)
  - 32-channel internally multiplexed direct or up to 81 externally multiplexed with 10-bit resolution, with 5 µsec conversion time
  - Flexible queuing system with up to 64 locations and automatic trigger modes
- System Interface Units (SIU)
  - Full burst mode support for glueless external memories (SRAM and Flash)
  - 32-bit data, 24-bit address bus with four chip-select regions, each with extensive timing options
  - 64-bit timebase, RTC, watchdog and bus monitor protection circuits
- Other Peripherals: MIOS, three TouCAN (CAN version 2.0B), and QSMCM
- Full Class 3 Nexus debug and calibration port
- 5V general-purpose I/O



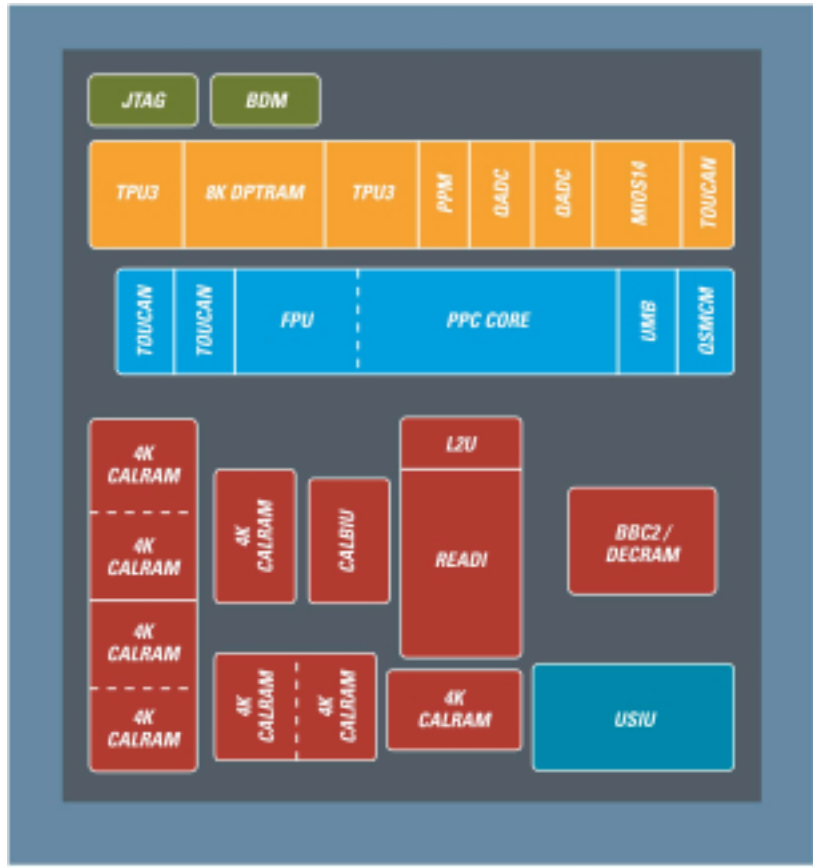
MPC561

- 40 or 56 MHz core compatible with the PowerPC instruction set architecture with FPU
- 32 kB static RAM
- Dual Time Processor Units with 8 kB of emulation RAM
  - 32 timing channels
  - Standard mask ROM functions or custom I/O routines that can be stored in emulation RAM
- 5V general-purpose I/O



MPC561

- Dual Queued Analog to Digital Converter (QADC)
  - 32-channel internally multiplexed direct or up to 81 externally multiplexed with 10-bit resolution, with 5 µsec conversion time
  - Flexible queuing system with up to 64 locations and automatic trigger modes
- System Interface Units (SIU)
  - Full burst mode support for glueless external memories (SRAM and Flash)
  - 32-bit data, 24-bit address bus with four chip-select regions, each with extensive timing options
  - 64-bit timebase, RTC, watchdog and bus monitor protection circuits
- Other Peripherals: MIOS, three TouCAN (CAN version 2.0B), and QSMCM
- Full Class 3 Nexus debug and calibration port
- Pin-compatible to MPC563



Tools Support

	MPC555	MPC561	MPC562	MPC563	MPC564	MPC565	MPC566	TPU
WindRiver								
BDM Debugger – SingleStep	X	X		X		X		
BDM Debugger – SingleStep with Vision	X	X		X		X		
Flash Programming – SingleStep	X	–		X		X		
BDM Debugger – VisionCLICK	X	X		X		X		
Nexus Debugger – VisionCLICK		X		X		X		
Nexus Debugger – SingleStep with Vision		X		X		X		
Flash Programming – VisionCLICK	X	–		X		X		
Compiler – DiabData	X	X	X	X	X	X	X	
MATRIXx	X	X		X		X		
Simulator – SingleStep	X	X	X	X	X	X	X	
Lauterbach								
BDM Debugger Trace32	X	X	X	X	X	X	X	X
Nexus Debugger Trace32		X	X	X	X	X	X	X
Code Trace (with Bus access)	X	X	X	X	X	X	X	
Code Trace (Nexus)	X	X	X	X	X	X	X	
Metrowerks								
IDE – CodeWarrior	X	X		X		X		
Flash Programming – IDE	X							
OSEK (RTOS)	X	X		X		X		
Automotive Development System	X			X				
Axiom Manufacturing								
Low Cost Evaluation Board	X							
Mid-range Evaluation Board	X							
Full Feature Evaluation Board	X	X	X	X	X	X	X	
Ashling Microsystems								
BDM Debugger – Opella, Genia, and Vitra	X	X	X	X	X	X	X	
Nexus Debugger – Vitra (w/trace)		X	X	X	X	X	X	X
Nexus Debugger – Opella, Genia		X	X			X		
GreenHills								
IDE, Debugger – Multi	X	X		X		X		
Compiler C/C++/EC++	X	X		X		X		

	MPC555	MPC561	MPC562	MPC563	MPC564	MPC565	MPC566	TPU
P & E Microsystems								
Low Cost Debugger	X	X		X		X		
Flash Programming Tools	X					X		
GNU								
Compiler/Debugger	X	X		X		X		
Motorola								
TRUASM								X
Ashware								
TPU Simulator								X
ETAS								
EsCOSEK	X	X		X		X		
Calibration Tools (ETK)	X	X		X		X		
Calibration Tools (ETK) Nexus	X	X		X		X		
dSPACE								
Target_ink	X	X		X		X		
dli								
Logic Analyzer	X	X		X		X		
Agilent								
Logic Analyzer	X	X		X		X		
Inverse Assembler, Source Correlation	X	X		X		X		
Emulation Probe (BDM)	X	X		X		X		
Tektronix								
Logic Analyzer	X	X		X		X		
Abatron AG								
BDM Support	X	X		X		X		
Accelerated Technologies								
Nucleus (RTOS)	X					X		

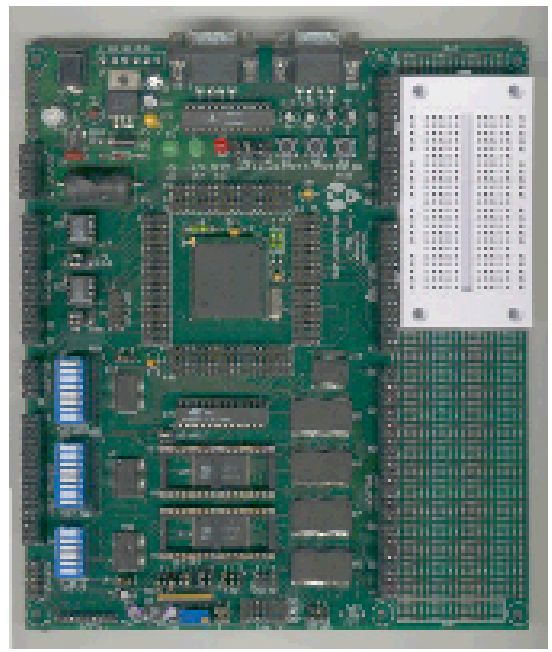
* Leading tools suppliers

* Comprehensive tools

Evaluation Board

MPC555 Evaluation Board

- Standard fixed memory: 128 kB x 32 Fast SRAM (12 ns), 128 kB x 32 Flash EPROM (120 ns)
- Two configurable 32-pin memory sockets for 32 kB to 2 MB PROM or 32 kB to 512 kB SRAM
- 2 TouCAN ports w/ transceivers (PCA82C250)
- LCD interface connector with contrast adjust, memory mapped (80 or 160 character)
- Power_Port with power supply access
- BDM debug development connector
- All I/O connectors on .1" grid
- Solderless and standard prototyping areas
- 6 to 25V DC input
- Part number: MPC555CME
- Suggested retail price ~ $650



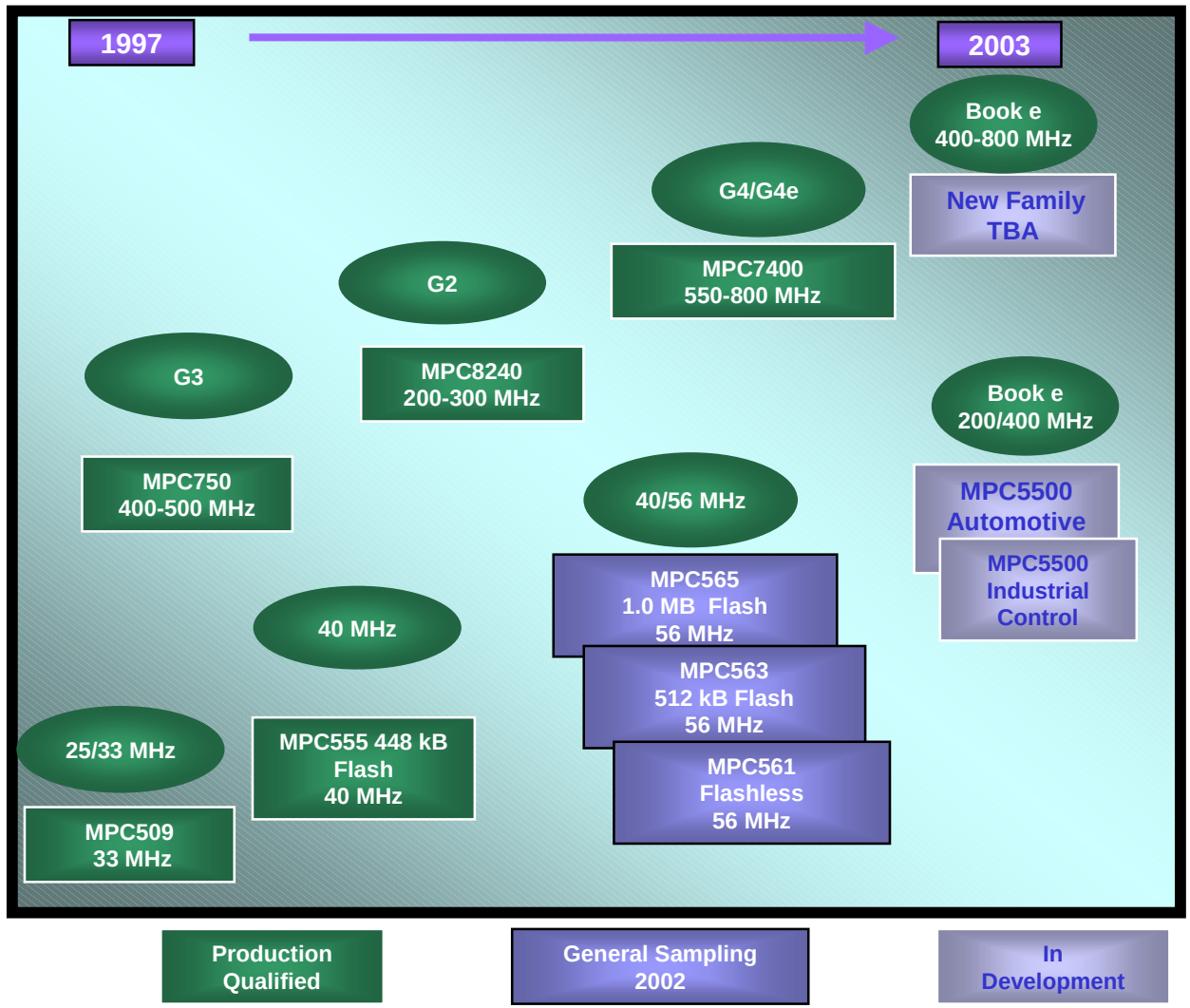
MPC500 Family Benefits

- Excellent functionality and performance
- High level of flexibility
- Low development costs
- Quick time-to-market
- Code capability and scalability among MPC500 family members and between generations
- Commitment to extensive product roadmap
- Software portability
- Comprehensive portfolio of hardware and software development tools

MPC500 Family Overview

Product	MHz	Flash (byte)	RAM (byte)	Timers	Serial	Temp	Apps
MPC555 Available Now	40	448K	26K static RAM 6K DPTRAM	2xTPU3 MIOS1	1xQSMCM (2xSCI, 1xQSPI), 2xCAN	-40° to +85°C -40°C to +125°C	Engine control, transmission control, suspension and stability, instrumentation, industrial control, avionics
MPC565 Engineering Samples Available Now	40 or 56	1.0M	36K static RAM 10K DPTRAM 4K DECRAM	3xTPU3 MIOS14	2xQSMCM (4xSCI, 2xQSPI), 3xCAN, J1850	-40° to +85°C -40°C to +125°C	
MPC561 Engineering Samples Available Now	40 or 56	0	32K static RAM 8K DPTRAM 2K DECRAM	2xTPU3 MIOS14	1xQSMCM (2xSCI, 1xQSPI), 3xCAN	-40° to +85°C -40°C to +125°C	
MPC563 Engineering Samples Available Now	40 or 56	512K	32K static RAM 8K DPTRAM 2K DECRAM	2xTPU3 MIOS14	1xQSMCM (2xSCI, 1xQSPI), 3xCAN	-40° to +85°C -40°C to +125°C	

MPC500 Family Roadmap

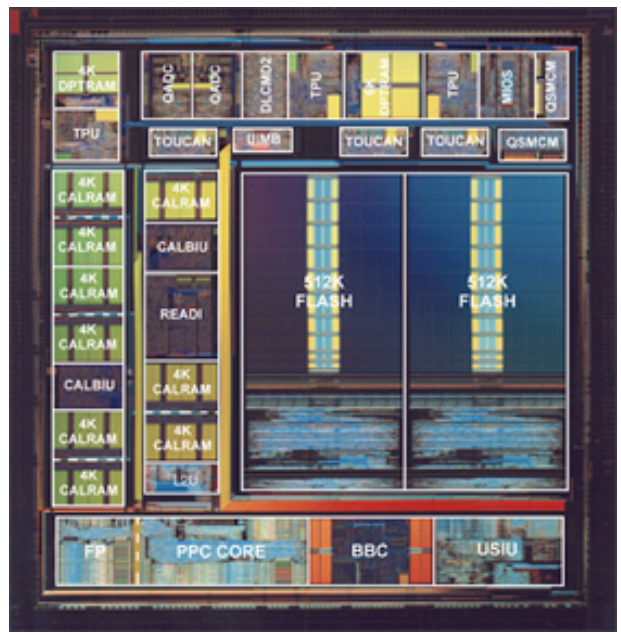


Motorola's High Integration Microcontrollers

Key Integration Features

- High-performance core
- SRAM
- Embedded Flash
- Intelligent timer systems
- Communications
- Analog
- System integration
- Nexus

MPC565



Information Sources

- **Product Library**
  - **http://e-www.motorola.com/webapp/sps/library/prod_lib.jsp**
- **Documentation Library**
  - **http://e-www.motorola.com/webapp/sps/library/docu_lib.jsp**
- **Tools Library**
  - **http://e-www.motorola.com/webapp/sps/library/tools_lib.jsp**
  - **Metrowerks—http://www.metrowerks.com/**
- **MPC500 Web Resources**
  - **http://e-www.motorola.com/automotive/architectures/powerpc.html**

- **Talk to Others Who Use Microcontrollers Compliant with PowerPC Architecture**

  To subscribe to the MPC500 list and receive information from Motorola's application engineers:
  - **Send a message to Majordomo@oakhill-csic.sps.mot.com**
  - **In the body of the message, type: Subscribe MPC500**