

Errata

Valis X3ERR/D
Rev. B, 9/2003

Valis Microprocessor
Evaluation System
Errata



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1 Introduction

This document describes the known errata and limitations of the Valis MPMC card for the Sandpoint reference platform. In all cases, if an errata has a workaround, it is applied to the system before shipped to customers.

The errata revision (“A”, “B”, etc.) is updated every time a new problem is found and systems have been shipped. If your current system is a “Valis X3 rev ‘A’”, then it has all rev “A” fixes, but no rev “B” fixes.

The errata should be applied to the published schematics to determine the correct wiring of the MPMC+Sandpoint system (i.e. after changes are applied).

Lastly, note that some errata are not true errors but requests for minor modifications to improve the system. These errata are not performed but may be rolled into possible future revisions of the system, if any.



ERRATA

Table 1: Summary of Valis Errata

#	Type	Problem	Impact	Work-Around	Affects	Rev
1	Assy	R35 and R36 should be 1206	Little.	BOM is correct; correct compont. X4: N/A.	X3	A
2	CAD	CKO and CKO_GND not accessible with heat sink installed.	Hard to use.	None. X4: Reposition.	X3	A
3	BOM	R95 (L3ADDR18 pulldown) not installed; required for non-MPC7457	Possible cache failure.	Install R59 (1K 0603) on MPC7450/MPC7451/MPC7455 builds. X4: None.	X3	A
4	Assy	All the LEDs are backwards.	LED's inoperative.	Rotate all SMD0603 LEDs 180 degrees. X4: Fix pad 1 geometry issue(?).	X3	A
5	BOM	Install J2 by default.	None.	Add to BOM. X4: None.	X3	A
6	BOM	LED series resistors should be 390 ohm, not 39 ohms.	Overcurrent, early failure.	Replace R1-R12 with 390 ohm resistors. X4: Change value.	X3	A
7	DES	COP_SRST* is not buffered and merged with on-board MPC107-based SRESET.	SRESET may not work.	TBD X4: TBD.	X3	A
8	CAD	Thermal relief insufficient; Q4 has none, Q2 could be larger.	Overheating.	None. X4: Add fill.	X3	A
9	BOM	R56 and R57 are both non-stuff.	PCI OVDD not set.	Install R56 (PCI 5V). X4: Correct BOM.	X3	A
10	CAD	VCC_PCI_C (PCI clamp) voltage trace too fine.	PCI clamp ringing/delay.	None. X4: Make VCC_PCI_C at least 10 mils, preferably 20.	X3	A

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#	Type	Problem	Impact	Work-Around	Affects	Rev
11	DES	LBS interface has connections to A(0:3) as part of the address, which are not very useful on the MPC745X+MPC107.	Reduced available address coverage.	None. X4: Use 8 bits starting at A(4).	X3	A
12	DES	R74 (GBL*) pullup need not be 300 ohm; 10K is sufficient.	None.	Change BOM. X4: Change component.	X3	A
13	DES	SDRAM LED is triggered by refresh.	SDRAM looks busier than it actually is.	None. X4: Use SDRAM WE* signal instead.	X3	A
14	DES	CPU PLL configuration pins are scrambled yet again.	Hard to map hardware spec to switches.	Use config sheet. If you hold the card correctly, PLL_CFG(0:4) can be entered left-to-right just as in the hardware spec. Just enter PLL_CFG(0:3) and jump to the last bit. X4: Order them as requested	X3	A
15	DES	CPU LED is not CPU activity, it is bus activity.	Misleading.	None. X4: Change label to "BUS".	X3	A
16	DES	R94 is not connected to VCORE (if installed), it is connected to OVDD.	VCORE abnormally low due to incorrect sense voltage.	For MPC7450, MPC7451 and MPC7455: Remove R94 ; wire R88 right side pad to C85 right side (w/PMC hdr to left) For MPC7457: None; R94 is no-stuff. X4: R94 should connect to VDD; change component to make that clear.	X3	A

Version	Date	Changes
A	2003 May 5	Initial Errata
B	2003 Sep 9	Corrected errata #16 (note: boards have been built correctly, only the documentation was incorrect).



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