

### 1 General description

The FS26 is a power system basis chip (Power SBC) designed for low and mid-end micro controllers units. It features advance power managment conversion to support battery voltage from 3.2 V up to 40 V.

System level power is provided with a high efficiency buck controller, two programmable LDOs, a high precision voltage reference and two voltage tracker with high voltage protection to support loads off-module.

The FS26 features fully indepenent and configurable functional safety state machine with up to two fail-safe outputs and system level monitoring mechanism to reach a high integrity safety level targeting system up to ASIL-D. Electrical characteristics are maintained in the FS26 data sheet

### 2 Features and benefits

- High voltage boost converted supporting front-end or independent operation
- One high voltage buck pre-regulator with low power mode support
- One high efficiency buck regulator for MCU core voltage support
- Two linear regulators with low power mode support
- High precission 1% accurate voltage reference
- Two Voltage tracking regulator with high voltage protection for off-module load support
- Fully independent safety state machine with monitoring mechanism targeting ASIL-B applications
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Selectable wake-up sources to bring the system back from low power modes
- Two configurable GPIO pins
- 10 MHz SPI communication interface

### 3 Applications

- Automotive motor control / gate driver systems
- 48 V battery systems
- Hybrid battery systems
- Electric vehicle battery systems
- Body controller systems



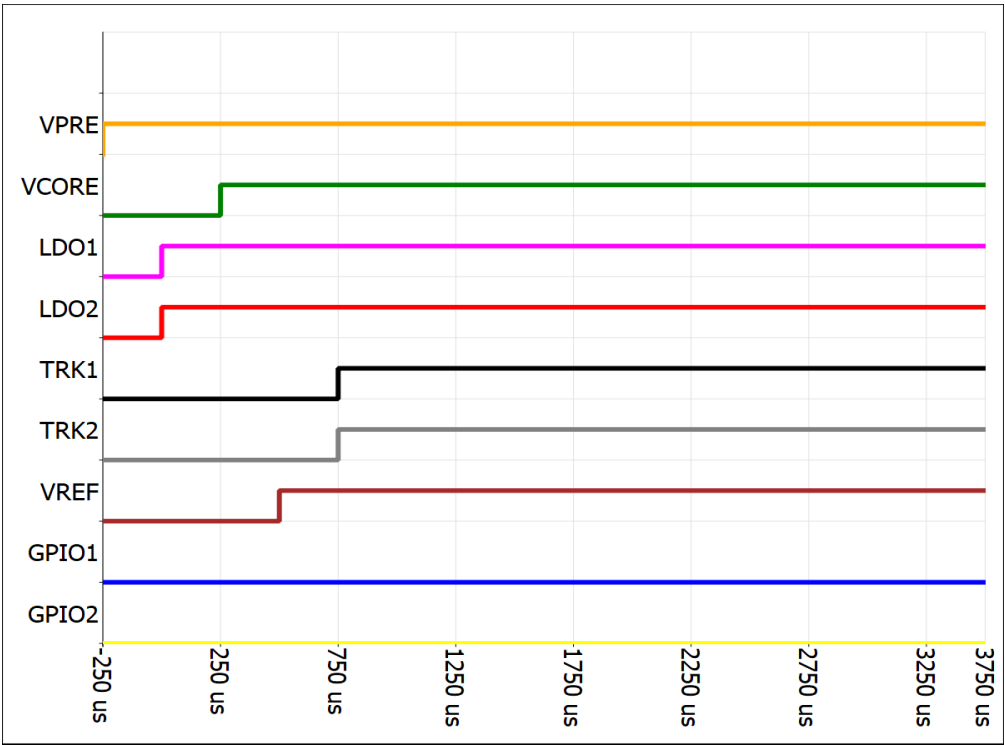
4 Ordering information

Table 1. Ordering information

| Type number <sup>[1]</sup> | Package   |   |           |
|----------------------------|-----------|---|-----------|
|                            | Name      | Description   | Version   |
| SFS2633AMDG6AD             | LQFP48 AE | HLQFP48-EP plastic thermally enhanced low profile quad flat package. 48 terminals; 0.5mm pitch; 7 mm x 7 mm x 1.4 mm body | SOT1571-1 |

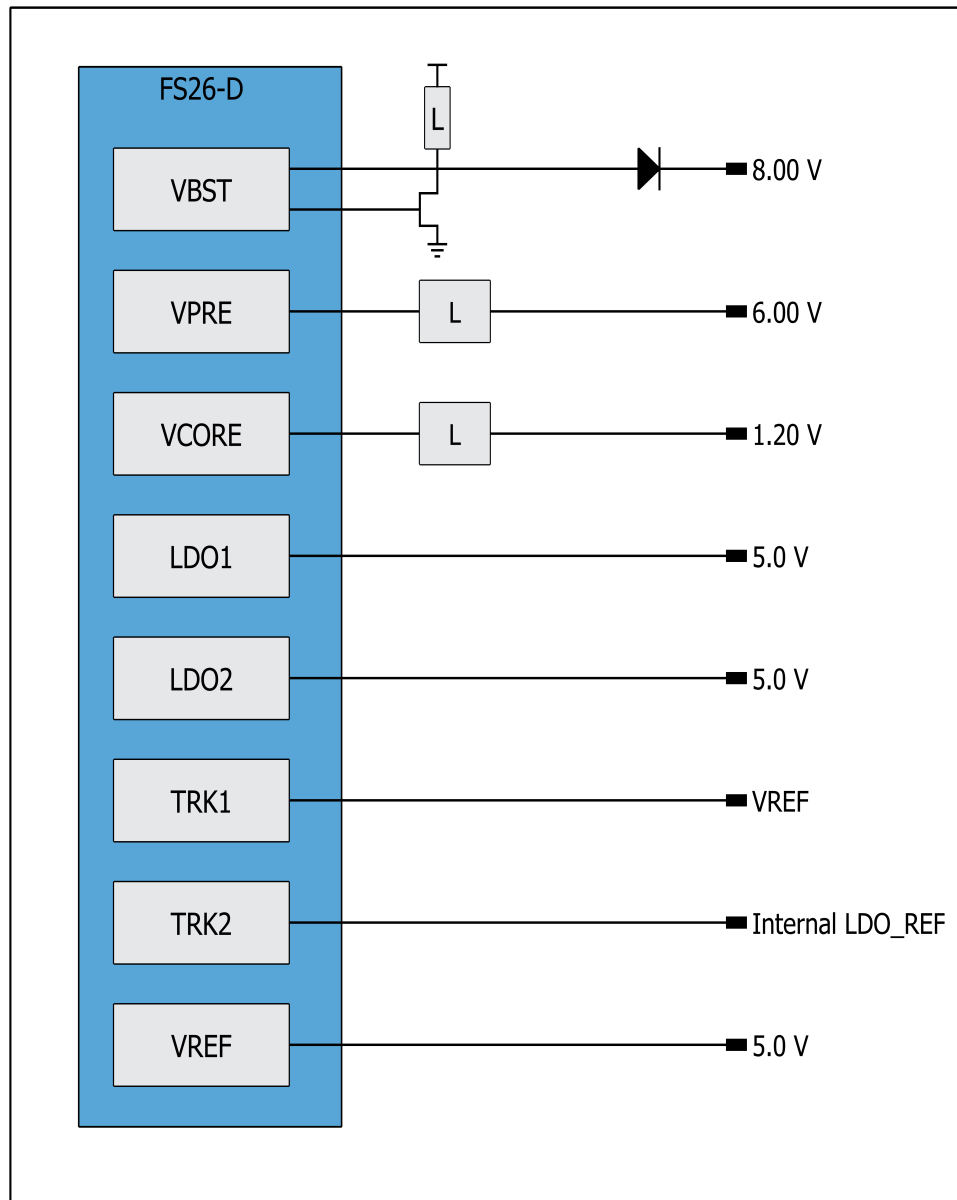
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

## 6 Hardware configuration diagram



## 7 OTP configuration

See FS26 datasheet for parametric details. The OTP configuration summary for G6 sequence ID is provided in Tables below.

**Table 2. Device OTP configuration**

| Functional block     | Feature                      | OTP selection                   |
|----------------------|------------------------------|---------------------------------|
| System configuration | VSUP UV Threshold            | 4.8 V/4.3 V                     |
|                      | Exit DFS On WAKE1 Event      | DFS Exit on Wake1 Event Enabled |
|                      | Auto-retry Power Up From DFS | Auto-retry Enabled              |
|                      | Auto-retry Mode              | Limited retry                   |
|                      | Auto-retry Timer Limit       | 800 ms                          |
|                      | Clock Frequency Selection    | 18 MHz                          |
|                      | VBOS Input Selection         | Auto Transition on VPRE_UVH     |
|                      | VBST Clock Selection         | 450 kHz                         |
| Power-up Sequence    | Power-up Slot Time           | 250 us                          |
|                      | Power-up Slot Bypass         | Bypass Disabled                 |
|                      | VCORE Power-up Slot          | Slot 1                          |
|                      | LDO1 Power-up Slot           | Slot 0                          |
|                      | LDO2 Power-up Slot           | Slot 0                          |
|                      | TRK1 Power-up Slot           | Slot 3                          |
|                      | TRK2 Power-up Slot           | Slot 3                          |
|                      | VREF Power-up Slot           | Slot 2                          |
|                      | GPIO1 Power-up Slot          | OFF                             |
|                      | GPIO2 Power-up Slot          | OFF                             |
| I/O Configuration    | GPIO1 Configuration          | GPIO1 configured as an Input    |
|                      | GPIO1 Low Side Polarity      | GPIO1 LS active high            |

## Configuration report for FS26-D OTP program ID: G6 rev A

|  |                           |                                    |
|--|---------------------------|------------------------------------|
|  | GPIO1 Pull-up             | Pull-Up Disabled                   |
|  | GPIO1 Pull-down           | Pull-Down Enabled                  |
|  | GPIO1 Detection Threshold | High voltage threshold             |
|  | GPIO1 TSD Pull-down       | Pull-down enabled in TSD           |
|  | GPIO2 Configuration       | GPIO2 configured as an Input       |
|  | GPIO2 Low Side Polarity   | GPIO2 LS active high               |
|  | GPIO2 VCORE PGOOD         | GPIO2 is not driven by VCORE PGOOD |
|  | GPIO2 Pull-up             | Pull-Up Disabled                   |
|  | GPIO2 Pull-down           | Pull-Down Enabled                  |
|  | GPIO2 Detection Threshold | High voltage threshold             |
|  | WAKE1 Detection Threshold | High voltage threshold             |
|  | WAKE2 Detection Threshold | High voltage threshold             |
|  | WAKE1 Pull-down           | Pull-Down Enabled                  |
|  | WAKE2 Pull-down           | Pull-Down Enabled                  |
|  | WAKE1 Pull-down Selection | 200 kOhm                           |
|  | WAKE2 Pull-down Selection | 200 kOhm                           |

Table 3. Switching Regulators

| Functional block   | Feature                | OTP selection |
|--------------------|------------------------|---------------|
| VPRE Configuration | VPRE In Normal Mode    | 6.00 V        |
|                    | VPRE In Standby Mode   | 5.35 V        |
|                    | DVS Ramp Rate          | 11 mV/us      |
|                    | VPRE Over Current Flag | 2.2 A         |
|                    | Over Current Deglitch  | 2000 us       |
|                    | Soft-start Ramp        | 2150 us       |

## Configuration report for FS26-D OTP program ID: G6 rev A

|                    |                         |                             |
|--------------------|-------------------------|-----------------------------|
|                    | VPRE Power Down Delay   | 100 us                      |
|                    | VPRE Transition Voltage | 5.35 V                      |
|                    | VPRE Phase Delay        | No delay                    |
|                    | VPRE LX Slew Rate       | Slow mode                   |
|                    | Transconductance Amp    | 15 uS                       |
|                    | Comp Capacitance        | 23.0 pF                     |
|                    | Comp Resistance         | 1137 kOhm                   |
|                    | Slope Compensation      | 266 mV/us                   |
|                    | Minimum On Time In PFM  | 1125 ns                     |
|                    | Minimum Off Time In PFM | 720 ns                      |
|                    | VPRE Clock Selection    | FSW/40                      |
|                    | TSD Behavior            | Go to DFS                   |
|                    | TSD Pull-down           | Pull-down enabled in TSD    |
|                    |                         |                             |
| VBST Configuration | VBST Voltage            | 8.00 V                      |
|                    | VBST Configuration      | Front-end boost             |
|                    | VBSTFB OV Monitor Mode  | Auto-enable mode            |
|                    | Phase Delay             | 1 Clock Cycle               |
|                    | Low-side Slew Rate      | PU = 1.5 Ohm / PD = 1.0 Ohm |
|                    | Minimum TON             | 200 ns                      |
|                    | VBST Soft Start         | 425 us                      |
|                    | Max Duty-cycle          | 87.50 %                     |
|                    | Comp Capacitance        | 200 pF                      |
|                    | Comp Transconductance   | 3.9 uS                      |
|                    | Comp Resistance         | 500 kOhm                    |

## Configuration report for FS26-D OTP program ID: G6 rev A

|                     |                      |                                  |
|---------------------|----------------------|----------------------------------|
|                     | Current Limit        | 150 mV/RSNS                      |
|                     | Slope Compensation   | 155 mV/us                        |
| VCORE Configuration | VCORE Voltage        | 1.20 V                           |
|                     | Control Type         | Valley mode control              |
|                     | Operating Mode       | CCM only                         |
|                     | Soft Start           | 10 mV/us                         |
|                     | VCORE Current Limit  | 3.4 A                            |
|                     | Phase Delay          | 2 Clock Cycles                   |
|                     | High-side Slew Rate  | Rise = 4.5 V/ns; Fall = 1.2 V/ns |
|                     | Transconductance Amp | 26 uS                            |
|                     | Comp Capacitance     | 50 pF                            |
|                     | Comp Resistance      | 150 kOhm                         |
|                     | VCORE Inductor       | 1 uH                             |
|                     | TSD Behavior         | Go to DFS                        |
|                     | TSD Pull-down        | Pull-down enabled in TSD         |

Table 4. Regulators

| Functional block    | Feature                 | OTP selection            |
|---------------------|-------------------------|--------------------------|
| LDO1 configurations | LDO1 Voltage In Normal  | 5.0 V                    |
|                     | LDO1 Voltage In Standby | 5.0 V                    |
|                     | LDO1 In Standby Mode    | LDO1 Enabled             |
|                     | TSD Behavior            | LDO1 disabled only       |
|                     | TSD Pull-down           | Pull-down enabled in TSD |
| LDO2 configurations | LDO2 Voltage In Normal  | 5.0 V                    |
|                     | LDO2 Voltage In Standby | 5.0 V                    |

## Configuration report for FS26-D OTP program ID: G6 rev A

|                     |                        |                          |
|---------------------|------------------------|--------------------------|
|                     | LDO2 In Standby Mode   | LDO2 Enabled             |
|                     | TSD Behavior           | LDO2 disabled only       |
|                     | TSD Pull-down          | Pull-down enabled in TSD |
| VREF configurations | VREF Voltage           | 5.0 V                    |
|                     | Internal LDO Reference | 3.3 V                    |
| TRK1 configurations | TRK1 Input Selection   | VREF                     |
|                     | TSD Behavior           | TRK1 disabled only       |
|                     | TSD Pull-down          | Pull-down enabled in TSD |
| TRK2 configurations | TRK2 Input Selection   | Internal LDO_REF         |
|                     | TSD Behavior           | TRK2 disabled only       |
|                     | TSD Pull-down          | Pull-down enabled in TSD |

Table 5. Voltage Monitoring

| Functional block       | Feature                     | OTP selection |
|------------------------|-----------------------------|---------------|
| VMONPRE Configuration  | VPRE Monitoring Voltage     | 6.00 V        |
|                        | VPRE OV Threshold           | 110.0 %       |
|                        | VPRE UV Threshold           | 90.0 %        |
|                        | VMONPRE OV Deglitch         | 45 us         |
|                        | VMONPRE UV Deglitch         | 40 us         |
| VMONLDO1 Configuration | LDO1 Monitoring Voltage     | 5.0 V         |
|                        | LDO1 OV Threshold           | 107.0 %       |
|                        | LDO1 UV Threshold           | 93.0 %        |
|                        | LDO1 Degraded UV Monitoring | Normal UV     |
|                        | VMONLDO1 OV Deglitch        | 45 us         |
|                        | VMONLDO1 UV Deglitch        | 40 us         |



Configuration report for FS26-D OTP program ID: G6 rev A

|                        |                             |                                 |
|------------------------|-----------------------------|---------------------------------|
|                        | LDO1 Pin Lift Detection     | LDO1 pin lift detection enabled |
| VMONTRK1 Configuration | TRK1 Monitoring Voltage     | 5.0 V                           |
|                        | TRK1 OV Threshold           | 107.0 %                         |
|                        | TRK1 UV Threshold           | 93.0 %                          |
|                        | VMONTRK1 OV Deglitch        | 45 us                           |
|                        | VMONTRK1 UV Deglitch        | 40 us                           |
| VMONCORE Configuration | VCORE Monitoring Voltage    | 1.20 V                          |
|                        | CORE OV Threshold           | 106.0 %                         |
|                        | CORE UV Threshold           | 94.0 %                          |
|                        | VMONCORE OV Deglitch        | 45 us                           |
|                        | VMONCORE UV Deglitch        | 40 us                           |
| VMONLDO2 Configuration | LDO2 Monitoring Voltage     | 5.0 V                           |
|                        | LDO2 OV Threshold           | 107.0 %                         |
|                        | LDO2 UV Threshold           | 93.0 %                          |
|                        | LDO2 Degraded UV Monitoring | Normal UV                       |
|                        | VMONLDO2 OV Deglitch        | 45 us                           |
|                        | VMONLDO2 UV Deglitch        | 40 us                           |
|                        | LDO2 Pin Lift Detection     | LDO2 pin lift detection enabled |

## Configuration report for FS26-D OTP program ID: G6 rev A

|                        |                            |                                 |
|------------------------|----------------------------|---------------------------------|
| VMONTRK2 Configuration | TRK2 Monitoring Voltage    | 3.3 V                           |
|                        | TRK2 OV Threshold          | 107.0 %                         |
|                        | TRK2 UV Threshold          | 93.0 %                          |
|                        | VMONTRK2 OV Deglitch       | 45 us                           |
|                        | VMONTRK2 UV Deglitch       | 40 us                           |
| VMONEXT Configuration  | External VMON OV Threshold | 108.0 %                         |
|                        | External VMON UV Threshold | 92.0 %                          |
|                        | VMONEXT OV Deglitch        | 45 us                           |
|                        | VMONEXT UV Deglitch        | 40 us                           |
| VMONREF Configuration  | VREF Monitoring Voltage    | 5.0 V                           |
|                        | VREF OV Threshold          | 104.5 %                         |
|                        | VREF UV Threshold          | 95.5 %                          |
|                        | VMONREF OV Deglitch        | 45 us                           |
|                        | VMONREF UV Deglitch        | 40 us                           |
|                        | VREF Pin Lift Detection    | VREF pin lift detection enabled |

## Configuration report for FS26-D OTP program ID: G6 rev A

Table 6. System Safety Configuration

| Functional block            | Feature                          | OTP selection                    |
|-----------------------------|----------------------------------|----------------------------------|
| ABIST1 Configuration        | ABIST1 On VMONPRE                | ABIST1 Enabled                   |
|                             | ABIST1 On VMONCORE               | ABIST1 Enabled                   |
|                             | ABIST1 On VMONLDO1               | ABIST1 Enabled                   |
|                             | ABIST1 On VMONLDO2               | ABIST1 Enabled                   |
|                             | ABIST1 On VMONTRK1               | ABIST1 Enabled                   |
|                             | ABIST1 On VMONTRK2               | ABIST1 Enabled                   |
|                             | ABIST1 On VMONREF                | ABIST1 Enabled                   |
|                             | ABIST1 On VMONEXT                | ABIST1 Disabled                  |
| System Safety Configuration | DFS Entry Mode                   | Go to DFS when FLT_ERR_CNT = max |
|                             | FS1B Assertion Mode              | Delayed Assertion Enabled        |
|                             | RSTB Delay From FS0B             | 0 us                             |
|                             | RSTB Low Detection Timer         | 8 Second Timer Enabled           |
|                             | Watchdog Timer                   | WD Timer Enable                  |
|                             | Bypass LBIST From Standby        | Always perform LBIST             |
|                             | Main DFS Availability            | Deep Fail Safe Available         |
|                             | Deep Failsafe State Availability | Deep Fail Safe Available         |

Table 7. OTP ID

| Functional block | Feature         | OTP selection |
|------------------|-----------------|---------------|
| OTP Program ID   | Program ID High | G             |
|                  | Program ID Low  | 6             |

## Configuration report for FS26-D OTP program ID: G6 rev A

|                    |                         |                          |
|--------------------|-------------------------|--------------------------|
| Main Version Bits  | LDO2 Regulator          | LDO2 available           |
|                    | VCORE Regulator         | CORE available           |
|                    | TRK1 Regulator          | TRK1 available           |
|                    | TRK2 Regulator          | TRK2 available           |
|                    | VREF Regulator          | VREF available           |
|                    | VBST Regulator          | VBST available           |
|                    | GPIO1 Pin               | GPIO1 available          |
|                    | GPIO2 Pin               | GPIO2 available          |
|                    | LDT Function            | LDT available            |
|                    | TWARN Selection         | 155 °C                   |
|                    | VCORE Max Current       | 1650 mA                  |
|                    | Device ID               | 0x20                     |
|                    |                         |                          |
| FS Versioning Bits | VPRE Monitor            | VMON Enabled             |
|                    | VCORE Monitor           | VMON Enabled             |
|                    | LDO1 Monitor            | VMON Enabled             |
|                    | LDO2 Monitor            | VMON Enabled             |
|                    | TRK1 Monitor            | VMON Enabled             |
|                    | TRK2 Monitor            | VMON Enabled             |
|                    | VREF Monitor            | VMON Enabled             |
|                    | External Monitor        | VMON Disabled            |
|                    | FCCU Function           | FCCU available           |
|                    | Fault Recovery Function | Fault Recovery available |
|                    | Watchdog Type           | Challenger WD            |
|                    | FS1B Type               | FS1B available           |
|                    |                         |                          |

Configuration report for FS26-D OTP program ID: G6 rev A

|  |                  |                      |
|--|------------------|----------------------|
|  | ABIST On-demand  | ABIST2 available     |
|  | Cyclic OTP Check | CORRUPT available    |
|  | ERRMON Function  | ERRMON not available |
|  | LBIST Operation  | LBIST available      |

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### Contents

|  |    |
|--|----|
| 1 General description .....            | 1  |
| 2 Features and benefits .....          | 1  |
| 3 Applications .....                   | 1  |
| 4 Ordering information .....           | 2  |
| 5 Power up sequence summary .....      | 2  |
| 6 Hardware configuration diagram ..... | 3  |
| 7 OTP configuration .....              | 4  |
| 8 Legal information .....              | 14 |

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