



SC33FS8500C1ES

Configuration report for FS8500 OTP program ID: C1 rev A

Rev 2.5 — 23-Apr-2025

Report

1 General description

The FS85/FS84 device family is developed in compliance with ASIL D process, FS84 is ASIL B capable and FS85 is ASIL D capable. All device options are pin to pin and software compatible.

The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

Note: All parametric information is maintained in FS84_FS85 datasheet

2 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on device options:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on device options:** low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 μ A typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.



NXP Semiconductors

SC33FS8500C1ES

Configuration report for FS8500 OTP program ID: C1 rev A

3 Applications

- Radar
- Vision
- ADAS domain controller
- Radio
- V2x

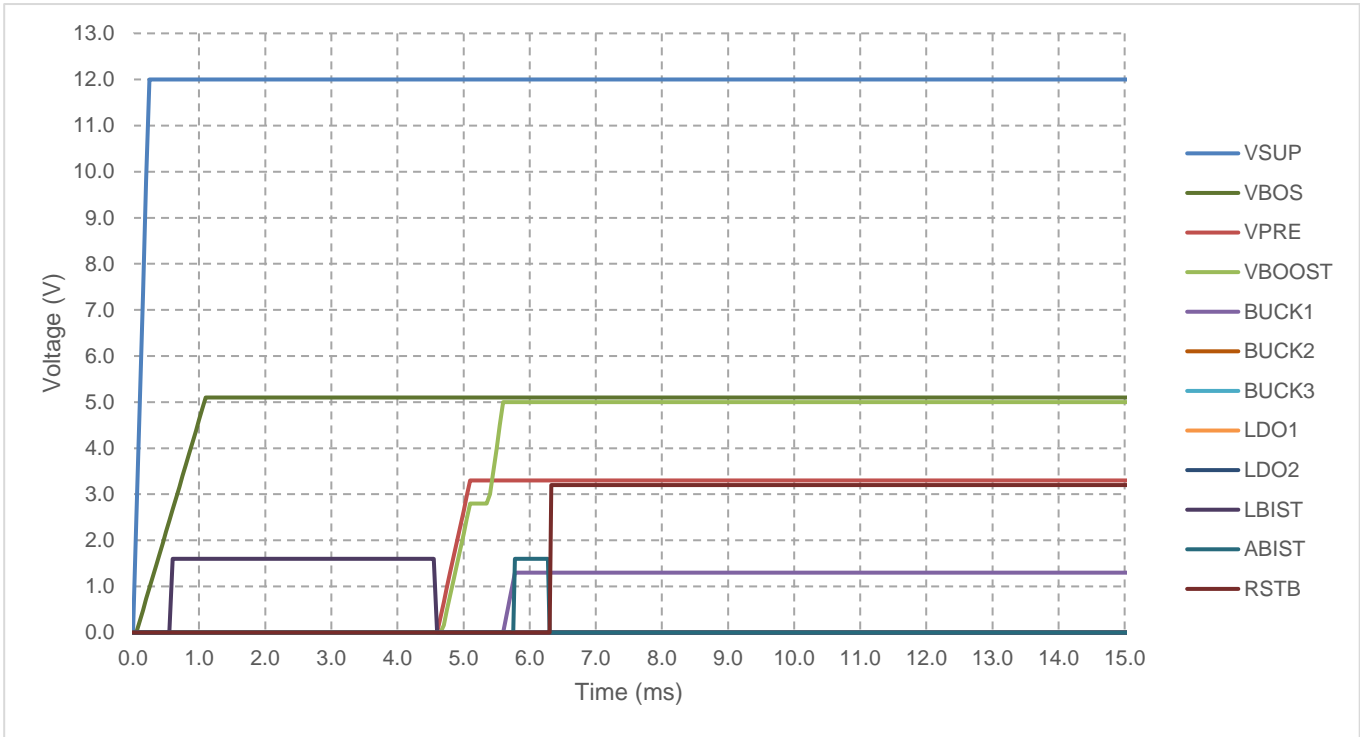
4 Ordering information

Table 1. Ordering Information

Type number ^[1]	Package		
	Name	Description	Version
SC33FS8500C1ES	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-23

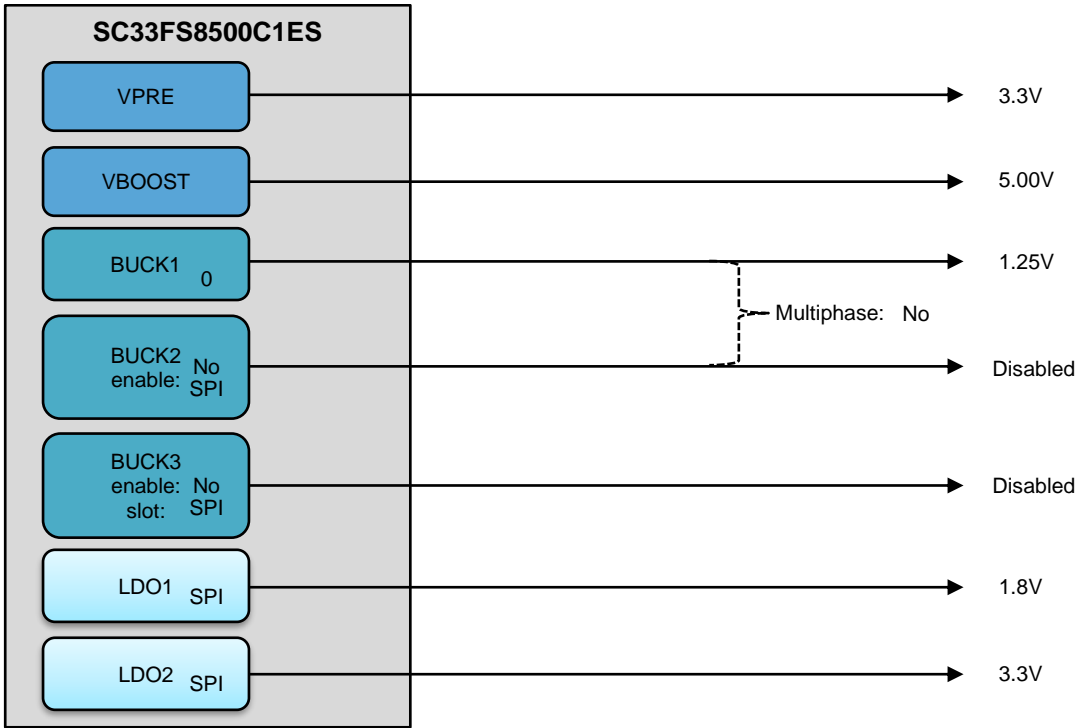
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power up sequence summary



Note: VBOS is set at 5.1 V and RSTB at 3.2 V or 4.9 V to differentiate from regulators on the graph

6 Hardware configuration diagram



7 OTP configuration

Table 2. Main OTP configuration

Functional block	Feature	OTP selection
VPRE	Output voltage	3.3V
	Slope compensation	100mV/μs
	Current limitation	50mV
	High Side slew rate	PU/PD/520mA
	Low Side slew rate	PU/PD/900mA
	Switching frequency	455KHz
	Phase shifting	delay 1
	Turn OFF delay	32ms
	VPRE mode	Force PWM

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
VBOOST	Enabled	Yes
	Output voltage	5.00V
	Slope compensation	160mV/μs
	Slew rate	500V/μs

	Compensation resistor	750kohms
	Compensation capacitor	125pF
	Switching frequency	2.22MHz
	Phase shifting	delay 1
	Behavior in case of TSD	BOOST Shutdown
BUCK1	Output voltage	1.25V
	Inductor	1µH
	Current limitation	4.5A
	Compensation network	48.75 GM
	Switching frequency	2.22MHz
	Phase shifting	delay 1
	Behavior in case of TSD	BUCK1 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 0
	Soft start ramp	7.81mV/µs
BUCK2	Enabled	No
	Output voltage	0.9V
	Inductor	1µH
	Current limitation	2.6A
	Compensation network	48.75 GM
	Switching frequency	2.22MHz
	Multiphase with Buck1	No
	Phase shifting	delay 1
	Behavior in case of TSD	BUCK2 Shutdown
	Power sequencing slot	Regulator does not Start (Enabled by SPI/I2C)
	Soft start ramp	7.81mV/µs

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
BUCK3	Enabled	No
	Output voltage	3.3V
	Inductor	1µH
	Current limitation	2.6A
	Compensation resistor	Default
	Gain control	Default
	Switching frequency	2.22MHz
	Phase shifting	delay 1
	Behavior in case of TSD	BUCK3 Shutdown

LDO1	Power sequencing slot	Regulator does not Start (Enabled by SPI/I2C)
	Soft start ramp	10.4mV/μs
	Output voltage	1.8V
	Current limitation	400mA
	Behavior in case of TSD	LDO1 Shutdown
LDO2	Power sequencing slot	Regulator does not Start (Enabled by SPI/I2C)
	Output voltage	3.3V
	Current limitation	400mA
	Behavior in case of TSD	LDO2 Shutdown
	Power sequencing slot	Regulator does not Start (Enabled by SPI/I2C)
Miscellaneous	Power up/down slot duration	250μs
	PSYNC	Disabled
	PLL enabled	No
	Deep Fail Safe (autoretry)	Infinite
	VSUP power-up threshold	4.9V for Vpre < 4.5V
	Regulator assigned to VDDIO	VPRE
	I2C address	0x20
	Device ID	00000001

Table 3. Fail-safe OTP configuration

Functional block	Feature	OTP selection
VCOREMON	Monitoring Voltage	1.25V
	OVTH	112%
	UVTH	88%
	OV_DGLT	45μs
	UV_DGLT	25μs
	SVS_CLAMP	No SVS

Table 3. Fail-safe OTP configuration (continued)

Functional block	Feature	OTP selection
VDDIOMON	Monitoring Voltage	3.3V
	OVTH	112%
	UVTH	88%
	OV_DGLT	45μs
	UV_DGLT	25μs
VMON1	OVTH	112%
	UVTH	88%
	OV_DGLT	45μs
	UV_DGLT	25μs
VMON2	OVTH	112%
	UVTH	88%
	OV_DGLT	45μs

VMON3	UV_DGLT	25µs
	OVTH	112%
	UVTH	88%
	OV_DGLT	45µs
	UV_DGLT	25µs
VMON4	OVTH	112%
	UVTH	88%
	OV_DGLT	45µs
	UV_DGLT	25µs
PGOOD	VCOREMON	Yes
	VDDIOMON	Yes
	VMON1	No
	VMON2	No
	VMON3	No
	VMON4	No
	RSTB	No
ABIST1	VCOREMON	Yes
	VDDIOMON	Yes
	VMON1	No
	VMON2	No
	VMON3	No
	VMON4	No

Table 3. Fail-safe OTP configuration (continued)

Functional block	Feature	OTP selection
Safety enable	VMON1	No
	VMON2	No
	VMON3	No
	VMON4	No
	FCCU	Yes
	ERRMON	No
	WATCHDOG	Challenger WD
	FLT_RECOVERY	Yes
I2C	I2C address	0x21

8 Legal information

8.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

8.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.

NXP Semiconductors

SC33FS8500C1ES

Configuration report for FS8500 OTP program ID: C1 rev A

Contents

1. General description	1
2. Features and benefits	1
3. Applications	2
4. Odering information	2
5. Power up sequence summary	2
6. Hardware configuration diagram	3
7. OTP configuration	3
8. Legal information	8

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2019.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

Date of release: 23-Apr-2025

Document identifier: R_SC33FS8500C1ES_Rev_A