

MVR5510AVMA6EP – NXP Standard

Configuration report for QM OTP program ID: A6 rev B

Rev. 1.0 - 7/23/2024

Report

1 General description

The VR5510 is a multi-output power management integrated circuit, with focus on Gateway, V2X and Infotainment applications. It includes multiple high efficiency switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The VR5510 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASILB and ASILD safety integrity level. It is developed in compliance with ISO 26262 standard.

2 Features and benefits

- 60 V DC maximum input voltage
- Configurable VPRE synchronous buck controller with external MOSFETs.
- Configurable Single/dual-Phase Low voltage buck converters with DVS capability
- Configurable Low voltage integrated synchronous BUCK3 converter
- BOOST converter with integrated low side switch
- 3x linear voltage regulators with configurable Output Voltage
- High voltage linear regulator (HVLDO) with LDO and Switch mode operation
- EMC optimization with frequency tuning, clock synchronization, frequency spread spectrum and slew rate control
- Low power standby mode (40 uA quiescent Current)
- 2x input pins for wake-up detection and battery voltage sense
- Device control via I2C interface with CRC (up to 3.4 MHz)
- Selectable OTP Default configuration

3 Applications

- Automotive Infotainment
- High - End Industrial

4 Ordering information

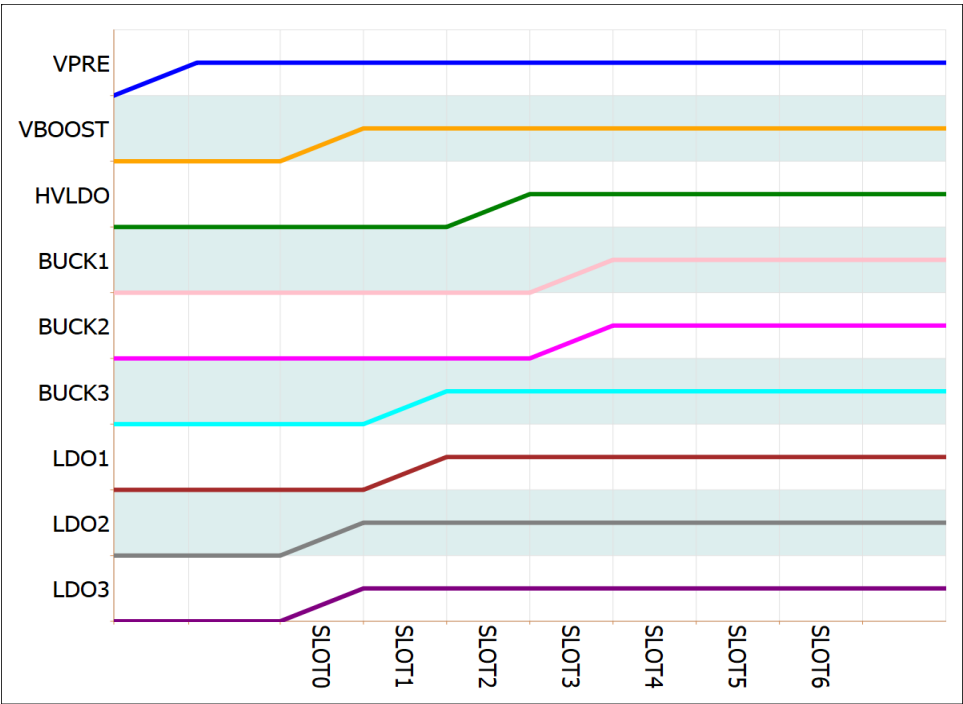
Table 1. Ordering information

| Type number ^[1] | Package | | |
|----------------------------|----------|--|-----------|
| | Name | Description | Version |
| MVR5510AVMA6EP | QFN56 EP | QFN56 plastic thermally enhanced very thin quad flat non-leaded package. Wettable flanks; 56 terminals; 0.5mm pitch, 8mmx8mmx0.85mm body | SOT684-21 |

[1] To order parts in tape and reel, add the R2 suffix to the part number.

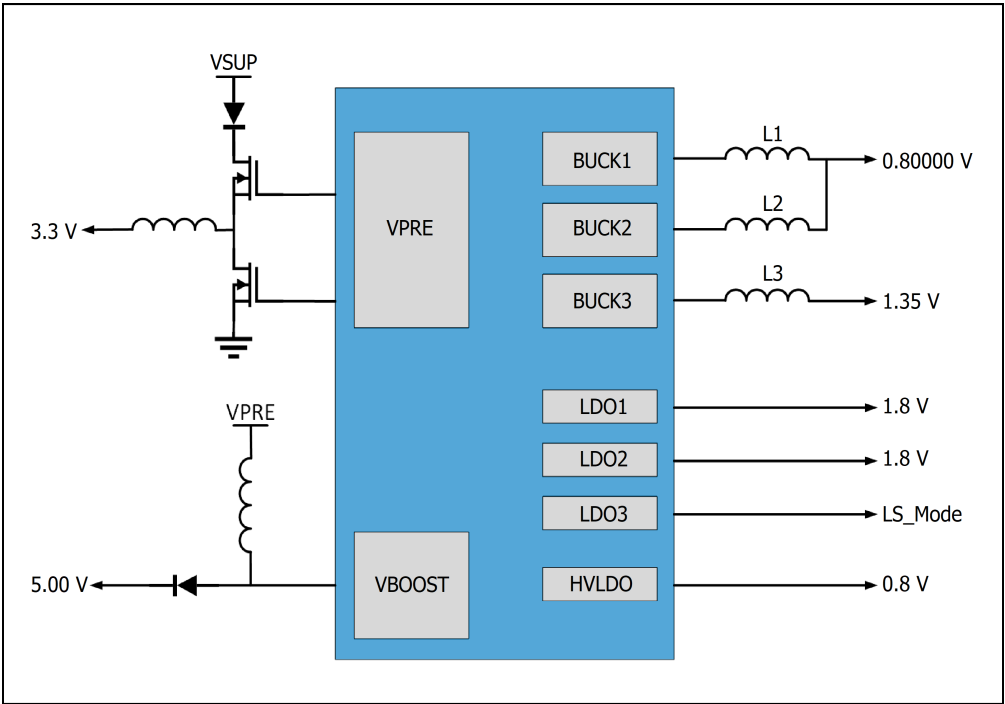


5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



7 OTP configuration

See VR5510 datasheet for parametric details. The OTP configuration summary for A6 sequence ID is provided in Tables below.

Table 2. Device OTP configuration

| Functional block | Feature | OTP selection |
|----------------------|--------------------------|--------------------------|
| Device Configuration | Main I2C Address | 0x20 |
| | VSUP UV threshold | 4.9 V |
| | Auto Re-try Enable | Enabled (default) |
| | Auto Re-try Timeout | 4 s (default) |
| | Number of Retries | Infinite Retry (default) |
| | PLL Enable | Disabled (default) |
| | Clock 1 Divider | 2.22 MHz (default) |
| | Clock 2 Divider | 455 KHz (default) |
| | Thermal Warning TH | 105 °C (default) |
| | Deep Sleep Enable | DSM Disabled (default) |
| IO Configuration | PWRON2 Control | Not Required |
| | AMUX/FOUT Select | AMUX Enabled (default) |
| | PSYNC Enable | PSYNC Disabled (default) |
| | PSYNC Mode | Sync 2 x VR5510 |
| | PSYNC Power Down Ctrl | Ignore for PwrDown |
| | Standby Transition Timer | Enabled (default) |
| | Standby Discharge TH | 75 mV (default) |
| | Standby Polarity | Active Low (default) |
| | Standby PGOOD Enable | Enabled (default) |
| | PSYNC PGOOD Ext | Disabled |

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| | | |
|--|--------------------------|----------------|
| | Ext Standby Discharge | Disabled |
| | Standby PGOOD Delay | 400 us |
| | VDDIO Supply Seletion | LDO3 (default) |
| | Multiphase Configuration | Dual Phase |

Table 3. Voltage Regulators Configuration

| Functional block | Feature | OTP selection |
|----------------------|--|-----------------------------------|
| VPRE Configuration | VPRE Voltage | 3.3 V (default) |
| | Slope Compensation | 41.4 mV/us |
| | VPRE Standby Output Ctrl | Set by VPREV_STBY (I2C) |
| | ILIM sense Voltage | 120 mV |
| | VPRE HighSide pull down Slew Rate Ctrl | PD/520 mA (455 KHz default value) |
| | VPRE HighSide pull up Slew Rate Ctrl | PU/520 mA (455 KHz default value) |
| | VPRE LowSide Slew Rate Ctrl | PU/PD/900 mA (default value) |
| | Soft Start Ramp | 2 mV/us (default) |
| | VPRE Off Time | 80 ns |
| | TON in PFM | 550 ns (default value) |
| | TON Min | 45 ns |
| | Turn OFF Delay | 250 us |
| VBOOST Configuration | VBOOST Voltage | 5.00 V (default) |
| | Slope Compensation | 67 mV/us (default) |
| | Minimum TON | 60 ns (default) |
| | Current Limit | 2.25 A (default) |
| | Low Side Slew Rate Ctrl | 500 V/us (default) |
| | Input Path to BOS | Enabled (default) |

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| | | |
|--|------------------------|--------------------|
| | Compensation Capacitor | 125 pF (default) |
| | Compensation Resistor | 500 KOhm (default) |

Table 4. BUCK Regulators

| Functional block | Feature | OTP selection |
|----------------------|--------------------|--|
| BUCK1/2 - Dual Phase | Output Voltage | 0.80000 V |
| | Current Limit | 3.6 A |
| | Output Inductor | 1 uH(default) |
| | Transconductance | 65 umho |
| | DVS Ramp of BUCK12 | 15.6 mV/us (power up) / 10.41 mV/us (power down) |
| BUCK3 | Output Voltage | 1.35 V |
| | Current Limit | 3.6 A |
| | Output Inductor | 1 uH(default) |
| | R Comp | 56 KOhm |
| | Ramp | 3.47 mV/us (power up/down) |
| | Transconductance | 65 umho |

Table 5. LDO Regulators

| Functional block | Feature | OTP selection |
|------------------|----------------|-----------------------|
| LDO1 Regulator | Output Voltage | 1.8 V |
| | Current Limit | 400 mA (default) |
| LDO2 Regulator | Output Voltage | 1.8 V |
| | LDO Mode | LDO Mode (default) |
| LDO3 Regulator | Output Voltage | LS_Mode |
| | LDO Mode | Load Switch (default) |

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Table 6. HVLDO Regulator

| Functional block | Feature | OTP selection |
|------------------|------------------|---|
| HVLDO Regulator | HVLDO Voltage | 0.8 V (default) |
| | Transition Mode | Switch in Normal / LDO in Standby (default) |
| | Sequence Control | Follows HVLDO_OTP slot |

Table 7. Voltage Sequence and Timing Configuration

| Regulator | Sequence | Enabled | Phase Delay | Clock | TSD Event |
|------------|--------------|---------|---------------|-------|----------------|
| VPRE | Auto-enabled | Enabled | No delay | CLK2 | |
| VBOOST | Slot 0 | Enabled | No delay | CLK1 | Shutdown + DFS |
| BUCK1 | Slot 3 | Enabled | 1 clock delay | CLK1 | Shutdown + DFS |
| BUCK2 | Slot 3 | Enabled | 2 clock delay | CLK1 | Shutdown + DFS |
| BUCK3 | Slot 1 | Enabled | 3 clock delay | CLK1 | Shutdown + DFS |
| LDO1 | Slot 1 | Enabled | | | Shutdown + DFS |
| LDO2 | Slot 0 | Enabled | | | Shutdown + DFS |
| LDO3 | Slot 0 | Enabled | | | Shutdown + DFS |
| HVLDO | Slot 2 | Enabled | | | Shutdown + DFS |
| SLOT Width | 250 us | | | | |

Table 8. Safety State Machine Configuration

| Functional block | Feature | OTP selection |
|----------------------|--------------------------|------------------------------|
| Safety Configuration | FailSafe I2C Address | 0x21 |
| | 8sec Timer to DFS | Timer Disabled |
| | ABIST1 to RSTB delay | 5 ms Delay |
| | VCOREMON SVS Clamp Limit | 16 steps available (default) |
| | VCOREMON SVS Offset Type | Negative offset (default) |

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| | | |
|--|------------------------|---|
| | PGOOD assert with RSTB | PGOOD Asserts with RSTB Fault (default) |
| | HVLDO Mode Select | Switch Mode (default) |
| | WDI Polarity | Falling Edge |
| | WDI on FCCU1 | WDI Disabled (default) |
| | STANDBY Mode | STANDBY Enabled (default) |
| | STANDBY Polarity | Active Low in standby mode (default) |
| | STANDBY Request Path | I2C + STBY Pin Transition (default) |
| | STANDBY Window | STBY Window Enabled (default) |
| | WD Init Timeout | 1024 ms |
| | Fault Recovery Mode | Disabled |
| | WD Selection | Simple WD |
| | WD Monitoring | WD Disabled |
| | FCCU Monitoring | FCCU Disabled |
| | LBIST Enable | LBIST Disabled |

Table 9. Voltage Monitoring

| | VMONEN | Voltage | UV_TH | OV_TH | UV Dbnc | OV Dbnc | PGOOD Ctrl | ABIST Ctrl |
|----------|---------|-----------|--------|-------|---------|---------|----------------|-------------------|
| VCOREMON | Enabled | 0.80000 V | 95.5 % | 106 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |
| VDDIOMON | Enabled | 3.3 V | 95 % | 105 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |
| HVLDOMON | Enabled | 0.8 V | 93 % | 107 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |
| VMON1 | Enabled | 0.8 V | 95.5 % | 106 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |
| VMON2 | Enabled | 0.8 V | 96.5 % | 105 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |

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| | | | | | | | | |
|-------|---------|-------|------|-------|-------|-------|-------------------|----------------------|
| VMON3 | Enabled | 0.8 V | 95 % | 105 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |
| VMON4 | Enabled | 0.8 V | 95 % | 105 % | 25 us | 25 us | PGOOD Assigned | No ABIST at PWRUP |

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