

Freescale Semiconductor Release Note

P2ETYPEERN_0_0_3 Jan 22, 2010 Rev. 2

PPP to Ethernet Type E Interworking RAM Package Release 0.0.3

General

This release note reflects differences between the *QUICC Engine*TM *Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, and the features which are available for this device using the provided microcode RAM packages. The following release note reveals any exceptions to the features which are specified in this release of the specification. The notes describe any addition to the specification or any missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: MLMC PPP, Ethernet, Interworking and IP Reassembly and IEEE Std. 1588TM support. Features of these core blocks that are not supported in this package are described in Table 3.





Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8360 rev 2.1	iw_pe_type_e_mpc8360_r2.1.h
MPC8568 rev 1.1	iw_pe_type_e_mpc8568_r1.1.h



Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine*TM *Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3. The tables designate additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine*TM *Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (Which are not Described in QEIWRM, Rev 3)

Feature	Comments
None	

Table 3. Removed Features (Described in QEIWRM, Rev 3 but Not Supported)

Feature	Comments	QEIWRM, Rev 3
Header manipulation in termination mode Insert/remove/replace VLAN	REMODER[VTagOP] and REMODER[VNonTagOP] (in RxGPRAM) are not supported.	Section 8.5.3.9, "Rx Ethernet Mode Register (REMODER)"
	TAD[VTagOP] and TAD[VNonTagOP] are not supported.	Section 8.6.2.6.5, "Termination Action Descriptor (TAD)"
LPM PCD		Section 30.3.2.4, "Longest Prefix Match (LPM) PCD"
Expanded Hash Table		Section 30.5.3.3.1, "TableLookup_FourWayHa sh PCD"
VLAN Specific Header Manipulation Command Descriptor		Section 31.1.11.2, "VLAN Specific Header Manipulation Command Descriptor,
CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes		Section 30.5.3.1.1, "CAM Emulation Lookup Table (CELUT) for LookupKey Size of 2 Bytes"
IPHCoE		Section 31.1.11.18, "Ethernet IP/UDP Header Decompression Command Descriptor (HDCD)," Section 34.4.1.1.2, "Compression of Frames Transmitted on Ethernet Links," and Section 34.4.2.2, "Decompression of PPPoE Frames Received on Ethernet Links"

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Table 3. Removed Features (Described in QEIWRM, Rev 3 but Not Supported)

Feature	Comments	QEIWRM, Rev 3
Hierarchical Scheduler		Section "8.4.17 Hierarchical Scheduling Support"
PPP Mux		Section 25.9 PPP Mux Process
IP fragmentation	Tx Global Parameter RAM TEMODER bit 8 is not supported.	Section "8.5.3.3 Tx Global Parameter RAM"



Revision History

Table 4. Revision History for Release 0.0.3

Release Date: Jun 9, 2009 Revision Register Number: 0xBBE0E003	
New Features	This package contains performance optimizations for the ML/MC PPP Tx Back-End process.
	ML/MC PPP, Flush WBD command for flushing the WBD for a given class. This command can be used when the host is interested in limiting the time spent by the fragments in the WBD ring.
Removed Features	None
Bug Fixes	ML/MC PPP, for links under bundle configured in interworking mode, short fragments with 24 bit sequence number are not handled correctly.
	ML/MC PPP, packets can be lost in ML/MC receive process due to synchronization issue between front-end and back-end tasks.

Table 5. Revision History for Release 0.0.2

Release 0.0.2 Revision Register value 0xBBE0E002		
New Features	Race condition on class interrupt queue can cause some interrupt entries to be lost.	
	Using aging for external hash tables might introduce a SDMA error exception.	
	MLMC PPP transmits illegal HDLC frames when ACFC enabled and PID in buffer. In such a case illegal data is being transmitted.	
	The number of PPP IW CPU queues were increased from four to eight.	
Bug Fixes	This package introduces enhancements for PPP Tx bandwidth use optimization.	
	The number of PPP IW CPU queues were increased from four to eight.	
	New counter on IP Decompressor Statistics table - "Total bytes in error frames". Counts the total bytes in frames that are not decompressed due to errors.	
	New counter on IW Special Statistics table (IWCS) - "DQ_DroppedByte_Cnt". Counts the total bytes in frames that are dropped due to reasons related to IW destination queue.	

Table 6. Revision History for Release 0.0.1

Release 0.0.1 Revision Register value 0xCEBEE001	
New Features	First version
Bug Fixes	First version

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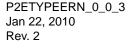
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