

P1021 Type A Instruction RAM Microcode Package Release 0.0.0

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, and the features which are available for this device using the provided microcode Instruction RAM (IRAM) packages. The following release note reveals any exceptions to the features which are specified in this release of the specification. The notes also describe any addition to the specification or any missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: ATM Termination (AAL0 and AAL5), Ethernet Termination (10/100/1000), Ethernet Parser, asynch HDLC, IP fragmentation, SPI, HDLC, USB, UART, BISYNC and UMCC.

Limited interworking (IW) capabilities were added that allow parse, lookup and forward of frames to CPU only or reject.

It is possible to configure Ethernet and PPP to operate in IW mode but under the following limitations:

Parser:

- Parser interrupts are not allowed. Meaning that (HIE, MIE, UIE and LIE) must be cleared

Ethernet:

- IW forwarding to ENET is not available. Usage of IWAD is not allowed. TAD is the only possible configuration.
- No IWCT/HM/IWCS support, meaning that IWCT index on TAD and IWAD must be zero.

Features of these core blocks that are not supported in this package are described in [Table 3](#).

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

| Device | Loader file name (.h) |
|-------------------------------|-----------------------|
| P1021 rev 1.0 | iram_P1021_Type_A.h |

Package Content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3. The tables below show additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM, Rev 3, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (which are not Described in QEIWRM, Rev 3)

| Feature | Comments |
|---------|----------|
| None | |

Table 3. Removed Features (Described in QEIWRM, Rev 3 but Not Supported)

| Feature | Comments | QEIWRM, Rev 3 |
|----------------------|----------|---|
| LPM PCD | | Section 30.3.2.4, "Longest Prefix Match (LPM) PCD" |
| Protocol IW Function | | Chapter 31, "Protocol Interworking Programming Model" |
| ATM AAL2 | | Chapter 12, "ATM Adaptation Layer 2" |
| IP Reassembly | | Chapter 33, "IP Reassembly" |
| Virtual Port | | Chapter 32, "Virtual Port" |
| IMA and IMA counters | | Chapter 27, "Inverse Multiplexing for ATM" |
| Serial ATM | | Chapter 26, "Serial ATM Microcode" |
| ATM AAL1 CES | | Chapter 28, "ATM AAL1 Circuit Emulation Service" |
| ATM AAL1 | | Chapter 11, "ATM Controller AAL0, AAL1, and AAL5" |

Revision History

Table 4. Revision History for Release 0.0.0

| Release Date: Jan 6, 2010 Revision Register Number: 0xB100A000 | |
|---|------------------------|
| New Features | None. Initial Release. |
| Removed Features | None. Initial Release. |
| Bug Fixes | None. Initial Release. |

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