Migrating from PowerQUICC II Pro to QorIQ's P1010

Technical Details

January 2012

Session Objectives

- Provide overview and highlight the new features introduced with the QorIQ P1010 family of processors
- Provide the detail and guidance on migrating designs from PowerQUICC II Pro to the QorIQ P1010 family

Contents

- Introduction to P1010 QorIQ Platforms
- Challenges of Migration
- Device Features
- Hardware Design Guide
- Software Design Guide
  - Code migration
  - Migration to dual core
- Application Study

Introducing Freescale's QorIQ platforms

- Designed to enable the development of the next era of networking applications by delivering:
  - Improved processing performance—high-performance Power Architecture® based multicore solutions
  - Power efficiency—45 nm process technology for industry-leading power-to-performance solution
  - Programmability—programming tools, ecosystem partners, common software and pin-compatible processors
    - Note that the P1010/P1014 family of products is not pin-compatible with the rest of the P1 or P2 family

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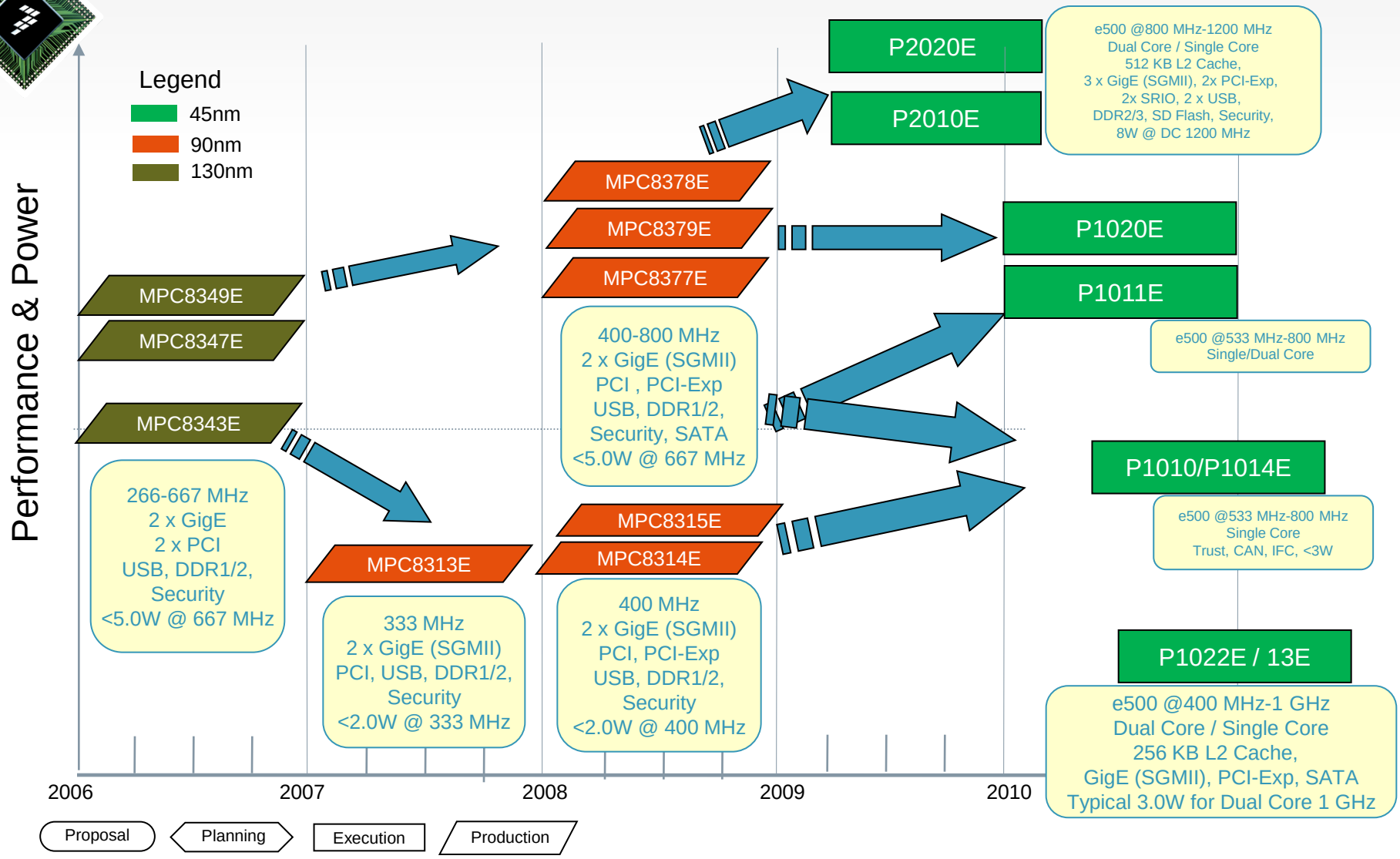
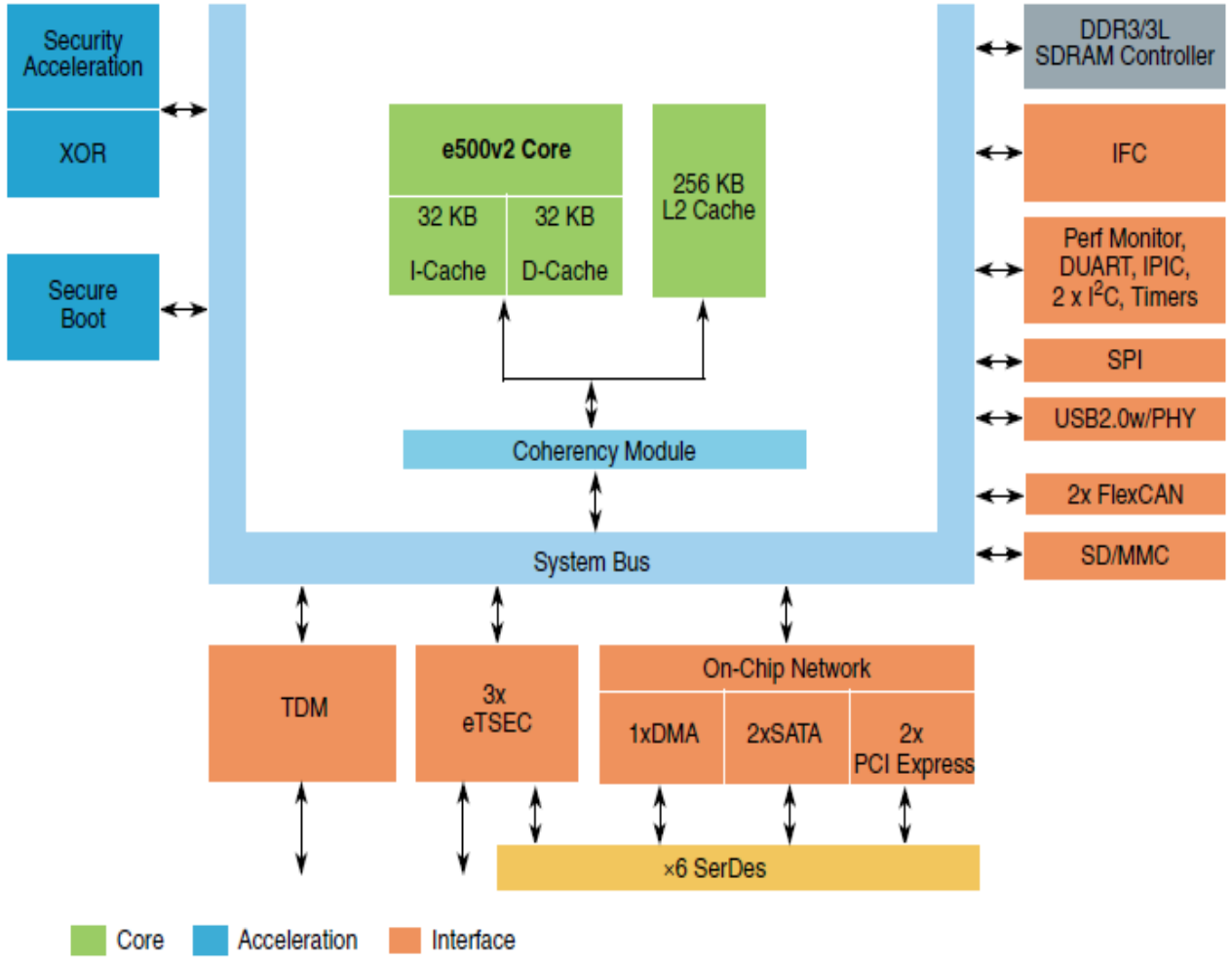
PowerQUICC II Pro to QorIQ Evolution



P1010 Block Diagram

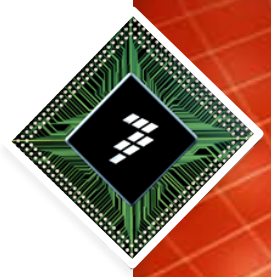


- **e500v2 533 MHz up to 800 MHz**
- **Power consumption less than 3.0 W at 800 MHz core speed**
- **45-nm SOI process technology**
- **Data rate of up to 800 Mbps/pin for DDR3 and DDR3L**
- **Supply voltage 1.0V**
- **Operating temperature (Ta–Tj) range: 0–125°C and –40 to 125°C (industrial specification)**
- **19 × 19 mm 425-pin TEPBGA I (temperature-enhanced plastic BGA)**

P1010 Differentiated Features

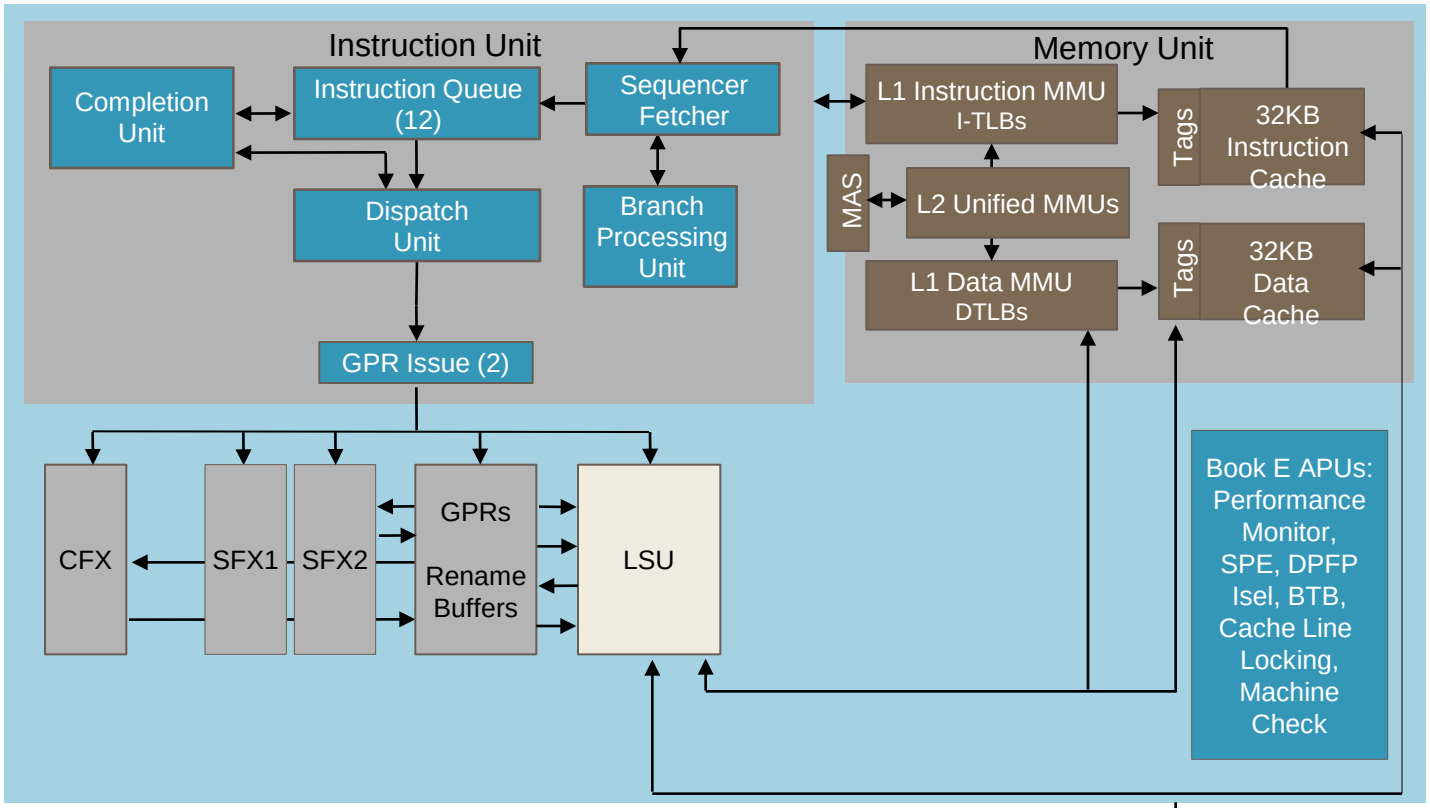
- New IPs/blocks
  - Integrated Flash Controller (IFC)—replacing the eLBC
  - Integrated USB PHY—first in 45nm devices
  - Secure boot—first in the P1 series
  - DDR3L—first in Freescale devices
  - FlexCAN—first in NMG devices
  - Sec 4.x—first in P1 series

QorIQ P1010/P1014 Device Features



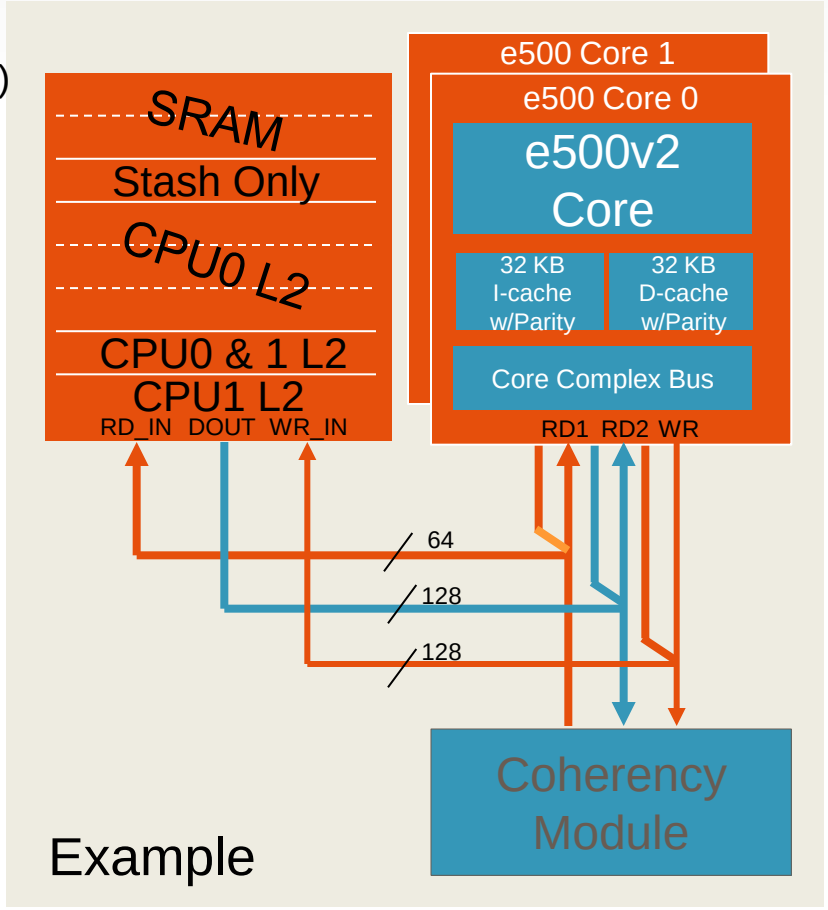
e500v2 Core Architecture

- Up to 1.2 GHz (800 MHz in P1010)
- L1: 32 KB, 8-way set associative, parity
- L2: Front side, 8-way set associative, ECC
- Cache line locking supported
- MESI cache coherence
- Peak IPC 2 instructions plus 1 branch
- Out of order execution
- Multiple book E APUs
- 16 TLB variable page sizes
- 512-entry 4K pages
- 36-bit physical address



L2 Cache Controller

- Shared 256 KB / 512 KB unified front side L2 cache w/8-way associativity (each way: 64 KB)
  - –L2 is 256 KB in the P1010/P1014
- Assignment granularity
  - –One, two, four or all eight “ways” of the cache can be assigned as the following:
  - –SRAM
  - –Stash only
  - –CPU0 L2 only
  - –CPU1 L2 only
  - –Both CPU0 and CPU1 L2
- Stash-only regions can now be defined
  - –Prevents stash data from polluting processor data and vice versa
  - –One, two or four “ways” of the cache can be dedicated as stash only
- Stash allocate disable mode added
  - –Allows update of all resident cache lines without allocation of new lines



P1010 Differentiated Feature DDR3/3L

- DDR memory controller
  - DDR3 with support for a 32-/16-bit data interface (32-bit without ECC and 16-bit with ECC), up to 800 Mbps data rate DDR3 memory controller
  - 4 chip selects
    - All 4 chip selects can be used if interfaced with dual/quad stacked memories
    - Only 2 chip selects can be used if interfaced with memories supporting single chip-select
  - Four layer boards can be designed with discrete DDR memories
    - For DIMMs six layer boards are recommended

DDR Controller

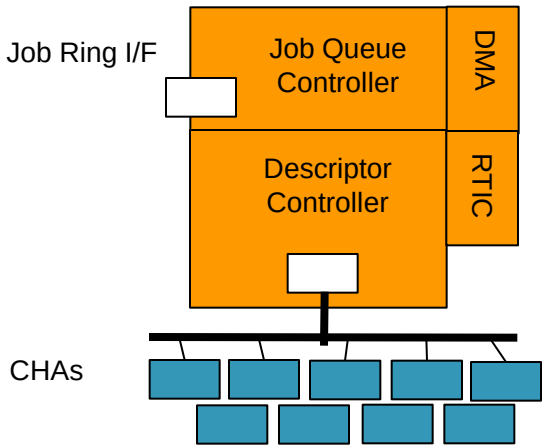
- DDR 3—new feature
  - Lower power performance – ~25% compared to DDR2 (Source - JEDEC)
  - Supply voltage reduced from 1.8V to 1.5V
  - Support for “fly by” routing
    - Results in fewer stubs and improved signal integrity for faster clock speeds
  - Introduced additional registers for write-levelling control for DDR3
  - Asynchronous reset pin for cold or warm reset of memories
  - Separate voltage reference pins for address and data signals for noise reduction
  - Improved pin-out for signal integrity and reduced skew
  - Dynamic ODT for also aids signal integrity
- DDR clocking—ability to asynchronously clock from platform clock supported for higher speed memory devices

Enhanced Three-Speed Ethernet (eTSEC) Controllers

- eTSEC MAC controllers support 10 Mbps, 100 Mbps, 1 Gbps Ethernet /IEEE 802.3 interfaces
  - Similar in specification to MPC831x & MPC837x devices
- Backwards compatible with TSEC controllers used on MPC834x
- Support following PHY interfaces
  - RGMII
  - SGMII interfaces share available SerDes lanes
- Advanced functions part of enhanced controller:
  - TCP/IP acceleration
  - QOS support for up to 8 queues
  - MAC address recognitions
  - CRC generation & checking
  - Extraction and allocation of data to L2 cache
  - Remote monitoring statistics support
- IEEE® 1588 timer support
- Interrupt virtualisation added to P1 devices
  - eTSEC controllers and interrupts can be grouped, to be assigned to a particular core by software
  - Further available information in software section

P1010 Differentiated Feature SEC 4.4

- Public key hardware accelerators (PKHA)
  - RSA and Diffie-Hellman (to 4096b)
  - Elliptic curve cryptography (1023b)
  - Supports run-time equalization
- Data encryption standard accelerators (DESA)
  - DES, 3DES (2K, 3K)
  - ECB, CBC, OFB modes
- Advanced encryption standard accelerators (AESA)
  - Key lengths of 128-, 192- and 256-bit
  - ECB, CBC, CTR, CCM, GCM, CMAC
  - OFB, CFB and XTS
- Message digest hardware accelerators (MDHA)
  - SHA-1, SHA-2 256,384,512-bit digests
  - MD5 128-bit digest
  - HMAC with all algorithms
- ARC four hardware accelerators (AFHA)
  - Compatible with RC4 algorithm
- Kasumi/F8 hardware accelerators (KFHA)
  - F8 , F9 as required for 3GPP
  - A5/3 for GSM and EDGE
  - GEA-3 for GPRS
- Snow 3G hardware accelerators (STHA)
  - Implements Snow 3.0
- CRC unit
  - CRC32, CRC32C, 802.16e OFDMA CRC
- Random number generator, random IV generation
- Header & trailer off load for the following security protocols:
  - IPSec, 802.1ae, SSL/TLS, SRTP, 802.11i, 802.16e
- 1-2 Gbps



SATA Interfaces

- Dual SATA 3 Gbps controllers with integrated PHY
  - SATA controllers supports SATA 2.0
  - Supports 1.5 Gbps and 3 Gbps data rates

PCIe Controller

- PCI Express controller
  - Two PEX controller/interfaces compliant with “PCI Express Base Specification Revision 1.1”
  - Each supports only by x1 interface
  - MAX_PAYLOAD_SIZE has been reduced from 256 bytes to 128 bytes (every other 85xx and QorIQ devices have 256)
  - Few changes in the P1010 programming model to support secure trust architecture
  - Inbound window 0 is now programmable

Pin-Mux Options

- Pin multiplexing is available between following interfaces:
  - IFC/eSDHC/ULPI
    - Address-only lines of IFC are multiplexed
    - NAND interface signals are not multiplexed
    - LCLK0 is muxed with CS3
  - CAN/UART/TDM
    - UART0 is non-muxed
  - TSEC1 (RGMII)/1588
    - Doesn't disable 1588
- Pin multiplexing can be configured through PMUXCR1/2 registers

P1010 Differentiated Features IFC

- Integrated flash controller (replacement for eLBC)
  - Flash controller with four chip-selects
  - AXI V1.0 slave interface
  - Sky blue bus interface for register access
  - Support for error and debug registers
  - Functional muxing of pins between NAND (512 to 4K Bytes Page, NOR and GPCM)
  - Support memory banks of size 64 KByte to 4 Gbytes
  - Write protection capability
  - Provision of software reset

P1010 Pin-Mux Options (Cont.)

- SerDes I/O port multiplexing (through POR configs)

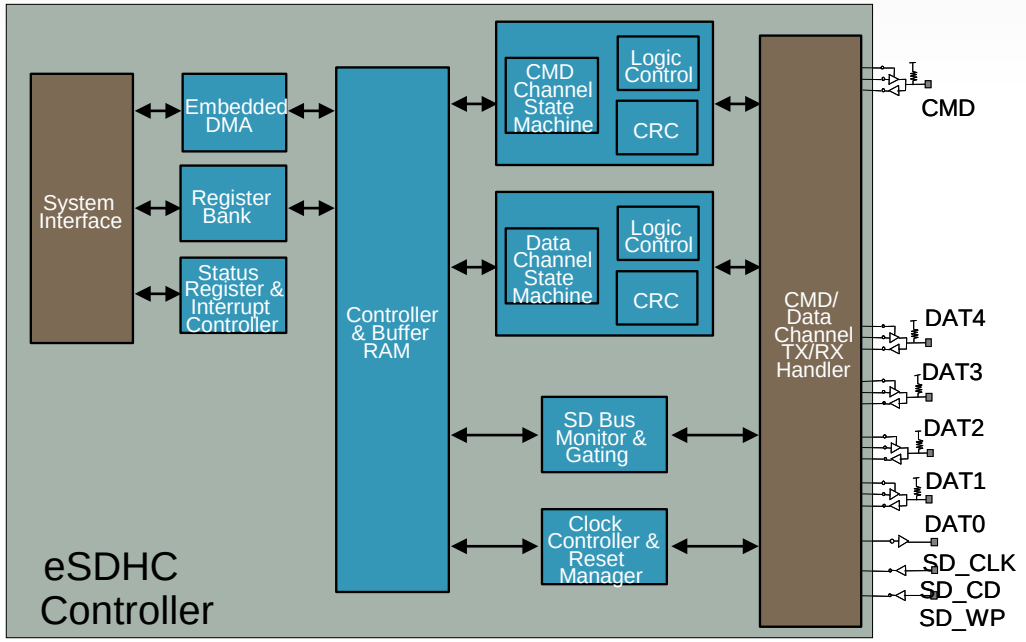
Not in P1014

Table 4-19. SerDes I/O Port and Protocol Selection

Functional Signal	Reset Configuration Name	Value (Binary)	4-Lane SerDes				2-Lane SerDes	
			0	1	2	3	0	1
IFC_AD[13:14] Default (11)	cfg_io_ports[0:1]	00	off	off	off	off	off	off
		01	PCI Express 1 x1 (2.5)	PCI Express 2 x1 (2.5)	SGMII 2 (1.25)	SGMII 3 (1.25)	SATA1 (3.0)	SATA2 (3.0)
		10	PCI Express 1 x1 (2.5)	SGMII 1 (1.25)	SGMII 2 (1.25)	SGMII 3 (1.25)	SATA1 (3.0)	SATA2 (3.0)
		11	off	SGMII 1 (1.25)	SGMII 2 (1.25)	SGMII 3 (1.25)	PCI Express 1 x1 (2.5)	PCI Express 2 x1 (2.5)

Enhanced Secure Digital Host Controller (eSDHC)

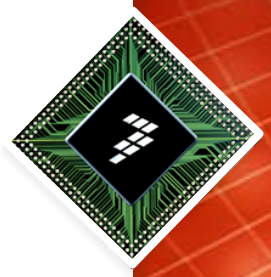
- Memory card interface available on QorIQ platforms
  - Similar in specification to the eSDHC on MPC837x
- Provides high-speed, flexible data storage capability to a system
- Designed to work with various SD & MMC card formats
  - SD, SDHC, miniSD, SD combo, MMC, MMC*plus* & RS-MMC cards
- Supports capacities of up to 32 GB, with different speeds
- Boot interface support—new feature
  - Revision 1.0 of the P1010 has an errata that prevents boot from SD. Although a work around exists there are no plans to revise the device and fix the errata



P1010 Differentiated Feature USB 2.0 Plus PHY

- USB 2.0 host and device controller with an on-chip, high-speed PHY
  - Supports ULPI and UTMI
  - Provides four wire USB bus interface (internal PHY, UTMI mode)
  - PHY supply needs to follow power sequencing and ramp rate constraints (refer to H/W spec for more info)

Hardware Design Considerations

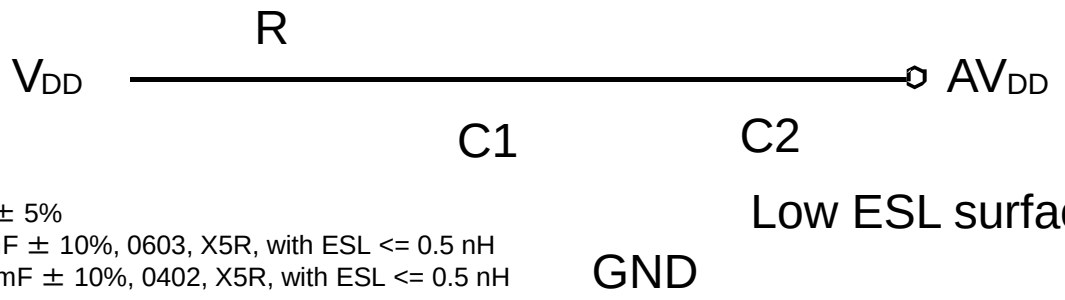


Power Sequencing

- Power sequencing is different from PowerQUICC II Pro
- P1 devices requires power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:
  - VDD, AVDD_n, BVDD, LVDD, OVDD,CVDD, XVDD_SRDS and XVDD_SRDS
  - GVDD
  - NOTE: Items on the same line have no ordering requirement with respect to one another
  - NOTE: If any of the I/O power supplies ramp prior to VDD core supplies, the associated I/O supply may drive a logic one or zero during power-up thus causing excessive current to be drawn by the device.
- All supplies must be at their stable values within 50 milliseconds

PLL Filter Circuit

- Provide independent filter circuit to each of the AVDD pins
  - AVDD_PLAT, AVDD_CORE[0:1], AVDD_DDR, and AVDD_LBIU, respectively
  - Independent circuits reduces chance of noise injection between PLLs



R = 5 W ± 5%
C1 = 10mF ± 10%, 0603, X5R, with ESL <= 0.5 nH
C2 = 1.0 mF ± 10%, 0402, X5R, with ESL <= 0.5 nH

Low ESL surface mount capacitors

  - Circuit will filter noise in 500 KHz to 10 MHz range
  - Use surface mount capacitors with a low effective series inductance (ESL)
  - Place as close to AVDD as possible to reduce noise

- See HW guide for filter specs

SerDes: Design Guidelines

- There are three different supplies used for SerDes block, consistent with PowerQUICC devices:
  - SVDD: Core power supply for SerDes transceivers
  - XVDD: Pad power supply for SerDes transceivers
  - AVDD_SRDS: SerDes PLL supply
- Need clean, tightly regulated power supply with low jitter
- Additional SerDes supply decoupling requirements
  - See HW manual for details
- Design guidelines consistent with *"High Speed Digital Design: A Handbook of Black Magic"*
- Unused SERDES lanes
  - Leave outputs unconnected with inputs connected to GND

POR Configuration Inputs

- P1/P2 platforms have power on reset (POR) signals used for device configuration
  - Signals are muxed with existing I/O pins
- The settings for the following POR pins will determine CPU boot enable, PLL ratios and boot device selection:
  - LA[29:31] - cfg_sys_pll[0:2]
  - LBCTL, LALE, LGPL2 - cfg_core0_pll[0:2]
  - LWE0, UART_SOUT1, READY_P1 - cfg_core1_pll[0:2]
  - TSEC1_TXD[6:4],TSEC1_TX_ER - cfg_rom_loc[0:3]
  - LA[27] - cfg_cpu0_boot
  - LA[16] - cfg_cpu1_boot
  - LGPL3, LGPL5 - cfg_boot_seq[0:1]
- Further configuration signals may be used in the future to control functionality. It is advised that boards are built with the ability to pull up or pull down these pins.
  - LA[20] - cfg_eng_use[00]
  - LA[21] - cfg_eng_use[01]
  - LA[22] -cfg_eng_use[02]
  - UART_SOUT[00]- cfg_eng_use[03]
  - TRIG_OUT -cfg_eng_use[04]
  - MSRCID[01] -cfg_eng_use[05]
  - MSRCID[04]- cfg_eng_use[06]
  - DMA1_DDONE[00]- cfg_eng_use[07]
- POR signals are sampled on HRESET negation

POR Configuration Pins Termination Requirements

- The following pins must NOT be pulled down during power-on reset, otherwise it may trigger the internal test mode:
  - DMA1_DACK[00]
  - USB1_STP
  - HRESET_REQ
  - MSRCID[2:3]
  - MDVAL
  - ASLEEP

DDR Interface Design

- DDR3 guidelines available from AN108
  - "Designing for DDR3 Memory on Freescale Microprocessors"
- DDRCLK input
  - Input is only required when the DDR controller is running in asynchronous mode
  - Not required if DDR controller is selected to work in synchronous mode, via POR setting cfg_ddr_pll[0:2]=111
  - It is recommended to tie it off to GND when DDR controller is running in synchronous mode
  - DDR3 is only supported in asynchronous mode

eTSEC Pin Termination

- Addition termination requirements for eTSECs compared to PowerQUICC II Pro
  - When eTSEC1 and eTSEC2 are used as parallel interfaces, pins TSEC1_TX_EN and TSEC2_TX_EN requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven
  - TSEC2_TXD[01] is used as cfg_dram_type. It must be valid at power-up, even before HRESET assertion
- Unused eTSEC pin termination
  - For I/Os, tie signals high or low through a resistor; recommended resistor values are 2–10K ohm
  - For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low; recommended resistor values are 2–10 K ohm

Suggestion on Power Supply and Power Supply Test Point

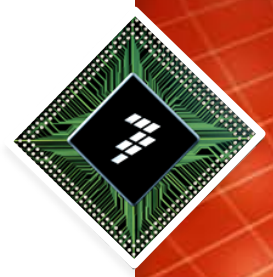
Following applies for both PowerQUICC II Pro and QorIQ devices:

- For prototype board, suggest isolating power supplies and have independent controls over:
  - VDD, AVDDs (Core and PLLs)
  - SVDD (SerDes core)
  - XVDD (SerDes pad)
  - OVDD (DUART, I^2C, JTAG etc...)
  - LVDD (eTSECs)
  - GVDD (DDR)
  - BVDD (local bus)
  - CVDD (USB, eSPI, eSDHC)
- The voltage range should be adjustable
  - Particularly for VDD, AVDDs, SVDD and XVDD, they should be adjustable at least between 1.0V to 1.1 V nominal; also allows for easier migration between device families
  - Have test points near processor for these supplies
- Have visibility of all processor BGA pins on the back of card

Debug

- **QorIQ P1 / P2 devices have specific debug assist pins**
  - TRIG_OUT/READY (this helps to verify the end of the reset sequence)
  - TRIG_IN (trigger in to trigger the watchpoint and trace buffers)
  - MSRCID [0:4] & MDVAL—memory debug signals
- **General list of signals to have accessible for analysis on all devices**
  - DDR3—address, data, control & clock signals
  - Local bus—address, data, control & clock signals
  - Machine check & interrupt signals
  - SerDes—transmission lanes & reference clock signals
  - HRESET# / HRESET_B
  - SD_PLL_TPA, & SD_PLL_TPD (SerDes analog and digital PLL lock indication)
- **Debug signals specific to the MPC831x/MPC837x**
  - CFG_RESET[0:3] source signals
  - SRESET_B
  - PORESET_B
- **Debug signals specific to the P1 / P2 platforms**
  - HRESET_REQ (this helps to verify proper boot sequencer functions and reset requests)
  - ASLEEP (this helps to verify the end of the reset sequence)
  - SYSCLK (to verify input clock at the device pin)
  - CLK_OUT (this helps to verify the CCB clock)
  - DDRCLK (to verify DDR Clk when in asynchronous mode)
  - CKSTP_OUT[0:1] (e500 checkstop indication)
  - Debug assist pins

Reset Configuration, Clocking and Initialization



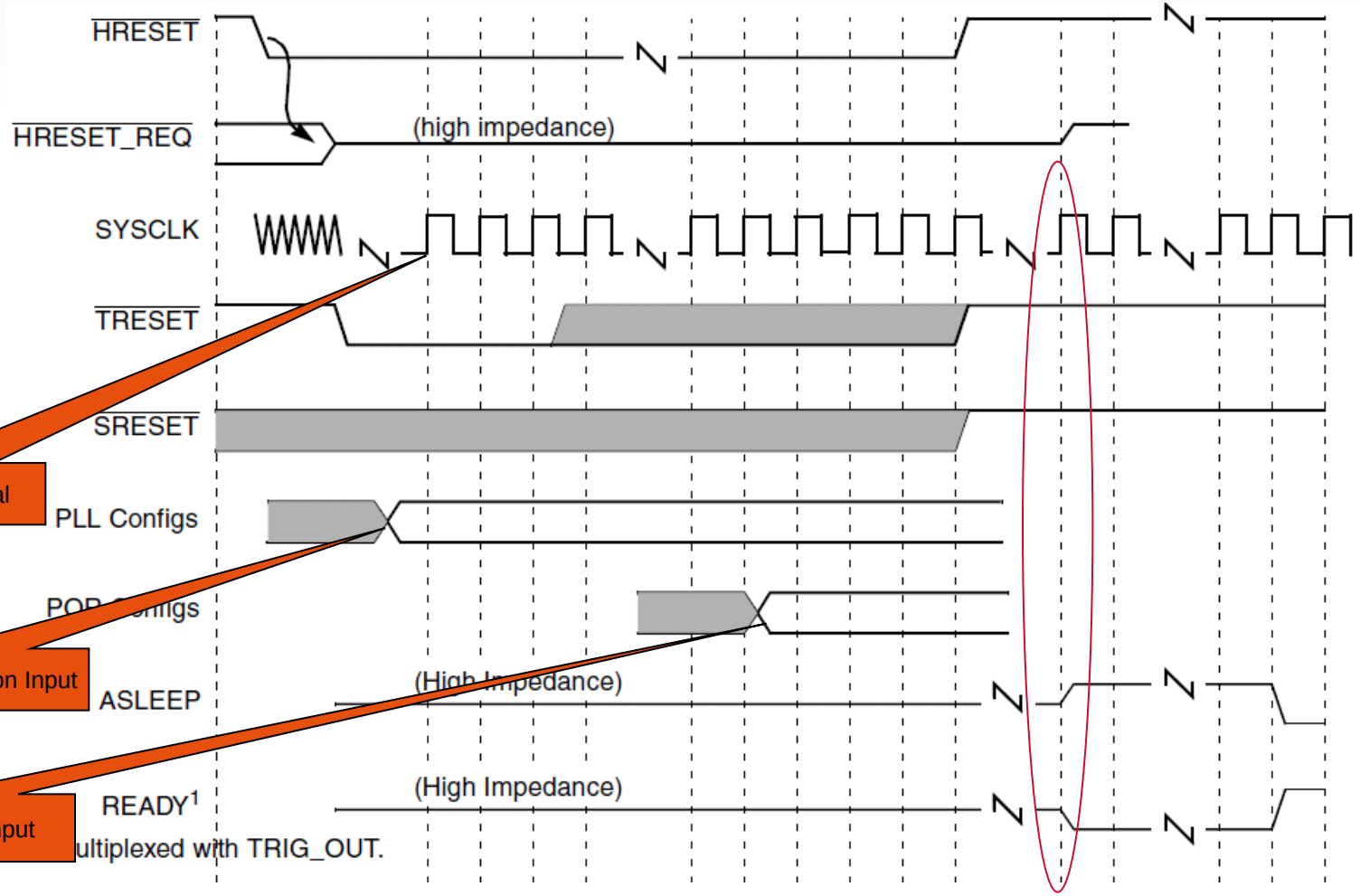
POR Configuration

- QorIQ P1 / P2 devices use power-on reset (POR) configuration pins, which are sampled during the assertion of HRESET_B
- All POR configuration pins are typically multiplexed with the output signals
- All POR configuration pins have internal pull-up resistor (~20 KΩ) and those resistors are activated only during the POR configuration
- During HRESET, all other signal drivers connected to these POR configuration signals must be in the high-impedance state
  - Reason: If other devices also drive POR pin during HRESET, device may sample the wrong POR configuration information from the POR pin

Power-On Reset

- Power-on reset sequence is significantly different to PowerQUICC II Pro family
  - HRESET# —now input only and replaces PORESET# input
  - HRESET_REQ# —output, used to request reset
  - SRESET# —input only
  - READY_P0 / TRIG_OUT —Core 0 ready output / external trigger output
  - READY_P1 —Core 1 ready output (if available)
- Signals no longer available
  - CFG_RESET_SOURCE[0:3] —used to load configuration words; function replaced by POR configuration pins
  - CFG_CLKIN_DIV# —clock division selection is carried out by POR PLL config pins

Power-On Reset Sequence



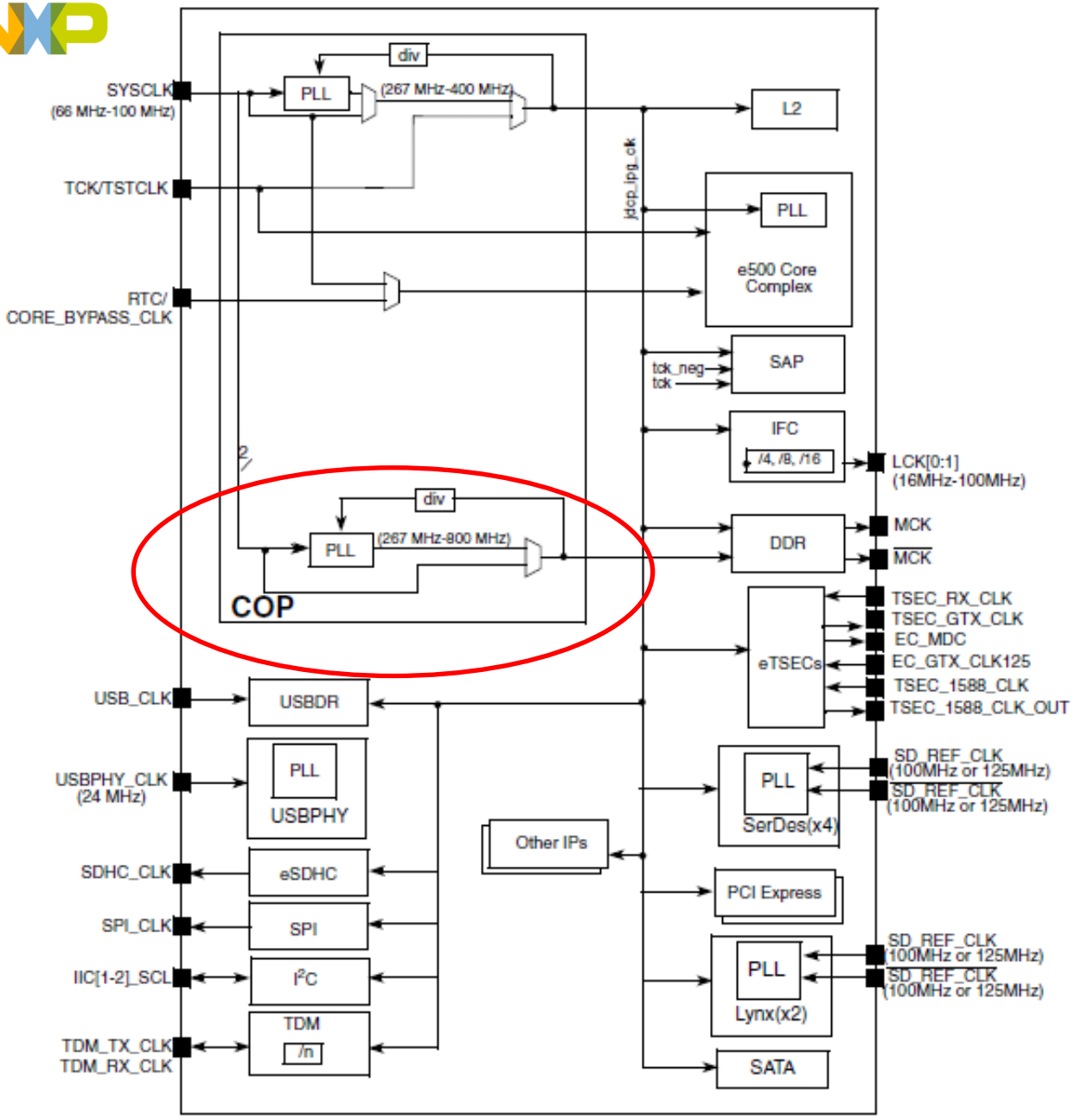


Figure 4-6. P1010 Clock Subsystem Block Diagram

- **Supports DDR asynchronous mode through separate DDR PLL**
- **No separate clock input required for async mode**

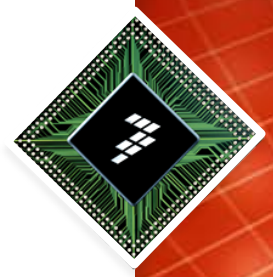
Boot Modes

- Possible boot interfaces
  - IFC (NOR, NAND, MLC, SLC)
  - DDR3/3L memory controller
  - PCI Express interface
  - eSPI interface
  - eSDHC interface (errata on P1010 prevents boot on SD)

New boot interfaces supported on P1

- Boot sequencer—migrated from PowerQUICC II Pro
- Boot hold-off—registers used to suspend core booting
  - Used when booting two cores; CPU0 boots while CPU1 waits
  - Used when external master boots device over eg. RapidIO or PCIe
- Reset - e500 begins execution from fixed location of 0xFFFF_FFFC

Software Design Considerations



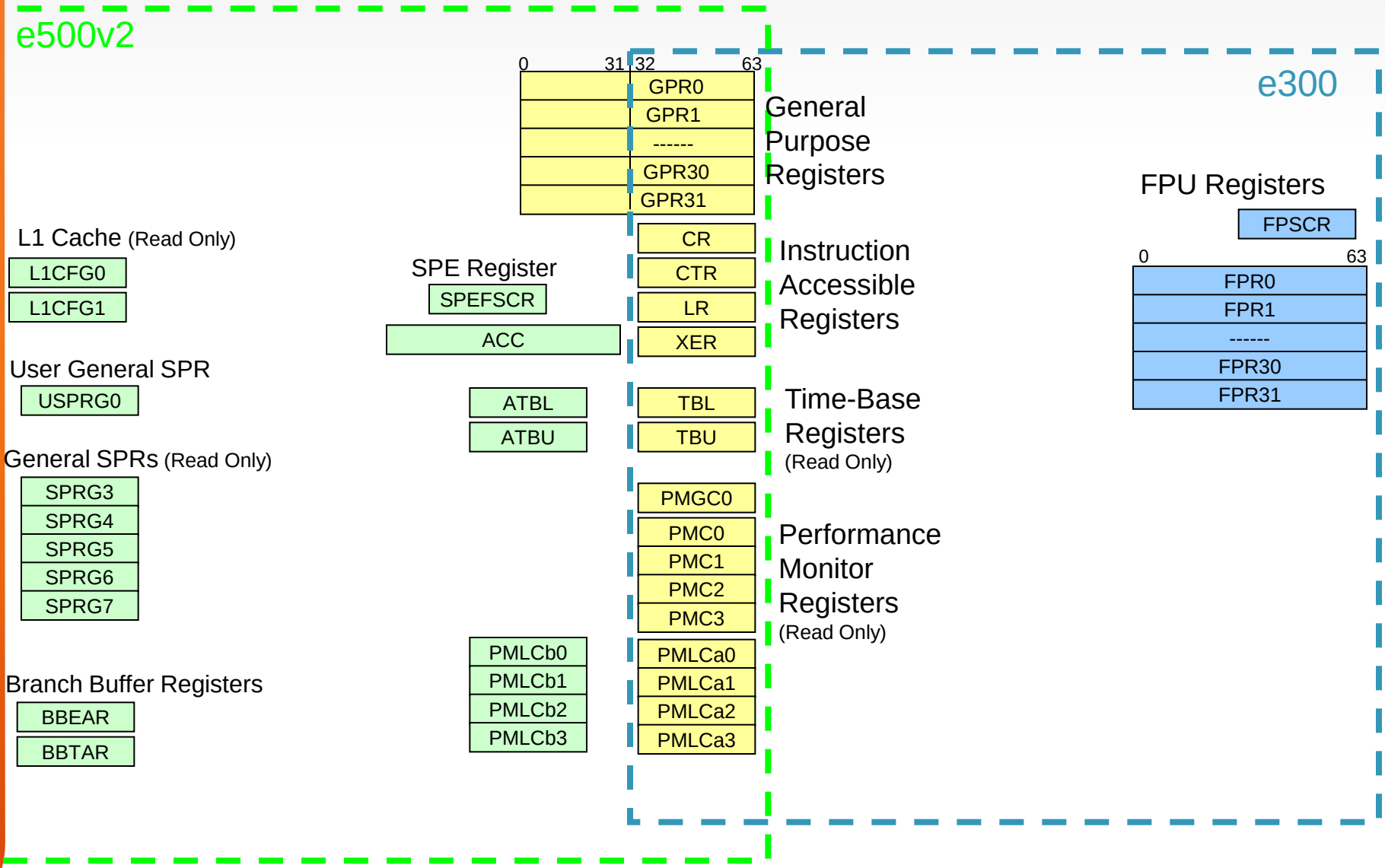
Memory Map

- e500v2 based QorIQ devices deploy a 36-bit local address space
- Local Access Windows (LAWs)
  - Support multiple access windows like e300 devices
  - Maximum window size increased from 2 GBytes to 32 GBytes
- ATMU—Address Translation & Mapping Unit
  - Used for translating between local & external address spaces
  - Further ATMUs added on QorIQ platforms for additional PCIe controllers & SRIO
- CCSR—Command, Configuration & Status Registers
  - Replacement to IMMR space registers on PowerQUICC II Pro
  - All registers contained within a 1 MByte address region
  - Offers additional flexibility—can be relocated, and provides easier external access

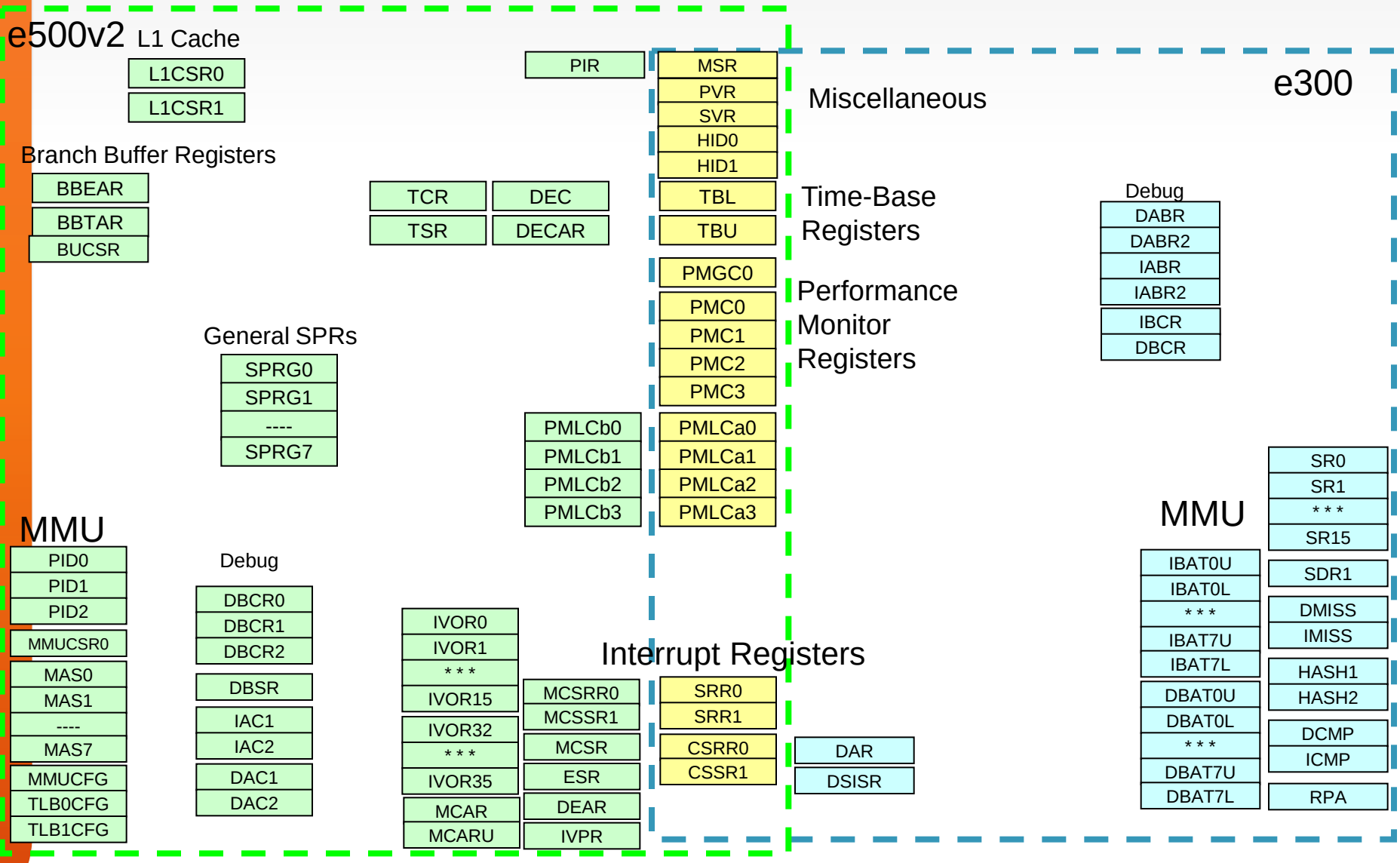
e300 to e500v2 Migration Privileges: Programming Model

- Power Architecture cores operate in either of the following two modes
  - *Supervisor mode*: This is the highest privilege mode where entire programming model is available for the software. Operating systems and boot loaders operate on this mode.
  - *User mode*: Resources, which can affect whole system, are not available in this mode. User-level applications or non-trustable programs operate on this mode.

e500 to e500v2 Migration: User Level Registers



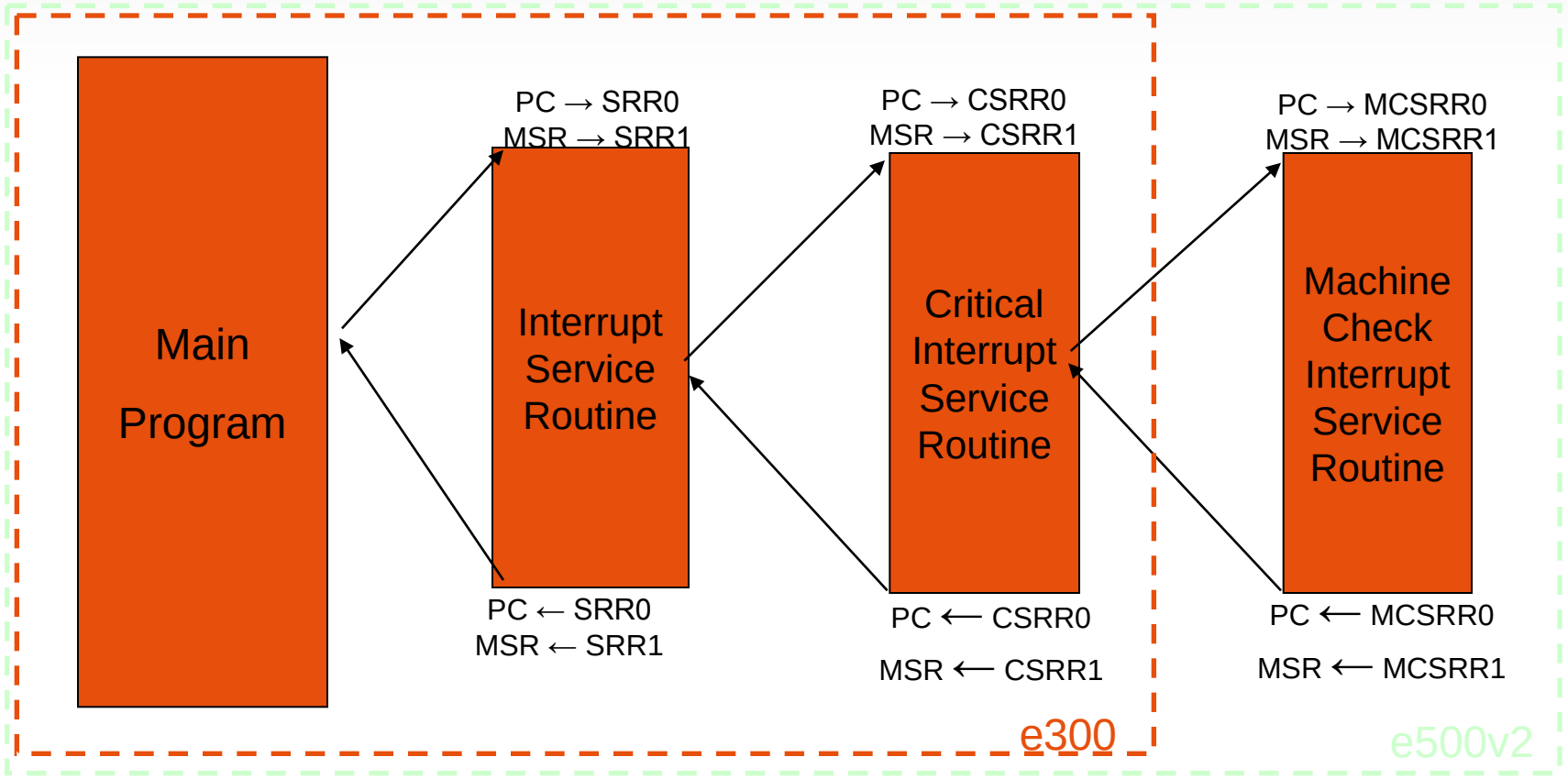
e500 to e500v2 Migration: Supervisor Level Registers



e300 to e500v2 Migration: Exceptions

- While exceptions had fixed vector addresses in e300, they are programmable in e500v2 except reset vector
- In e300, reset vectors at 0x0000_0100 while it vectors at 0xFFFF_FFFC in e500v2
- e500v2 has a new category of exception via machine check

e300 to e500v2 Migration: Exception Handling

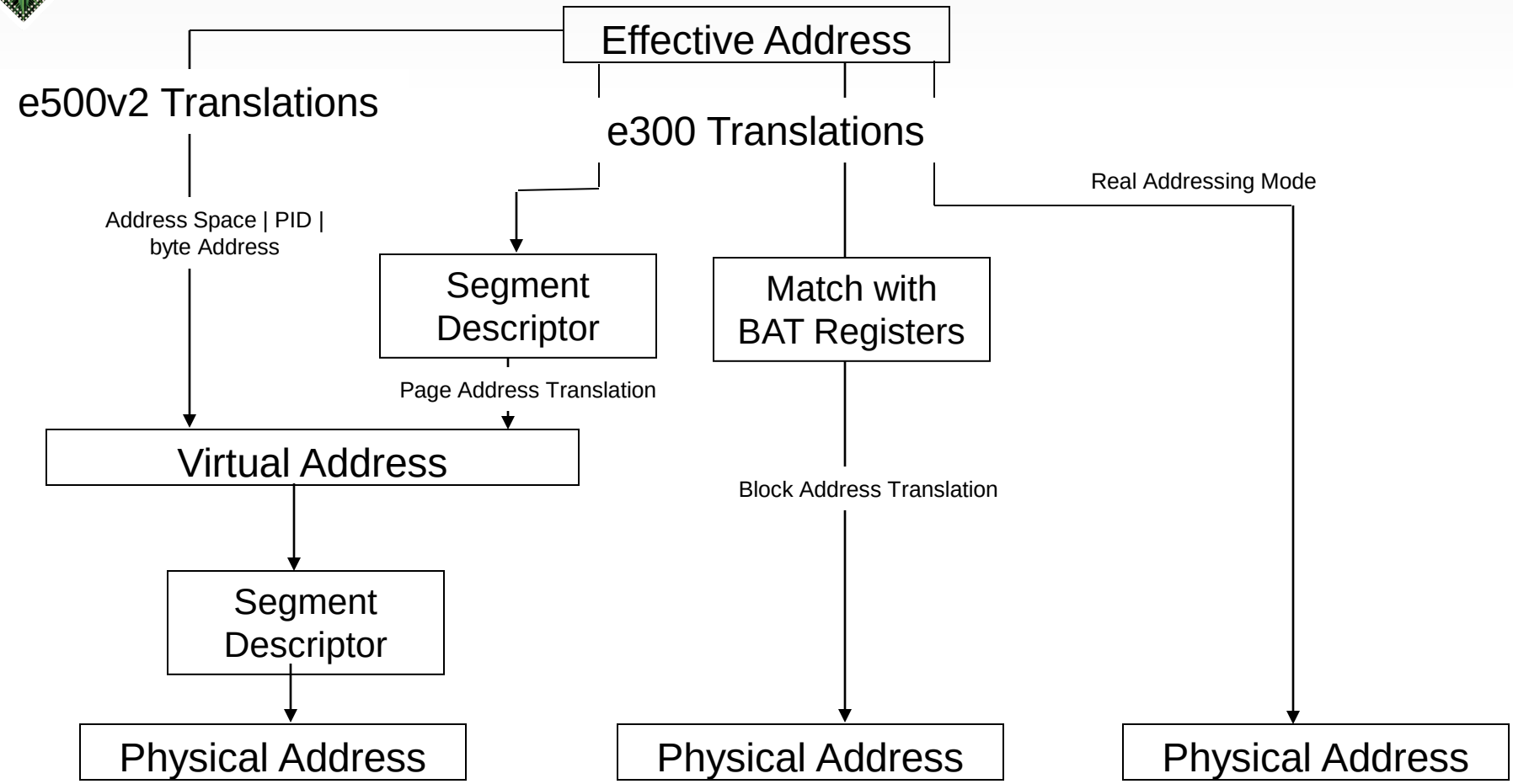


A new category of machine check interrupt has been added in e500v2

e300 to e500v2 Migration: MMU

- e300 supports BAT and page translations while e500v2 has 512 entries of fixed 4k pages and 16 entry variable size pages
- e300 endian mode is controlled on system basis while e500v2 allows endian configuration per page basis
- Unlike e300, MMU is always on in e500v2
- After reset, a default entry in MMU maps logical address 0xffff_f000 to physical address 0xffff_f000

e300 to e500v2 Migration: MMU Translation Difference



Cache

- e300 has 16/32k L1 I/D cache while e500v2 has 32k L1 I/D cache and 256k L2 cache
- e300 supports way-locking while e500v2 supports line-locking
- e500v2 has non-blocking caches (support hit under misses and miss under misses)
- e500v2 supports stashing on L2

e300 to e500v2 Migration
Instruction Model

- Integer arithmetic, compare, logical, rotate and shift
  - Unchanged between e300 and e500v2
  - e500v2 implements the Power ISA™ integer select (*isel*) instruction
  - e500v2 also supports integer instructions in the signal processing engine (SPE) APU
- Integer load / store
  - e500v2 does not implement load / store string operations
  - All other load / store instructions are unchanged
  - e500v2 SPE APU allows double word loads and stores

Refer to Appendix B

e300 to e500v2 Migration
Instruction Model

- Floating Point
  - e300 used a dedicated floating point unit (FPU) for 32-/ 64-bit floating point registers (Note: e300c2 does not have a FPU)
  - e500v2 implements scalar single-precision, vector single-precision and scalar double-precision embedded floating point categories through the SPE APU
  - e500v2 uses general purpose registers, extended to 64 bits to accommodate vector and double precision operations
  - e300 and e500v2 floating point opcodes are not the same

Refer to Appendix B

e300 to e500v2 Migration
Instruction Model

- Processor control
  - All move to / from SPR, CR, XER, TB, MSR, PMR are unchanged (note e300c1 and c2 do not have performance monitors)
  - e500v2 does not have segment registers or a FPSCR
  - e500v2 implements the Power ISA™ write MSR external enable instruction (*wrtee[i]*)
- Memory synchronisation
  - Reservation instructions (*lwarx, stwcx.*) are unchanged
  - Instruction synchronise (*isync*) is unchanged
  - Memory synchronise is defined as *sync* for the e300 and *msync* for the e500v2. Power™ ISA defines *msync* as a simplified mnemonic of *sync*
  - Enforce in order execution of I/O is supported as *eieio* on the e300 and maps to the *mbar* instruction on the e500v2

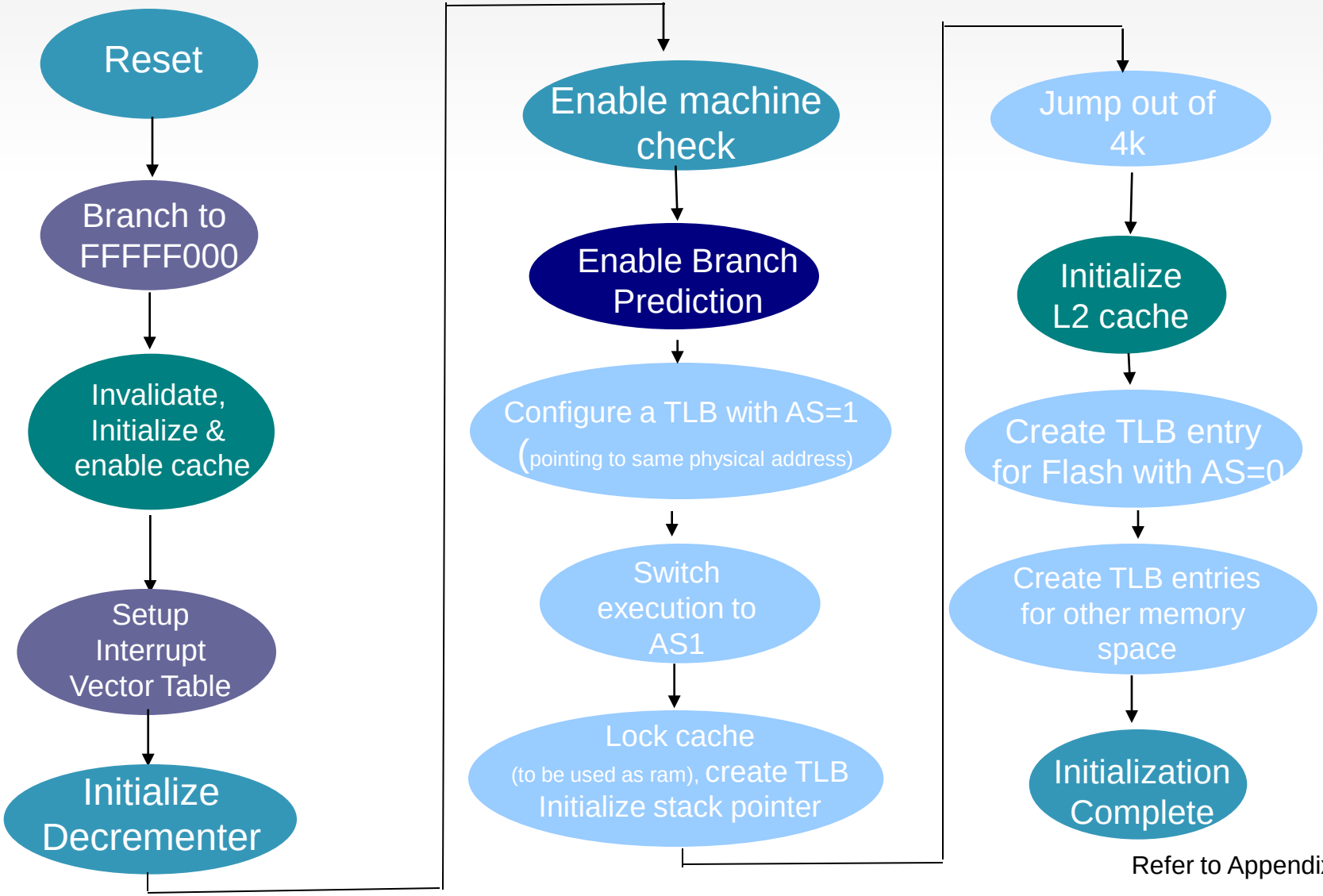
Refer to Appendix B

e300 to e500v2 Migration
Instruction Model

- Memory control
  - Cache
    - User level cache instructions (touch, touch for store, allocate, clear, zero, store and flush) are unchanged
    - e500v2 implements Power ISA™ cache lock instructions (*icblc, icbtls, dcblc, dcbtls, dcbstls*)
    - e500v2 cache instructions can specify target cache as L1 or L2
  - MMU
    - e300 and e500v2 MMUs are architecturally different
    - e500v2 uses MMU Assist registers to access the translation lookaside buffers (TLBs)
    - e300 directly updates the TLBs
    - TLB invalidation and synchronisation remains unchanged

Refer to Appendix B

500v2 Initialization Flow



Refer to Appendix A

Software Migration Considerations
Operating System Migration

- e500v2 imposes numerous changes to classic PowerPC operating systems
- Areas affected include:
  - Instruction set use
  - Context switching
  - Exception handling
  - MMU operation
  - Reset
- Necessary changes have already been made by PowerPC OS vendors
- Linux BSPs with gcc based toolchain available from Freescale
  - http://www.freescale.com/linux

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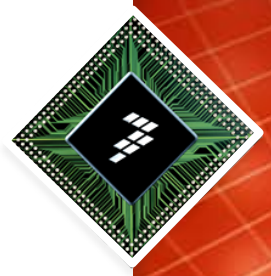
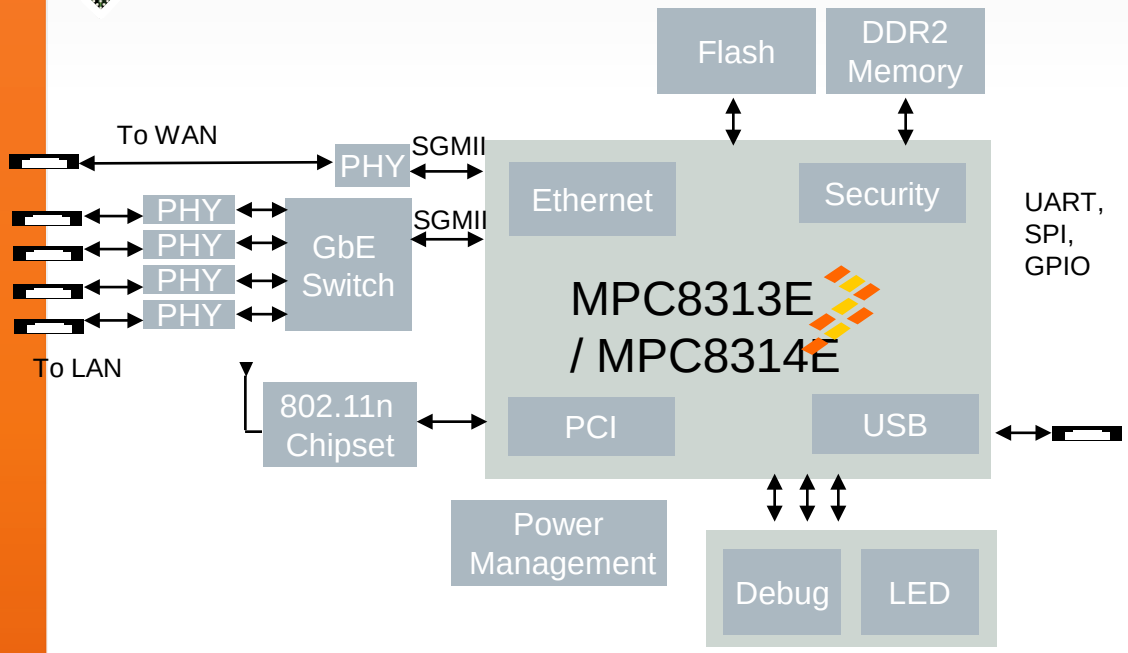
Application Case Studies

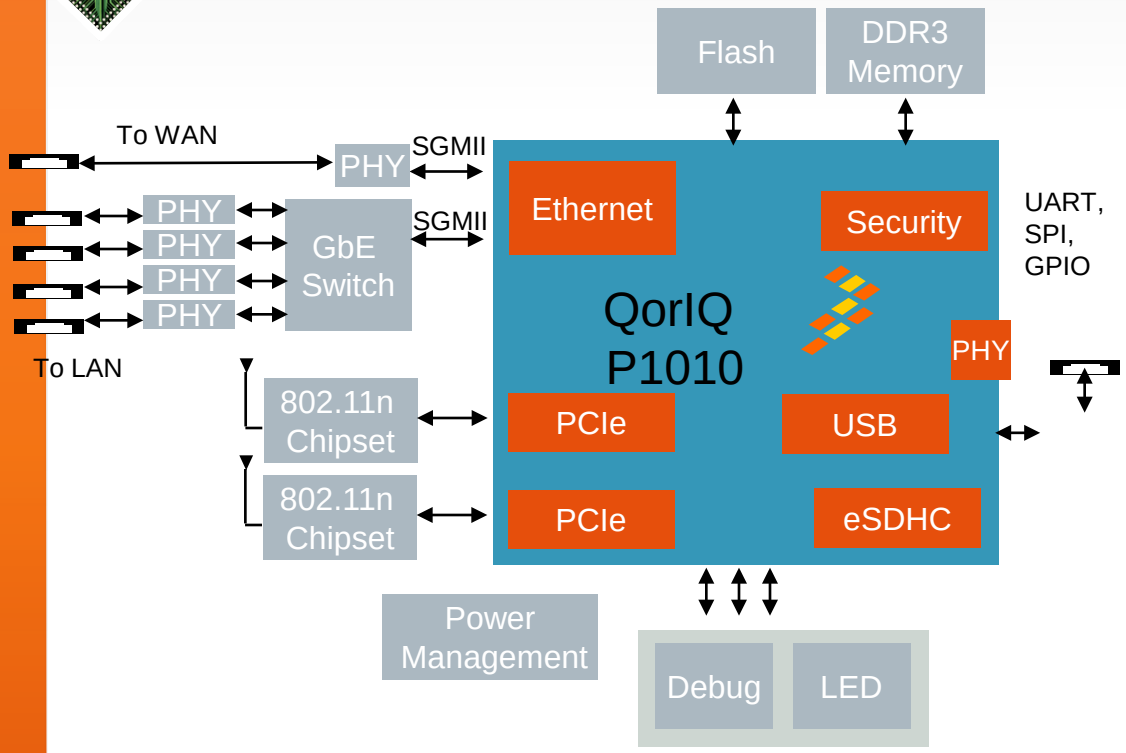


Wireless Router Application—PowerQUICC II Pro



- Based on MPC8313E/14E
  - e300 core, 400 MHz max
- DDR / DDR2 memory
- WAN
  - VDSL2 (GMII based)
  - Dedicated GbE interface
- LAN
  - 4x 100/1000BT w/ RJ45
- Wireless
  - 802.11n interface via PCI
- Security
- Onboard flash memory
- 1 x USB 2.0
- Power modes

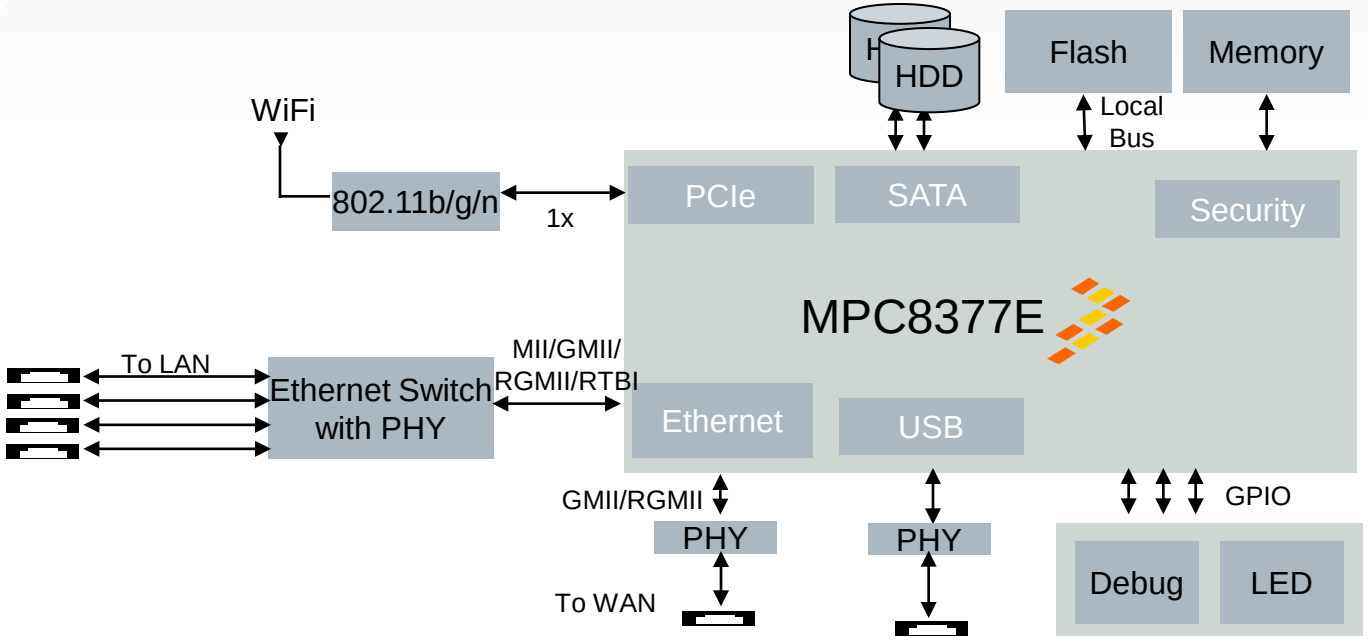
Wireless Router Application—QorIQ



- Based on P1010
  - 800 MHz max freq
- DDR3 memory support
- WAN
  - Dedicated GbE interface
- LAN
  - 4x 10/100/1000 w/ RJ45
- Wireless
  - 2 x 802.11n via 1x PCIe interfaces
  - Support for 2x2 MIMO
- Security
- Onboard flash memory
- USB 2.0
- eSDHC interface
- Power modes

- Benefits
  - Increased performance per core
  - Existing interfaces supported
  - Ability to support 2x2 MIMO, enhanced network performance of up to 300 Mbps
  - eSDHC for onboard storage

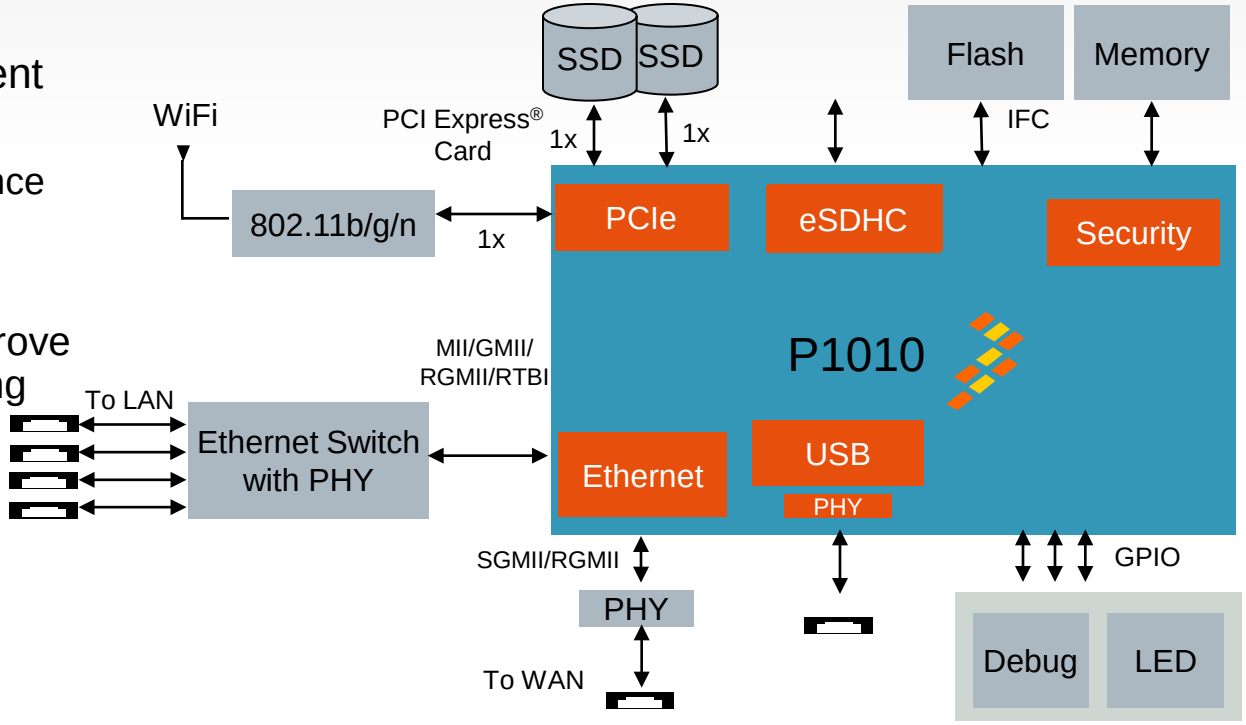
NAS Storage Application—PowerQUICC II Pro



- e300 based platform, up to 800 MHz performance, 1.92 DMIPS/MHz performance, <5W @ 800 MHz
- Integrated SATA controller used to connect up to 2x HDD
- Gigabit Ethernet LAN and WAN interface
- Wireless capability available through PCIe card
- USB interface accessible through external PHY

NAS Storage Application—QorIQ P1 / P2

- Performance improvement with e500 core
  - Up to 800 MHz performance per CPU
  - 2.4DMIPS/MHz
- L2 cache available to improve Ethernet packet processing
- Storage capability:
  - SSD on PCIe
  - eSDHC interface



- Gigabit Ethernet LAN and WAN interface maintained

- Potential to add additional services using extra CPU processing capability

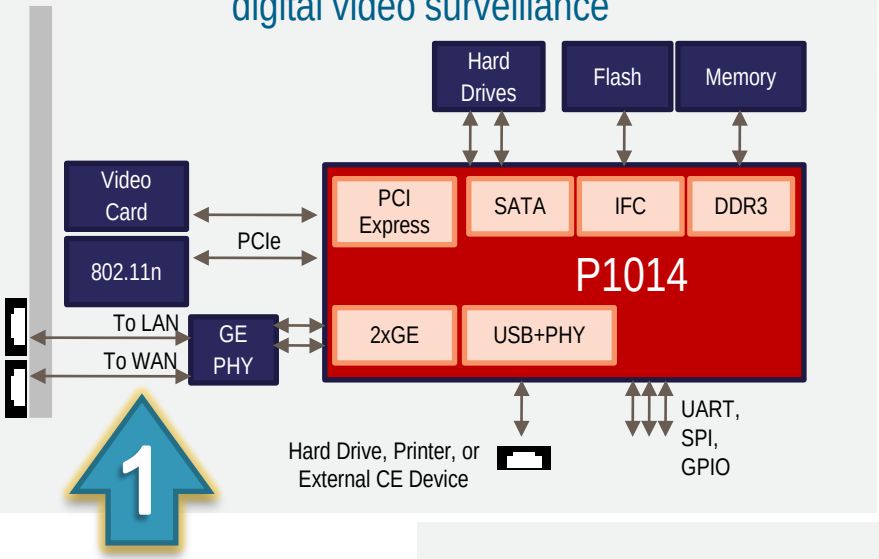
Application Migration—Hardware

- New board design required for QorIQ device

Issue	Solution with QorIQ P1 /P2
Power supply	Same voltage architecture. Adjustable supplies will ease migration from 1.1V on PowerQUICC II Pro to 1.0V for QorIQ P1
Existing interfaces	Re-use design for existing interfaces such as Ethernet, eSPI, JTAG and USB
New interfaces	Use application notes, evaluation boards and other resources from **www.freescale.com**
Power performance	Best-in-class power performance, enable fanless “green” design; advanced power management
Simulation	IBIS models available for all devices

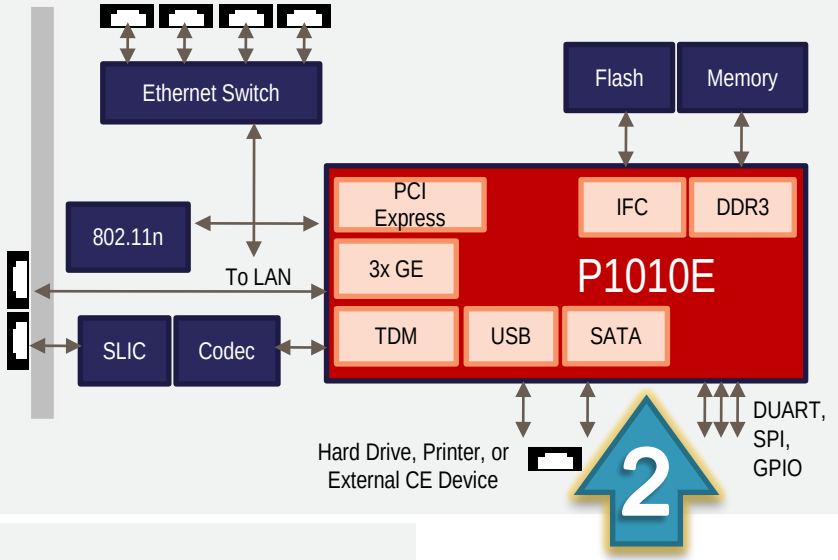
QorIQ P1010 and P1014 Target Applications

Network attached storage / digital video surveillance



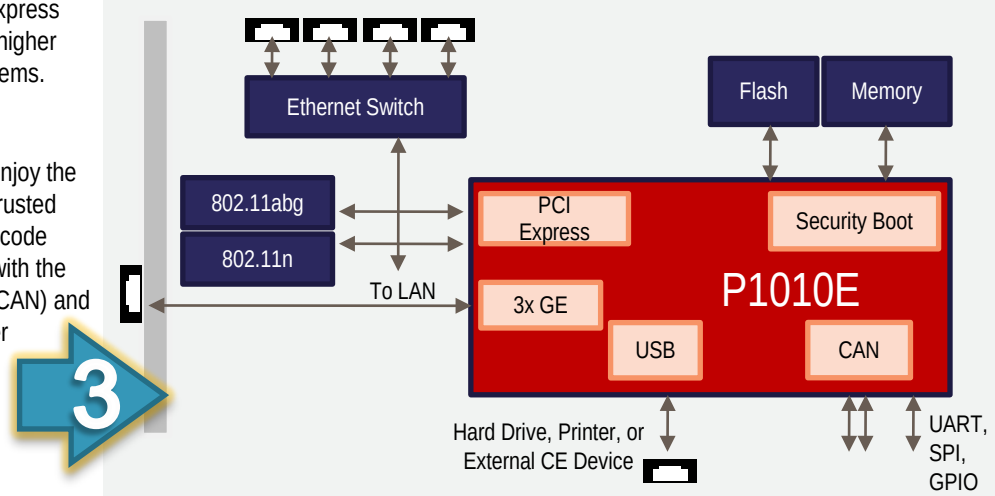
(NAS/DVR) systems benefit from leading performance and integration (PCI Express and SATA interconnects), enabling higher storage throughput in low BOM systems.

Cost-efficient routing applications



Cost-sensitive routing applications enjoy the benefits of software data path acceleration to increase networking performance. A small package (19 x 19 mm) and low power will enable low bill of materials—fanless designs

Industrial networking



Industrial networking applications enjoy the unique product differentiation of a trusted architecture that enables complete code signing and secure boot. Coupled with the integration of industrial interfaces (CAN) and outstanding performance in a power envelope of less than 1.1W, provides the ingredients for the most innovative designs in the segment.

Application Migration—Software

- Migration from e300 to e500 based platform

Issue	Solution with QorIQ P1 /P2
Code base migration	General code compatibility with exceptions in certain areas—floating point, interrupts, supervisor instructions. See resources at www.freescale.com
Operating systems & tools	Established ecosystem of operating systems BSPs, tools and drivers for e500 based platforms, thus reducing development time
Software compatibility for reused interfaces	Code used for existing interfaces such as Ethernet and security block will migrate
New interfaces and features	Driver-level source code available for Freescale evaluation platforms from www.freescale.com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Documentation

- e300
  - ***e300 Power Architecture® Core Family Reference Manual***, which describes functionality specific to the e300
  - ***Programming Environments Manual for 32-Bit Implementations of the PowerPC® Architecture*** (referred to as the PEM), which describes the functionality common to all PowerPC devices

- e500v2
  - ***e500 Power Architecture Core Family Reference Manual***, which describes functionality specific to the e500 cores
  - ***EREF: A Programmer's Reference Manual for Freescale Embedded Devices***, which describes the functionality common to all Freescale Power ISA™ embedded devices

e300 to e500v2 Migration
Exception Tables

Interrupt Type	e300	e500
System reset	0x100	-
Critical interrupt	0xa00	IVOR0
Machine check	0x200	IVOR1
Data storage interrupt	0x300	IVOR2
Instruction storage interrupt	0x400	IVOR3
External interrupt	0x500	IVOR4
Alignment	0x600	IVOR5
Program	0x700	IVOR6
Floating point unavailable	0x800	IVOR7
Decrementer	0x900	IVOR10
System call	0xc00	IVOR8
Trace	0xd00	-
Instruction translation miss	0x1000	-

Interrupt Type	e300	e500
Data store translation miss	0x1100	-
Data load translation miss	0x1200	-
Instruction address breakpoint	0x1300	-
System management interrupt	0x1400	-
Performance monitor	0xf00	IVOR35
Fixed interval timer	-	IVOR11
Watchdog timer	-	IVOR12
Data TLB error	-	IVOR13
Instruction TLB error	-	IVOR14
Debug	-	IVOR15
Vector unavailable	-	IVOR32
Embedded floating point data	-	IVOR33
Embedded floating point round	-	IVOR34

e500v2 MMU benefits

- e500v2 has a simpler page-based MMU than classic PowerPC
  - Software-managed TLBs, no hardware table walking
  - No segments, no BATs, no page table definition
  - Software can use its own page table format
  - TLB misses and faults cause exceptions, no hashing
- No real mode (translation is always on)
  - Real mode can be emulated by creating global TLB entries for address space 0 that map all physical memory 1 to 1
  - On reset, one 4 KB page is mapped
- Instructions architected to read/write and search/invalidate TLB entries

Appendix A: Code Snippets

- After reset, by default, the first entry in MMU L2 TLB1 has logical address 0xffff_f000 mapped to physical address 0xffff_f000
- Core issues first instruction fetch on 0xffff_fffc
- The address should contain a branch instruction

```
.section .resetvec,"ax"
    b _start_e500
```

- Cache initialization:
  - Invalidate I & D caches

```
li      r0,2
mtspr   L1CSR0,r0
```

  - Configure L1CSR0
  - Enable caches

```
lis     r2,L1CSR0_CPE@H /* enable parity */
ori     r2,r2,L1CSR0_DCE
mtspr   L1CSR0,r2       /* enable L1 Dcache */
isync
mtspr   L1CSR1,r2       /* enable L1 Icache */
isync
msync
```

Appendix A: Code Snippets (cont.)

- Setup interrupt vector table

```
  lis     r1,TEXT_BASE@h
 mtspr   IVPR,r1
 li      r1,0x0100
 mtspr   IVOR0,r1        /* 0: Critical input */
```

- Initialize decrementer, enable machine check & branch prediction

```
   li      r0,0x0000
 lis     r1,0xffff
 mtspr   DEC,r0              /* prevent dec exceptions */
 mttbl   r0                  /* prevent fit & wdt exceptions */
 mttbu   r0
 mtspr   TSR,r1              /* clear all timer exception status */
 mtspr   TCR,r0              /* disable all */
 mtspr   ESR,r0              /* clear exception syndrome register */
 mtspr   MCSR,r0             /* machine check syndrome register */
 mtxer   r0                  /* clear integer exception register */
/* Enable Time Base and Select Time Base Clock */
 lis     r0,HID0_EMCP@h      /* Enable machine check */
 ori     r0,r0,HID0_ENMAS7@l  /* Enable 36 bit phys MAS7 */
   ori     r0,r0,HID0_TBEN@l    /* Enable Timebase */
 mtspr   HID0,r0
/* Enable Branch Prediction */
  li      r0,0x201            /* BBFI = 1, BPEN = 1 */
 mtspr   BUCSR,r0
```

Appendix A: Code Snippets (cont.)

- AS=0 -> AS=1

```
/* create a temp mapping in AS=1 to the 4M boot window */
    lis     r6,FSL_BOOKE_MAS0(1, 15, 0)@h
    ori     r6,r6,FSL_BOOKE_MAS0(1, 15, 0)@l

    lis     r7,FSL_BOOKE_MAS1(1, 1, 0, 1, BOOKE_PAGESZ_4M)@h
    ori     r7,r7,FSL_BOOKE_MAS1(1, 1, 0, 1, BOOKE_PAGESZ_4M)@l

    lis     r8,FSL_BOOKE_MAS2(TEXT_BASE & 0xffc00000, (MAS2_I|MAS2_G))@h
    ori     r8,r8,FSL_BOOKE_MAS2(TEXT_BASE & 0xffc00000, (MAS2_I|MAS2_G))@l

    /* The 85xx has the default boot window 0xff800000 - 0xffffffff */
    lis     r9,FSL_BOOKE_MAS3(0xffc00000, 0, (MAS3_SX|MAS3_SW|MAS3_SR))@h
    ori     r9,r9,FSL_BOOKE_MAS3(0xffc00000, 0, (MAS3_SX|MAS3_SW|MAS3_SR))@l

    mtspr   MAS0,r6
    mtspr   MAS1,r7
    mtspr   MAS2,r8
    mtspr   MAS3,r9
    isync
    msync
    tlbwe
     /*
    lis     r6,MSR_CE|MSR_ME|MSR_DE|MSR_IS|MSR_DS@h
    ori     r6,r6,MSR_CE|MSR_ME|MSR_DE|MSR_IS|MSR_DS@l
    lis     r7,switch_as@h
    ori     r7,r7,switch_as@l

    mtspr   SPRN_SRR0,r7
    mtspr   SPRN_SRR1,r6
    rfi
```

Appendix A: Code Snippets (cont.)

- RAM is not available yet; it's good idea to lock cache to be used as RAM during this period

```
    lis     r3,CONFIG_SYS_INIT_RAM_ADDR@h
    ori     r3,r3,CONFIG_SYS_INIT_RAM_ADDR@l
    mfspr   r2, L1CFG0
    andi.   r2, r2, 0x1ff
    /* cache size * 1024 / (2 * L1 line size) */
    slwi    r2, r2, (10 - 1 - L1_CACHE_SHIFT)
    mtctr   r2
    li      r0,0
1:
    dcbz    r0,r3
    dcbtls  0,r0,r3
    addi    r3,r3,CONFIG_SYS_CACHELINE_SIZE
    bdnz    1b
```

Appendix B: List of e300 Mnemonics Not Available in e500

Mnemonic	e300	e500
eieio	√	Replaced with mbar
fabs	√	X
fadds	√	X
fadd	√	X
fcfid	√	X
fcmpo	√	X
fcmpu	√	X
fctidz	√	X
fctid	√	X
fctiwz	√	X
fctiw	√	X
fdivs	√	X
fdiv	√	X
fmadds	√	X
fmadd	√	X
fmr	√	X
fmsubs	√	X
fmsub	√	X

Mnemonic	e300	e500
fmuls	√	X
fmul	√	X
fnabs	√	X
fneg	√	X
fnmadds	√	X
fnmadd	√	X
fnmsubs	√	X
fnmsub	√	X
fres	√	X
frsp	√	X
frsqrte	√	X
fsel	√	X
fsqrts	√	X
fsqrt	√	X
fsubs	√	X
fsub	√	X
lfd	√	X
lfdu	√	X

Appendix B: List of e300 Mnemonics Not Available in e500 (cont.)

Mnemonic	e300	e500
lfdux	√	X
lfdx	√	X
lfs	√	X
lfsu	√	X
lfsux	√	X
lfsx	√	X
lswi	√	X
lswx	√	X
mcrfs	√	X
mfapidi	√	X
mfdcr	√	X
mtdcr	√	X
mtfsb0	√	X
mtfsb1	√	X
mtfsfi	√	X
mtfsf	√	X
stfd	√	X
stfdu	√	X

Mnemonic	e300	e500
stfdux	√	X
stfdx	√	X
stfiwx	√	X
stfs	√	X
stfsu	√	X
stfsux	√	X
stfsx	√	X
stswi	√	X
stswx	√	X


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