MPC8569E Instruction RAM Microcode Package Release 166

General

This release note reflects differences between the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM Rev. 2, and the features which are available for this device using the provided microcode Instruction RAM (IRAM) packages. The following release note reveals any exceptions to the features which are specified in this release of the specification. The notes also describe any addition to the specification or any missing functionality in comparison to the specification.

The user should follow tightly the instructions specified in the QE_Ucode_Loader file provided in the package in relation to the header files containing the code. These instructions assure proper operation and activation of the right features in the code.

Refer to the *QUICC Engine Microcode Errata* for all known issues related to this and other microcode packages.

This package includes the following core blocks: ATM (AAL0, AAL1, AAL2, AAL5), Ethernet (10/100/1000), Plain PPP, ML/MC PPP, PPP MUX, channelized HDLC, transparent, or SS7 protocols, CES, IMA, POS, IP fragmentation, IP Reassembly, Virtual Port, IP/UDP Header Compression, Longest Prefix Match, L2 switch, SPI, HDLC, USB, ESS7, UART, BISYNC, QMC, Serial ATM, and all interworking features. Features of these core blocks that are not supported in this package are described in Table 3.

Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Loader file name (.h)
MPC8569 rev 1.0	8569_IRAM_mpc8569_r1.0.h

Package content

The tables below designate the content of this package. The baseline is the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM Rev. 2. The tables below show additional features and features which are not supported. For the specification of additional features, which are not described in the *QUICC Engine™ Block Reference Manual with Protocol Interworking*, QEIWRM Rev. 2, please contact Freescale support. Contact information may be found at www.freescale.com.

Table 2. New Features (Which are Not Described in QEIWRM Rev. 2)

Feature	Comments
DF bit checking while interworking to Ethernet with IP fragmentation	IP frames with DF bit set on IP header, which violates the MTU configured on Ethernet Tx, will be treated as unrecognized frames and will be dropped according to interworking rules.
Header compression of IP header only (IPonlyHC).	New functionality of header compression for IP header only was added.

Table 3. Removed Features (Described in QEIWRM Rev. 2 but Not Supported)

Feature	Comments	QEIWRM Rev. 2
None		

Revision History

Table 4. Revision History for Release 166

Release Date: Sept. 21, 2009 Revision Register Number: 0xB6900166	
New Features	None
Removed Features	None
Bug Fixes	ATM AAL5/AAL2 Interworking Rx Thread management and synchronization mechanism might fail under heavy traffic load conditions. This can lead to MURAM corruption, packet loss, loss of buffers from the buffer pool and/or thread halt.
	POS-MPHY Tx Error Automatic recovery mode (EAR) is not functional.
	Corrupted bus attributes for External Indexed Table Lookup PCD may lead to wrong behavior on the bus.
	Bus Mode Register corruption on Ethernet Tx operating as Interworking destination. When data is interworked to Ethernet Tx after being altered by Header Manipulation Trailer Removal function, wrong BMR value can be used for DMA transactions which can lead to SDMA exception or loss of coherency between QUICC Engine and CPU.
	Bus Mode Register corruption in Fast Swap mode of Virtual Port. When Virtual Port queues operate in Fast Swap mode, wrong BMR value is used for DMA transactions which can lead to SDMA exception or loss of coherency between QUICC Engine and CPU.
	Possible race condition for ATM transmit command. Valid channels might be deleted from the APC.
	When enqueue busy or FBP busy conditions are encountered on Ethernet Interworking Rx and associated interrupts are unmasked, SDMA exception can occur on Ethernet Rx thread SNUMs leading to Ethernet Rx hang condition. Loss of coherency between QUICC Engine and CPU can occur due to the same issue.
	L2 switch TCBDs may not function properly. Bus Mode Register may not be loaded when using TCBDs.

Table 5. Revision History for Release 158

Release Date: Jun 29, 2009 Revision Register Number: 0xB6900158	
New Features	None
Removed Features	None
Bug Fixes	Initial public release

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