Product Type	Security Co-Processor
Freescale Part #	MPC180LM
Name	Titan
Package	100 LQFP

		Max Key Size (bits)
Algorithms	DES (ECB, CBC)	56
	3DES (ECB, CBC)	168 (3-keys)
	ARC-4	128
	MD-5+ HMAC	(up to 512 bit keys)
	SHA-1+ HMAC	(up to 512 bit keys)
	SHA-256+ HMAC	(up to 512 bit keys)
	RSA Digital Signature	2048-bit operands
	RSA Digital Verify	2048-bit operands
	ECC Digital Signature	512-bit field or modulus size
	ECC Digital Verify	512-bit field or modulus size
	RNG	On chip 32-bit

Target Applications :
DSLAMs, Broadband Gateways, mid-range routers, wireless access points, telecom equipment

Export Control Info:
Harmonized Tariff (US): 8542.31.0000
ENC Status: Restricted. US EAR part 740.17(b)(2)
ECCN: 5A002
CCAT: G018833

Overview:
The MPC180 is a memory-mapped device designed to interface to the Motorola PowerQUICC families of integrated Communications processors (MPC860/8260). The MPC180 behaves only as a bus slave. As a bus slave, an application being executed on a PowerQUICC can accelerate cryptographic functions by writing instructions, keys, and data to the MPC180, and reading the result. The MPC180 is expected to achieve 25 public key exchanges per second, and ~80Mbps 3DES throughput.